XPK8120

Single-Phase Synchronous Buck PWM Controller

FEATURES

- Wide Input Voltage Range : 3V to 13.5V
- Embedded Switching Boot Diode
- 0.8V ±1%, 0.6V ±1.5% Internal Reference
- Shoot-Through Protection and Short Pulse Free Technology for Gate Drivers
- Fixed Frequency 300kHz
- Internal Soft-Start
- Over Current Protection by Sensing MOSFET $R_{DS(ON)}$
- Enable/Shutdown Control
- Drives Two N-MOSFETs
- Full Duty Cycle : 0% to 85%
- Fast Transient Response
- Voltage Mode PWM Control with External Feedback Loop Compensation
- Pinless LGATE Over Current Setting (LGOCS)
- Under Voltage Protection
- SOP-8 (Exposed Pad) Package
- RoHS Compliant and Halogen Free

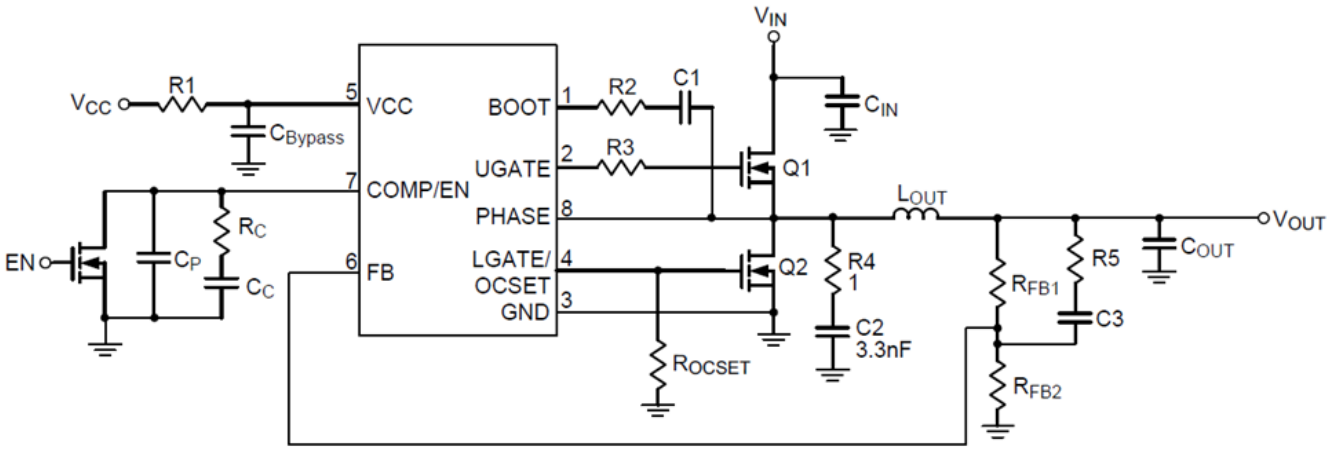
APPLICATIONS

- System (Graphic, MB) with 5V or 12V Power
- Graphic Cards (AGP 8X, 4X, PCI Express*16)
- 3.3V to 12V Input DC-DC Regulators
- Low Voltage Distributed Power Supplies

DESCRIPTION

The XPK8120 is a single-phase synchronous buck PWM DC-DC controller designed to drive two N-MOSFET. It provides a highly accurate, programmable output voltage precisely regulated to low voltage requirements with an internal 0.8V ±1% (option for 0.6V ±1.5%) reference. The XPK8120 uses a single feedback loop voltage mode PWM control for fast transient response. An oscillator with fixed frequency 300kHz reduces the external inductor and capacitor component size for saving PCB board area. The XPK8120 provides fast transient response to satisfy high current output applications while minimizing external components. It is suitable for high performance graphic processors, DDR and VTT power. The XPK8120 incorporates an externally compensated error amplifier and an internal soft-start and output enable. The XPK8120 comes in SOP-8 (Exposed Pad) package.

TYPICAL APPLICATION



REVISION HISTORY

Release	Rev	Changes	Date
Released	0.8	Updates	12/25/2023

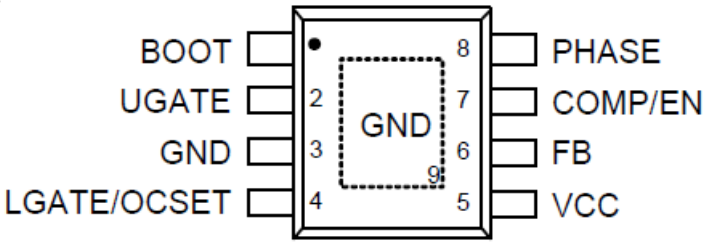
ORDERING INFORMATION

Part Number	VREF (V)	VIN Detection	Top Marking	MPQ
XPK8120A	0.8	X	8120A	3,000
XPK8120B	0.6	X	8120B	3,000
XPK8120C	0.8	V	8120C	3,000
XPK8120D	0.6	V	8120D	3,000

MPQ = Minimum Packaging Quantity.
For production orders greater than MPQ, the order must be a multiple of MPQ per package size above.

PIN CONFIGURATION AND DESCRIPTION

Top View



SOP-8 (Exposed Pad)

Pin Configuration

Pin	Name	Description
1	BOOT	Bootstrap Power Pin. This pin powers the upper gate driver. Connect a bootstrap capacitor between the BOOT pin and PHASE pin on the upper MOSFET.
2	UGATE	Upper-Gate Driver Output. Connect to gate of the high side power N-MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
3/9	GND	Ground for the IC. All voltage levels are measured with respect to this pin. Connect this pin directly to the low side MOSFET source and ground plane with the lowest impedance. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
4	LGATE/OCSET	Lower-Gate Driver Output. Connect to the gate of the low side power N-MOSFET. It provides the PWM-controlled gate drive (from VCC). This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off. During a short period of time following Power-On Reset (POR) or shutdown release, this pin is also used to determine the over-current threshold of the converter (LGOCS). Connect a resistor (R_{OCSET}) from this pin to GND. See the over current protection section for equations.
5	VCC	Supply Input Pin. Connect this pin to a well-decoupled 5V or 12V bias supply. It is also the positive supply for the lower gate driver, LGATE.
6	FB	Feedback Input Pin. This pin is the inverting input of the error amplifier. FB senses the switch output through an external resistor divider network.
7	COMP/EN	Feedback Compensation. And could be used as EN pin, when COMP < 0.4V, to disable entire chip.
8	PHASE	Switch Node. Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET.

ABSOLUTE MAXIMUM RATINGS(1)

Parameter	Min	Max	Units
VCC to GND, VCC		15	V
BOOT to PHASE, VBOOT−PHASE		15	V
PHASE to GND (DC)	-0.5	15	V
PHASE to GND (<20ns)	-8	25	V
UGATE to PHASE (DC)	-0.3	VBOOT−PHASE + 0.3	V
UGATE to PHASE (<20ns)	-5	VBOOT−PHASE + 5	V
LGATE to GND (DC)	-0.3	VCC + 0.3	V
LGATE to GND (<20ns)	-5	VCC + 5	V
Storage Temperature Range	-65	150	°C
Junction Temperature		150	°C
Lead Temperature (Soldering, 10 sec.)		260	°C
Power Dissipation, PD @ TA=25°C SOP-8 (Exposed Pad)		3.26	W
Electrostatic Discharge (HBM)	-2000	+2000	V

(1) Operation of the device outside of these parameters may cause permanent damage.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Units
Supply Input Voltage, VIN	V_{IN}	3	13.5	V
Control Input Voltage, VCC	VCC	4.5	13.5	V
Junction Temperature Range	T_{OJ}	-40	+125	°C
Ambient Temperature Range	T_{OA}	-40	+85	°C

Thermal Information

Junction to ambient thermal resistance is a function of board layout and ambient air flow condition. This data is based on four layers PCB (30mm x 30mm; 70µm Cu top signal layer) in still air box in accordance with JEDEC standard JESD51 on natural convection.

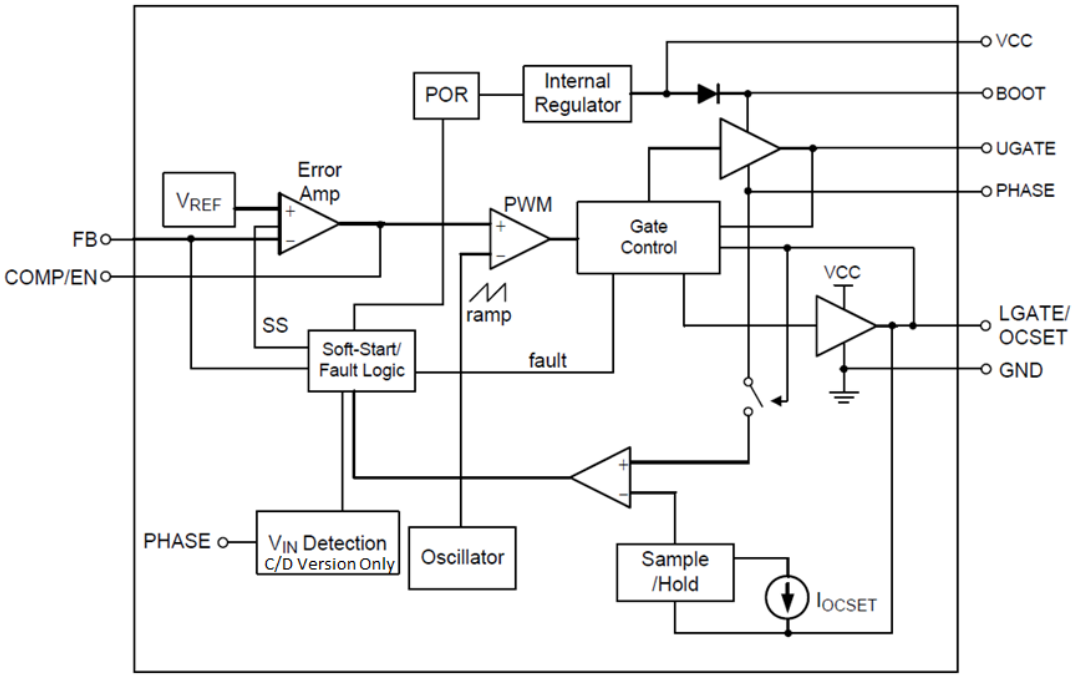
Parameter	Symbol	Typ	Units
Junction-to-Ambient Thermal Resistance	θ_{JA}	30.6	°C/W
Junction-to- Case Thermal Resistance	θ_{JC}	3.4	°C/W

ELECTRICAL SPECIFICATIONS

Typical values unless otherwise noted: Ambient Temperature = +25°C.

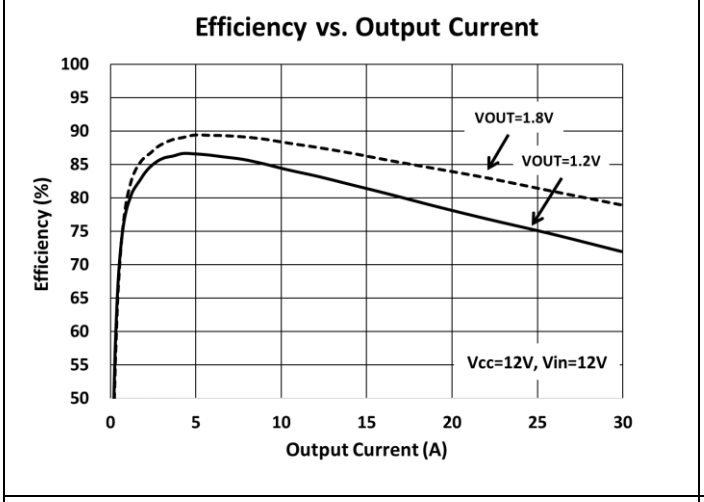
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
DC Characteristics						
Supply Current	ICC			1.5		mA
Shutdown Current	ISHDN			0.7		mA
Power On Reset Threshold	VCCR_TH		4.1	4.2	4.3	V
Power On Reset Hysteresis	VCCR_HYS				0.3	V
Switching Frequency	fOSC		270	300	330	kHz
Ramp Amplitude	ΔVOSC			1.3		Vp-p
Minimum Duty Cycle			0			%
Maximum Duty Cycle	DMAX			85		%
Reference Voltage	VREF	B/D Version	0.591	0.6	0.609	V
		A/C Version	0.792	0.8	0.808	V
Error Amplifier						
Open Loop DC Gain	ADC	Guaranteed by Design		70		dB
Gain Bandwidth	GBW	Guaranteed by Design		10		MHz
Slew Rate	SR	Guaranteed by Design, CL = 10pF		6		V/us
Transconductance	gm		500	700		uA/V
Output Source Current	ICOMPSK	VFB < VREF	80	130		uA
Output Sink Current	ICOMPSC	VFB < VREF	80	130		uA
Soft-Start Time	tSS	A/C Version		1.5		ms
		B/D Version		2		ms
Pre-drivier						
Upper Gate Sourcing Ability	IUG_SRC	VBOOT - VPHASE = 12V, max source current		1.2		A
Upper Gate RDS(ON) Sinking	RUG_SNK	VUGATE - VPHASE = 0.1V		3		Ohm
Lower Gate Sourcing Ability	ILG_SRC	VCC = 12V, max source current		1.2		A
Lower Gate RDS(ON) Sinking	RLG_SNK	VLGATE = 0.1V		1.8		Ohm
Deadtime between UGATE Off to LGATE On		VUGATE - VPHASE = 1.2V to VLGATE =1.2V		30		ns
Deadtime Between LGATE Off to UGATE On		VUGATE - VPHASE = 1.2V to VLGATE = 1.2V		30		ns
Internal BOOT Switch On-Resistance	RBOOT	VCC to BOOT, 10mA			80	Ohm
Protection						
Under Voltage Protection	VUVP_FB		65	75	80	%
Under Voltage Delay	VD_UVP			7		us
LGATE OC Setting Current	IOCSET		9	10	11	uA
Over Current Threshold	VPHASE	ROCSET = Open		375		mV
Enable Threshold	VEN		0.3	0.4	0.55	V

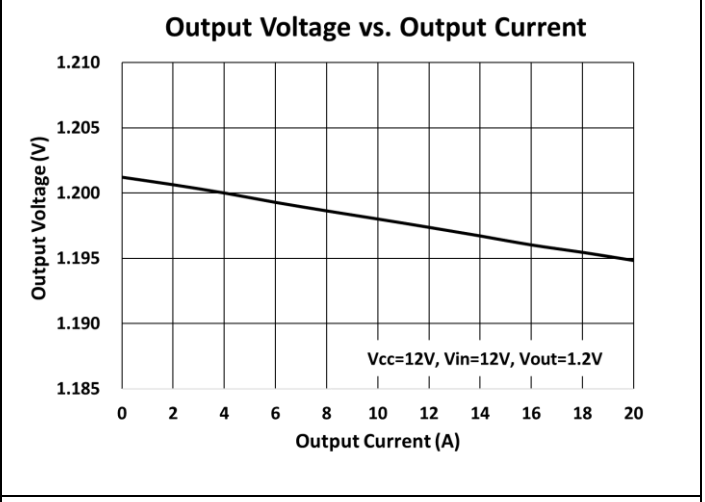
FUNCTIONAL DESCRIPTION

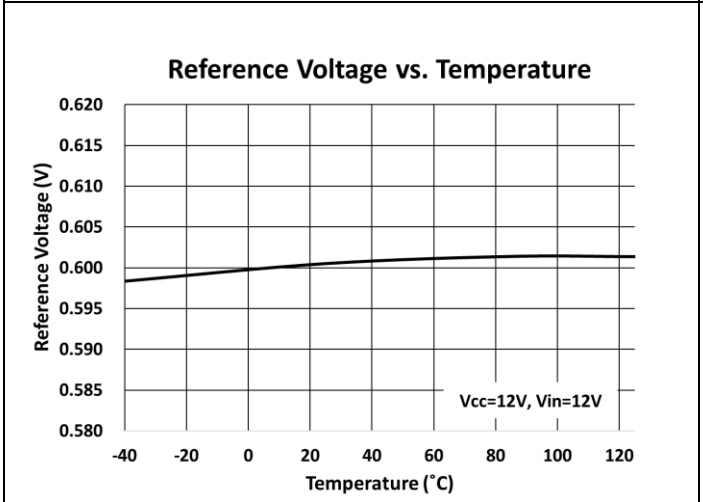


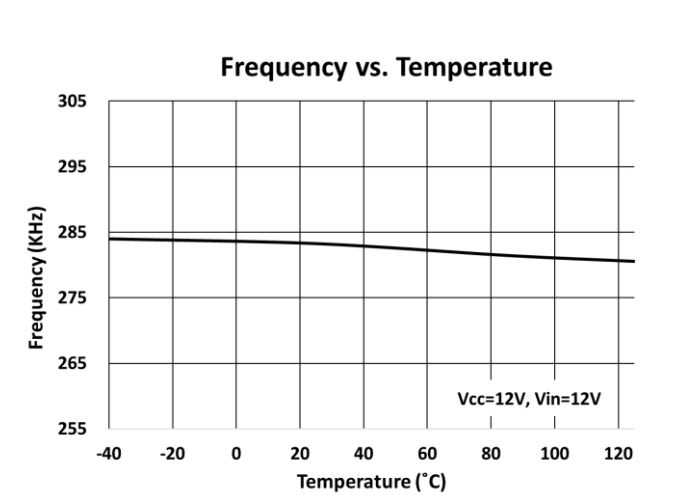
Block diagram

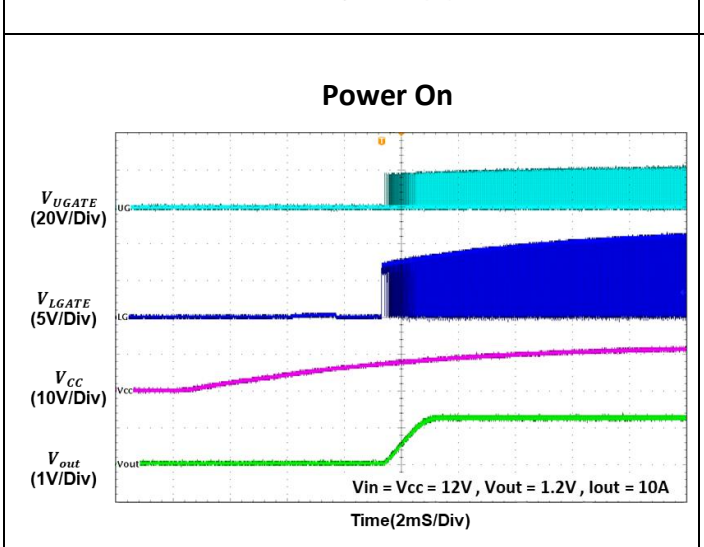
Typical Operating Characteristics

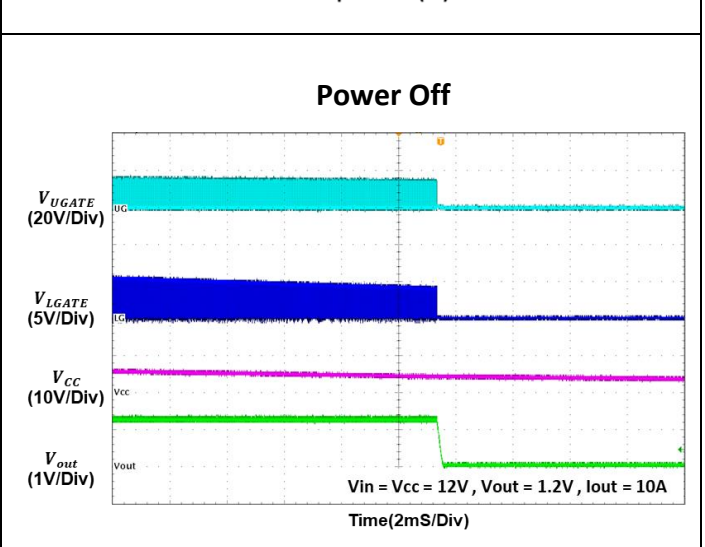




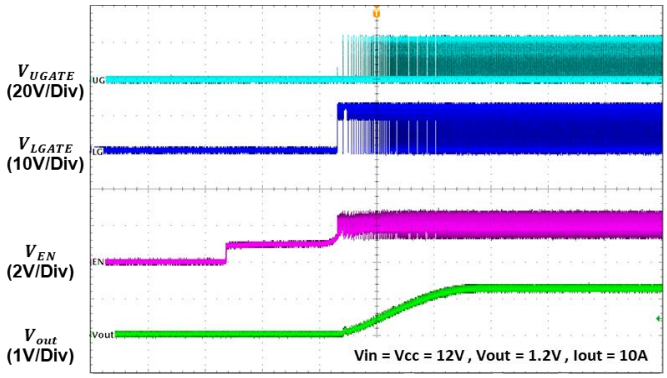




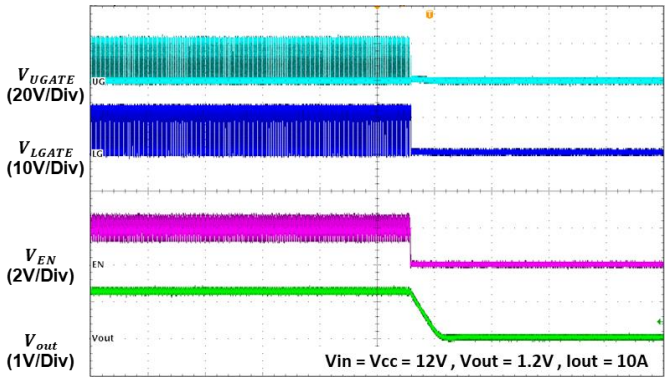




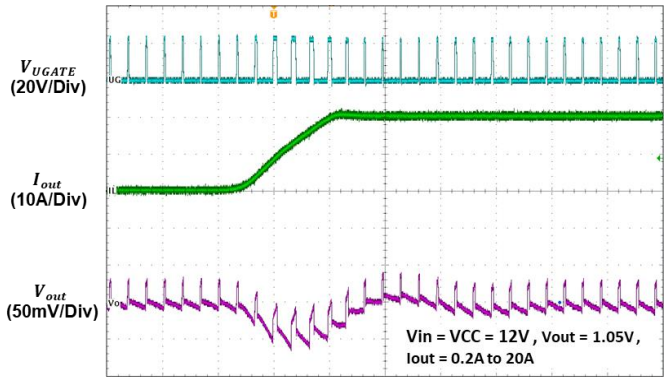
COMP/EN Power On



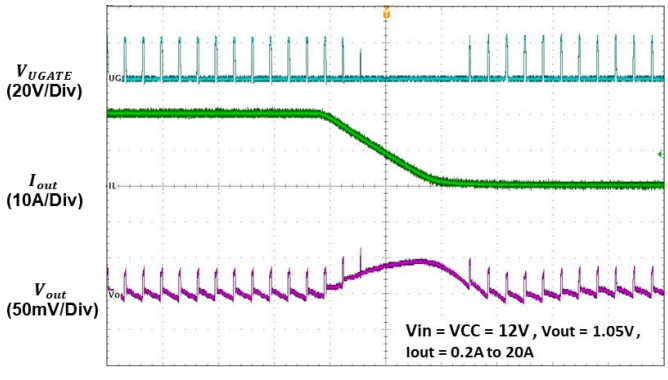
COMP/EN Power Off



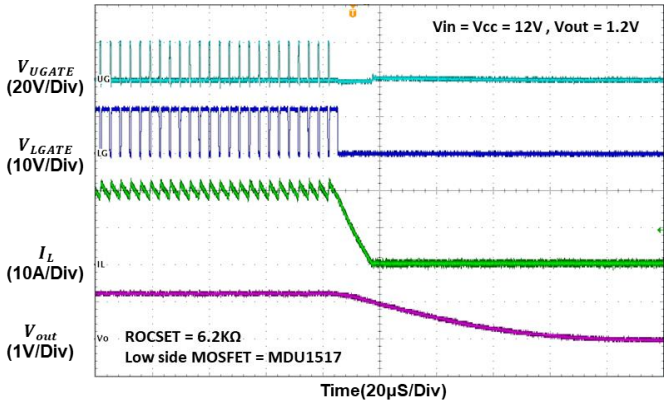
Load Transient Response



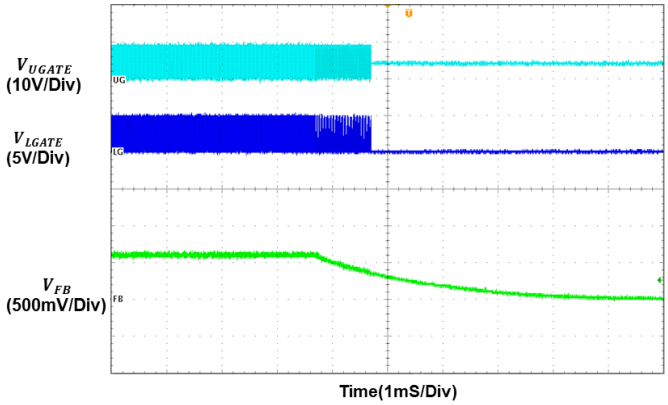
Load Transient Response



Over Current Protection



Under Voltage Protection



Application Information

Function Description
The XPK8120 is a single-phase synchronous buck PWM controller with integrated N-MOSFET gate drivers. The XPK8120 can be used in a broad variety of applications, with its wide input voltage range from 3V to 13.5V. It provides single feedback loop, voltage mode control with fast transient response. An internal 0.8V (option for 0.6V) reference allows the output voltage to be precisely regulated for low output voltage applications. A fixed frequency (300kHz) oscillator is integrated to minimize external components. Protection features include programmable over current protection and Under Voltage Lockout (UVLO).

Supply Voltage and Power On Reset (POR)
The input voltage range for VCC is from 4.5 V to 13.5 V with respect to GND. An internal linear regulator regulates the supply voltage for internal control logic circuit. A minimum 0.1uF ceramic capacitor is recommended to bypass the supply voltage. Place the bypassing capacitor physically near the IC. VCC also supplies the integrated MOSFET drivers. A bootstrap diode is embedded to facilitate PCB design and reduce the total BOM cost. No external Schottky diode is required in real applications.
The Power-On Reset (POR) circuit monitors the supply voltage at the VCC pin. If VCC exceeds the POR rising threshold voltage (typ. 4.2V), the controller resets and prepares the PWM for operation. If VCC falls below the POR falling threshold during normal operation, all MOSFETs stop switching. The POR rising and falling threshold has a hysteresis (typ.0.25V) to prevent unintentional noise-based reset.

Chip Enable and Disable
The COMP/EN pin of the XPK8120 is a multiplexed pin. During soft-start and normal converter operation, this pin represents the output of the error amplifier. When COMP/EN pin voltage falls or is pulled externally below the enable level V_{EN}, the chip shuts down. When the controller shuts down, UGATE and LGATE signals will go low. When the pull-down device is released and the COMP/EN pin rises above the V_{EN} trip point, the XPK8120 will begin a new initialization and soft-start cycle. This allows flexible power sequence control for specified application. In practical applications, connect a small-signal MOSFET to the COMP/EN pin to implement the enable/disable function.

VIN Detection (XPK8120C/D Only)
Once VCC exceeds its power on reset (POR) rising threshold voltage, UGATE will output continuous pulses (~60kHz, 200ns), and LGATE will be forced low for converter input voltage V_{IN} detection. If the voltage pulses at the PHASE pin exceed 1V when UGATE is turned on, V_{IN} is recognized as ready. Then, the controller will initiate soft-start operation.

Internal Soft-Start
The XPK8120 provides an internal soft-start function. The soft-start function is used to prevent large inrush current and output voltage overshoot while the converter is being powered-up. The soft-start function automatically begins once the chip is enabled. An internal current source charges the internal soft-start capacitor such that the internal soft-start voltage ramps up uniformly. The FB voltage will track the internal soft-start voltage during the soft-start interval. Therefore, the PWM pulse width increases gradually to limit the input current. After the internal soft-start voltage exceeds the reference voltage, the FB voltage no longer tracks the soft-start voltage but rather follows the reference voltage. Therefore, the duty cycle of the UGATE signal as well as the input current at power up are limited.

Over Current Protection (OCP)
The XPK8120 provides lossless over current protection by detecting the voltage drop across the low side MOSFET when it is turned on. The over current trip threshold is set by an external resistor, R_{OCSET}, at LGATE. During the initial stage when LGATE is turned on, the XPK8120 samples and holds the phase voltage. The sample-and-hold voltage represents the valley inductor current and is compared to the OCP threshold. If the sensed phase voltage is lower than the OCP threshold, OCP will be triggered. Both UGATE and LGATE will go low, and the controller will enter the hiccup mode until the OCP condition is released.

LGATE Over Current Setting (LGOCS)
Over current threshold is externally programmed by adding a resistor (R_{OCSET}) between LGATE and GND. Once VCC exceeds the POR threshold, an internal current source I_{OCSET} flows through R_{OCSET}. The voltage across R_{OCSET} is stored as the over current protection threshold V_{OCSET}. After that, the current source is switched off. R_{OCSET} can be determined using the following equation :

$$R_{OCSET} = \frac{I_{VALLEY} \times R_{LGDS(ON)}}{I_{OCSET}}$$

where I_{VALLEY} represents the desired inductor OCP trip current (valley inductor current). If R_{OCSET} is not present, there is no current path for I_{OCSET} to build the OCP threshold. In this situation, the OCP threshold is internally preset to 375mV (typical).

Under Voltage Protection (UVP)

The voltage on the FB pin is monitored for under voltage protection. If the FB voltage is lower than the UVP threshold (typically 75% x V_{REF}) during normal operation, UVP will be triggered. When the UVP is triggered, both UGATE and LGATE go low. The controller enters hiccup mode until the UVP condition is removed.

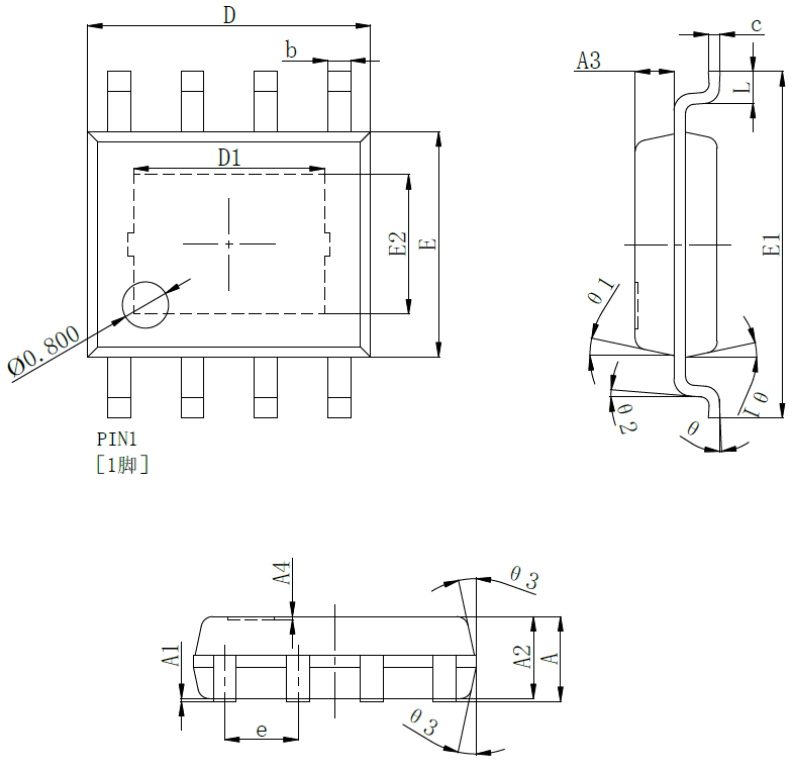
Output Voltage Setting

The XPK8120 allows the output voltage of the DC/DC converter to be adjusted from 0.8V (option for 0.6V) to 85% of V_{IN} via an external resistor divider. It will try to maintain the feedback pin at internal reference voltage (0.8V, with option for 0.6V). Output Voltage Setting According to the resistor divider network above, the output voltage is set as :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

Physical Dimensions

SOP-8 (Exposed Pad) Package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.300	1.500	1.700
A1	0.000	0.100	0.150
A2	1.350	1.420	1.550
A3	0.645	0.670	0.695
A4	0.020	--	0.050
c	0.170	0.203	0.250
E	3.800	3.900	4.000
E1	5.800	6.000	6.200
L	0.450	0.600	0.750
b	0.330	0.400	0.510
D	4.800	4.900	5.000
e	1.270BSC		
θ	0°	3°	8°
θ1	12° REF.		
θ2	5° REF.		
θ3	12° REF.		

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D1	3.272	3.372	3.472
E2	2.183	2.283	2.383

Package Marking and Reel Information

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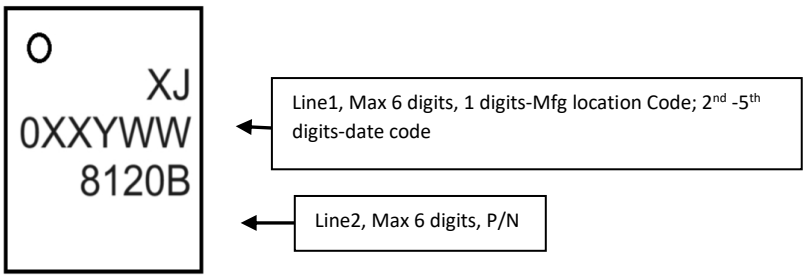
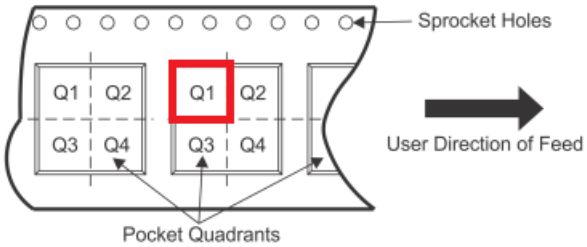


Pin 1 located in Q1 direction in T&R



Remark:

Font: Arial

Letter height of 0.5mm

Side pitch of 0.4mm

Line space of 0.25mm

Logo of XINJI should be required and placed on assigned Logo position as upside illustration.

Trace-ability Code:

Manufacturing Location Code + Assembly lot#+Year Code+WK code Line 1

a) 1st digit: assembly location code: ZUNYANG: 0
b) 2nd & 3rd digit: Assembly lot number
c) 4th digit: Year code:

Year Code 2020-2051

Year	Code
2020	0
2021	1
2022	2
2023	3
2024	4
2025	5
2026	7
2027	C

Year	Code
2028	D
2029	E
2030	F
2031	H
2032	I
2033	J
2034	K
2035	L

Year	Code
2036	N
2037	P
2038	R
2039	S
2040	T
2041	U
2042	V
2043	X

Year	Code
2044	Y
2045	Z
2046	b
2047	c
2048	d
2049	h
2050	i
2051	j

d)5th & 6th digit: Week code, 01 means the 1st Work Week base on XinJi's calendar.

Product Number Code: Line2

Product Name	P/N Code	Remark
XPK8120B	8120B	