10-Channel LED Driver and GPIO Controller

FEATURES

- 10-channel LED constant-current driver, each channel can be used for GPIO
- OUT0~OUT5 support 2 intelligent breathing mode: BLINK and SMART-FADE, breathing time is adjustable
- Support 256 steps linearity dimming, I_{MAX} is 37mA
- Support GPIO input/output mode
- GPIO input mode, internal 8μs debounce
- Compatible I²C Interface, V_{IO}: 1.8V ~ 3.3V
- I²C address: 0x58/0x59/0x5A/0x5B
- Support shutdown function, low level effective
- Simple Voltage Range VCC: 2.5V~5.5V
- QFN 3×3-20L Package

APPLICATIONS

Mobile Phones/ Portable Media Player

Home Appliances

GENERAL DESCRIPTION

AW9110CQNR is a 10-channel LED controller with I²C interface. Each channel can be used for GPIO. LED dimming combined with extended GPIO function, which can give full play to the application value of single chip.

AW9110CQNR configures the current level to realize 256 steps linear dimming with I²C interface. The default I_{MAX} current is 37mA.

When OUTx(x=0~9) works in a GPIO input mode, AW9110C detected input state to occur interrupt with internal 8μs debounce.

AW9110CQNR supports two intelligent breathing modes: BLINK mode and SMART-FADE mode. BLINK mode allows LED automatic to flash periodically according the setting time parameter. OUT0~OUT5 support intelligent breathing mode.

AW9110CQNR is available in QFN 3×3-20L package. The operating voltage range is 2.5V~5.5V.

TYPICAL APPLICATION CIRCUIT

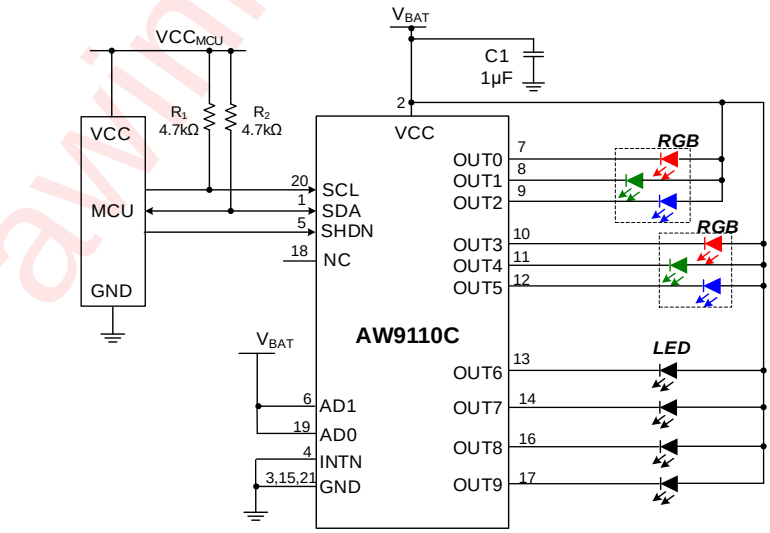
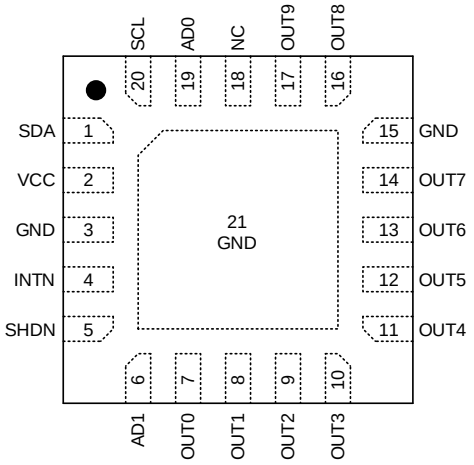


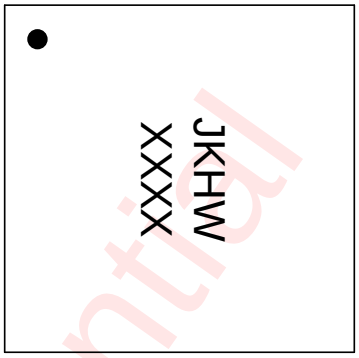
Figure 1 AW9110C Typical Application Circuit

PIN CONFIGURATION AND TOP MARK

AW9110CQNR
(Top View)



AW9110CQNR Marking
(Top View)



JKHW – AW9110CQNR
XXXX - Production Tracing Code

PIN DEFINITION

NO	NAME	DESCRIPTION
1	SDA	Serial Data I/O for I²C Interface
2	VCC	Power Supply
3	GND	Power Ground
4	INTN	Interrupt Output, Low Active
5	SHDN	Shutdown Pin, Low Active
6	AD1	I²C Address Pin
7	OUT0	Defaults to GPIO, LED driver configurable, support intelligence breathing mode. The default state after power on according to the level of AD1/AD0 PIN
8	OUT1	Defaults to GPIO, LED driver configurable, support intelligence breathing mode. The default state after power on according to the level of AD1/AD0 PIN
9	OUT2	Defaults to GPIO, LED driver configurable, support intelligence breathing mode. The default state after power on according to the level of AD1/AD0 PIN
10	OUT3	Defaults to GPIO, LED driver configurable, support intelligence breathing mode. The default state after power on according to the level of AD1/AD0 PIN
11	OUT4	Defaults to GPIO, LED driver configurable, support intelligence breathing mode. The default state after power on according to the level of AD1/AD0 PIN
12	OUT5	Defaults to GPIO, LED driver configurable, support intelligence breathing mode. The default state after power on according to the level of AD1/AD0 PIN
13	OUT6	Defaults to GPIO, LED driver configurable. The default state after power on according to the level of AD1/AD0 PIN
14	OUT7	Defaults to GPIO, LED driver configurable. The default state after power on according to the level of AD1/AD0 PIN
15	GND	Power Ground
16	OUT8	Defaults to GPIO, LED driver configurable. The default state after power on according to the level of AD1/AD0 PIN
17	OUT9	Defaults to GPIO, LED driver configurable. The default state after power on according to the level of AD1/AD0 PIN
18	NC	NC
19	AD0	I²C Address Pin
20	SCL	Serial Clock Input for I²C Interface
21	GND	Ground

FUNCTIONAL BLOCK DIAGRAM

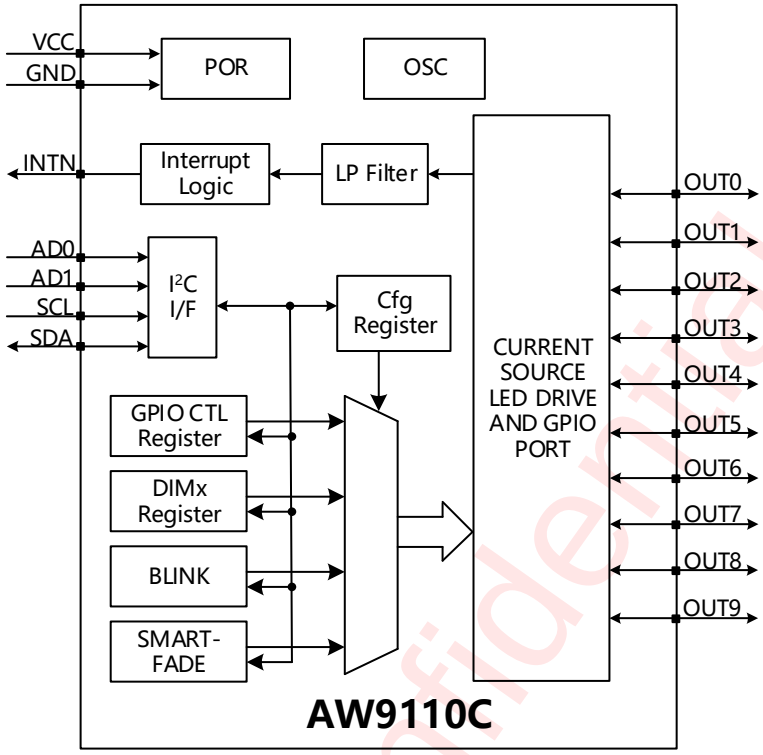
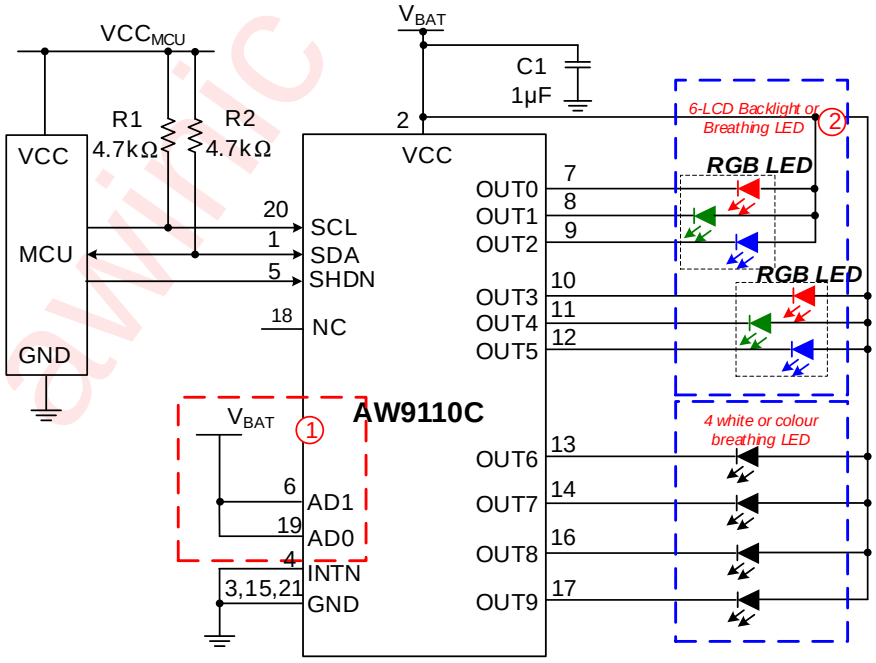


Figure 2 FUNCTIONAL BLOCK DIAGRAM

TYPICAL APPLICATION CIRCUITS

Using Single Chip To Realize 10-LED Breathing Or 6 LCD Backlight Control



1. When the anode of LED is connected to VBAT, AD1/AD0 of the chip should be connected to VBAT to ensure the default electricity state of GPIO is high or high resistance and the LED will be off. The default electricity state of GPIO is decided by AD1/AD0 level.

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW9110CQNR	-40°C～85°C	QFN3×3-20L	JKHW	MSL3	ROHS+HF	6000 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS(NOTE 1)

Parameter	Range
Supply Voltage range VCC	-0.3V to 6 V
SCL,SDA,AD0,AD1,INTN,SHDN,OUT0-9 PINs voltage range	-0.3V to V_{CC}
Max power dissipation (PD_{max}, package@ TA=25℃)	3.2 W
Package thermal resistance θ_{JA}	49°C /W
Maximum Junction temperature T_{Jmax}	125°C
Storage temperature range	-65°C to 150°C
Lead temperature (Sodering 10 Seconds)	260°C
ESD(NOTE 2)	
HBM(All Pins)	±4000V
CDM(All Pins)	±1500V
Latch-up	
Test Condition： JEDEC STANDARD NO.78E NOVEMBER 2016	+IT：+450mA -IT：-450mA

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883J Method 3015.9. The CDM test is based on JEDEC EIA/JESD22-C101F.

ELECTRICAL CHARACTERISTICS

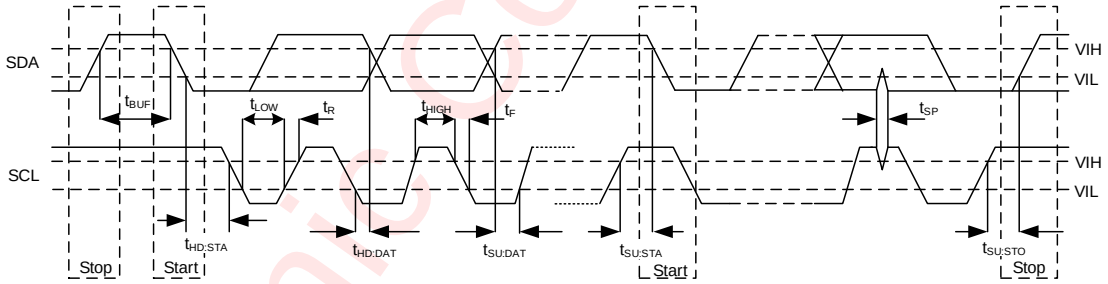
V_{CC}=3.8V, T_A=25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYPE	MAX	UNIT
Power supply voltage and current						
V_{CC}	Input voltage	T_A=-40°C ~85°C	2.5		5.5	V
V_{POR}	Power on reset voltage	T_A=-40°C ~85°C		1.8	2.3	V
$I_{SHUTDOWN}$	Current in Shutdown mode	SHDN=0V		0.5	2	μA
$I_{STANDBY}$	Current in Standby mode	SHDN=1.8V		0.8	2	μA
I_{ACTIVE}	Current in GPIO mode(SHDN=V_{CC})	GPIO mode Trigger Interrupt		50	70	μA
	Current in LED mode	INTN=0V, P0WKMD=0x00, P1WKMD=0x00, GCC<1:0>=11, DIMx=0xFF		3.6		mA
Digital output						
V_{OH}	Output high level(OUT0~9)	VCC=2.5V,I_{SOURCE}=10mA	V_{CC}-450	Vcc-360	V_{CC}-280	mV
		VCC=3.6V,I_{SOURCE}=20mA	V_{CC}-400	Vcc-240	V_{CC}-160	mV
		VCC=5V,I_{SOURCE}=20mA	V_{CC}-350	Vcc-180	V_{CC}-100	mV
V_{OL}	Output low level(OUT0~9)	VCC=2.5V,I_{SINK}=20mA	60	90	400	mV
		VCC=3.6V,I_{SINK}=20mA	40	60	300	mV
		VCC=5V,I_{SINK}=20mA	30	50	250	mV
	Output low level (SDA,INTN)	VCC=2.5V,I_{SINK}=6mA	40	70	300	mV
		VCC=3.6V,I_{SINK}=6mA	20	50	150	mV
		VCC=5V,I_{SINK}=6mA	10	40	120	mV
Digital input						
V_{IH}	Logic high level (SCL,SDA,SHDN,AD0,AD1,OUT0~9)		1.4			V
V_{IL}	Logic low level (SCL,SDA,SHDN,AD0,AD1,OUT0~9)				0.4	V
I_{IH},I_{IL}	Input current (SCL,SDA,AD0,AD1,OUT0~9)	V_I=VCC or GND	-0.2		+0.2	μA
$R_{\_SHDN}$	Resistant of shutdown pin			1M		Ω
C_I	Input capacitor (SCL,SDA,SHDN,AD0,AD1,OUT0~9)	V_I=VCC or GND		3		pF
t_{SP_SHDN}	Low burr pulse width	SHDN=VCC		10		μs
LED driver						
I_{MAX1}	Current Source	GCC<1:0>=11,DIMx=FFH	7.35	9.25	11.25	mA
I_{MAX2}	Current Source	GCC<1:0>=10,DIMx=FFH	14.75	18.5	22.25	mA
I_{MAX3}	Current Source	GCC<1:0>=01,DIMx=FFH	22.35	27.75	33.65	mA
I_{MAX4}	Current Source	GCC<1:0>=00,DIMx=FFH	31.95	37	43.05	mA
C_I	Input capacitor (SCL,SDA,SHDN,AD0,AD1,OUT0~9)	V_I=VCC or GND		3		pF

V_{drop}	OUT0~9 output voltage drop	I_{OUT}=21mA,GCC<1:0>=01, DIMx=C0H		90	200	mV
OSC	Oscillator Frequency		0.72	0.8	0.88	MHz
T_{FD_ON}	Fade on time	FDON_TMR<1:0>=010	441	630	819	ms
T_{FD_OFF}	Fade off time	FDOFF_TMR<1:0>=010	441	630	819	ms

I²C INTERFACE TIMING

PARAMETER		FAST MODE		FAST MODE PLUS		UNIT
		MIN	MAX	MIN	MAX	
F_{SCL}	Interface clock frequency	-	400	-	1000	kHz
$T_{HD:STA}$	(Repeat-start) START condition hold time	0.6	-	0.26	-	μs
T_{LOW}	Low level width of SCL	1.3	-	0.5	-	μs
T_{HIGH}	High level width of SCL	0.6	-	0.26	-	μs
$T_{SU:STA}$	(Repeat-start) START condition setup time	0.6	-	0.26	-	μs
$T_{HD:DAT}$	Data hold time	0	-	0	-	μs
$T_{SU:DAT}$	Data setup time	0.1	-	0.05	-	μs
T_R	Rising time of SDA and SCL	-	0.3	-	0.12	μs
T_F	Falling time of SDA and SCL	-	0.3	-	0.12	μs
$T_{SU:STO}$	STOP condition setup time	0.6	-	0.26	-	μs
T_{BUF}	Time between start and stop condition	1.3	-	0.5	-	μs



FUNCTIONAL DESCRIPTION

AW9110C is a 10 channel co-anode current breathing led driver. There is 256 current levels configurable via register DIM0~DIM9. The maximum driver current I_{MAX} is 37mA.

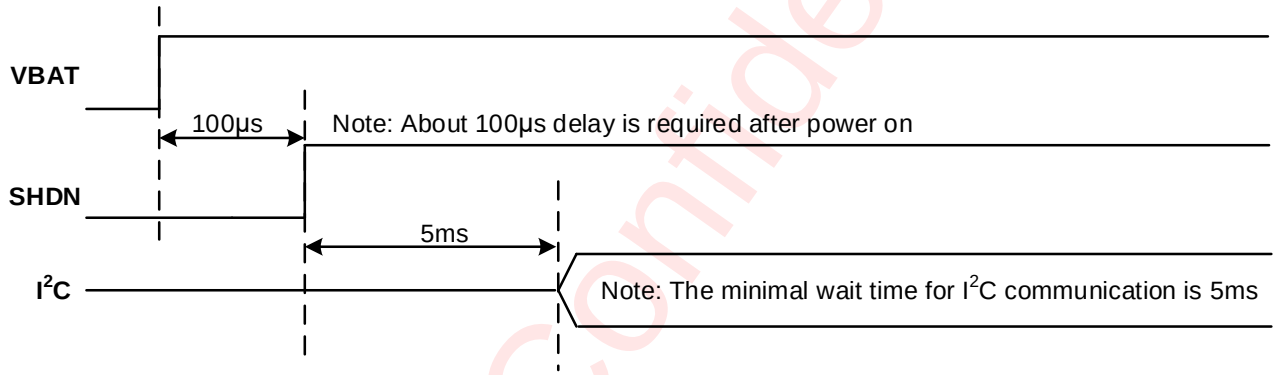
The LED drivers and GPIO functions can be switch with configuring register P0WKMD/P1WKMD. The default status of OUT0~OUT9 are used for GPIO function.

AW9110C supports two types of intelligent breathing modes: BLINK and SMART-FADE. In BLINK mode, AW9110C completes "fade-on" and "fade-off" breathing periodically. In SMART-FADE mode, AW9110C runs "fade-on" and "fade-off" independently with register P0DO/ P1DO configuration.

Shutdown And Reset

AW9110C enters shutdown mode when SHDN is low level. When SHDN is pulled up from shutdown state, AW9110C enters standby mode and will be reset to the default state.

Below is the recommended operation timing：



AW9110C offers two kinds of reset function：

- Power on reset -- 5ms after power on, the chip is reset to the default state.
- Hardware reset – keep SHDN low level over 20 μs, reset all internal circuit.
- Software reset -- write 00H to register 7FH, reset all internal circuit.

When AW9110C is reset, the default state of OUTx pin is GPIO.

LED Dimming Function

AW9110C LED driver uses co-anode current source. In default status, the maximum driving current I_{MAX} is 37mA.

After power on, OUTx(x=0~9) used for GPIO. AW9110C can switch OUTx to LED driver mode with configuring P0WKMD/P1WKMD, shown in Table 4&5.

AW9110C configures four dimming range by GCR [1:0], 0~I_{MAX4}(default), 0~I_{MAX3}, 0~I_{MAX2} or 0~I_{MAX1}, which means 256 steps dimming range: 0~37mA(default), 0~27.75mA, 0~18.5mA or 0~9.25mA. GCR[1:0] configuration is refer to Table 3.

The dimming level of each channel is configured by DIMx(x=0~9) register. 8-bits DIMx can be configured to 256 levels, from 00H to FFH.

DIMx bit								Dimming level
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	1/255×I_{MAX}
0	0	0	0	0	0	1	0	2/255×I_{MAX}
……								……
1	1	1	1	1	1	0	1	253/255×I_{MAX}
1	1	1	1	1	1	1	0	254/255×I_{MAX}
1	1	1	1	1	1	1	1	255/255×I_{MAX}

GPIO Function

When AW9110C is used in GPIO, the direction of OUTx is configured by P0DIR / P1DIR (Table13, 14). When OUTx is configured to output, write P0DO or P1DO register (Table11, 12) driver high or low level.

The following Table shows OUTx default output driving value after power on, whether SHDN is low or high.

AD1	AD0	OUT9	OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
GND	GND	0	0	0	0	0	0	0	0	0	0
GND	VCC	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	1	1	1	1
VCC	GND	Hi-Z	Hi-Z	0	0	0	0	0	0	0	0
VCC	VCC	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	1	1	1	1

When OUTx is configured to input mode, the logic level of OUTx can be acquired with reading P0DI or P1DI register (Table 9, 10). AW9110C can support 1.8V level logic.

OUT0~OUT3 are default to PUSH-PULL driver. OUT4~OUT9 are default to OPEN-DRAIN driver and can be configured as PUSH-PULL driver with GCR.GPMD0 (Table 3).

Interrupt Function

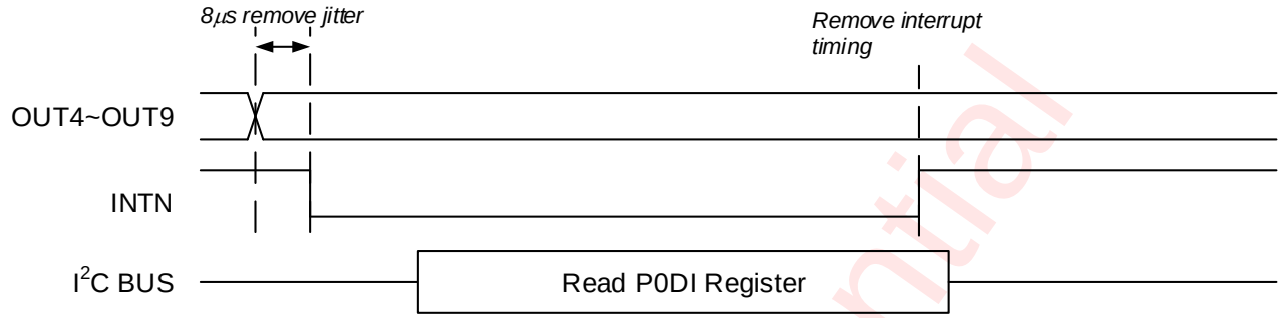
When OUTx is used for GPIO input, AW9110C detects the input state and produces interrupt request. Low level of INTN is active. INTN should be connected to pull-up resistor.

AW9110C has built-in debounce filter. The input state with 8μs low-pass filter will be steady. The interrupt request will not be produced when input state changes in 8μs.

In default status, GPIO interrupt is enabled (P0MSK or P1MSK setting, Table15,16). Only enable interrupt function and configured to GPIO input mode, the interrupt will be produced on INTN.

Clear the interrupt by reading register P0DI, P1DI register. The interrupt of OUT4~OUT9 only be cleared by read P0DI register. The interrupt of OUT0~OUT3 only be cleared by read P1DI register. The interrupts status can't be cleared by the other group.

When AW9110C produces the interrupt request, the interrupt request will be reserved until reading P0DI or P1DI GPIO. The interrupt will be not cleared even if AW9110C switches to GPIO output, or disable GPIO interrupt function.



Once interrupt is generated, P0DI/P1DI registers must be read through I2C read operation separately to clear the interrupt.

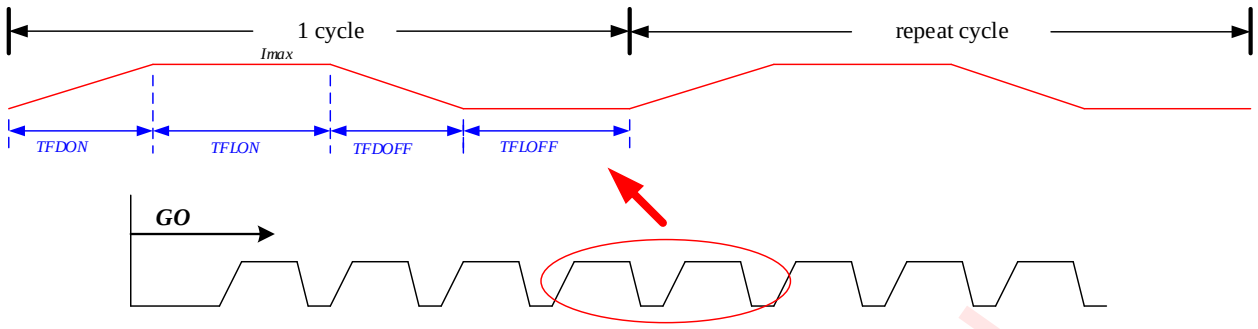
Blink Breathing Mode

OUT0~OUT5 of AW9110C supports BLINK breathing mode. In this mode, AW9110C will complete periodic blink effect automatically until exit the BLINK mode or close breathing function.

1. Configure OUTx to LED driver mode. According to application situation, set register PATEN to enable breathing mode. Set P0DIR/P1DIR (Table 13,14,pay attention to the switch of GPIO and breathing function) to open BLINK function.
2. Configure the timing parameter for BLINK breathing effects:
   - Fade-on process——FDTMR.TFDON (Table 7). The time of fade-on effect has 6 kinds of choice (0ms~5040ms). The fade-on has 64 step dimming level and led turns on gradually from dark.
   - Full-on process——FUTMR.TFLON (Table 8). Full-on state has 8 kinds of choice(0ms~20160ms). the led driving current of this period is decided by GCR[1:0].
   - Fade-off process——FDTMR.TFDOFF (Table 7). The time of fade-off effect has 6 kinds of choice (0ms~5040ms). The fade-off has 64 step dimming level and led turns off gradually from bright.
   - Full-off process——FUTMR.TFLOFF (Table 8). Full-off state has 8 kinds of choice(0ms~20160ms). The led driving current is 0 in this period.
3. After setting blinking parameter, enable GO control bit and the led in BLINK mode starts blink periodically and automatically. It is allowed to enable GO control bit only once. Before re-enabling GO control bit, it demands soft reset or hard reset, which means a reconfiguration of registers.

All ports share the same fade-on/ fade-off/ full-on/ full-off parameter. **None of these parameters can be set to zero. They can not be modified during blinking**.

AW9110C exits BLINK mode by disable P0DIR/P1DIR corresponding bit or disable PATEN setting. The difference is AW9110C will exit BLINK immediately by disable PATEN, but we must wait it complete breathing period by another one.



Smart-Fade Mode

The SMART-FADE mode of AW9110C is semi-automatic breathing, which will simplify 64 steps fade-on and fade-off interface operation into 1bit writing operation: Writing ’1’ means fade-on process and remaining all bright; Writing ’0’ means fade-off process and remaining all dark.

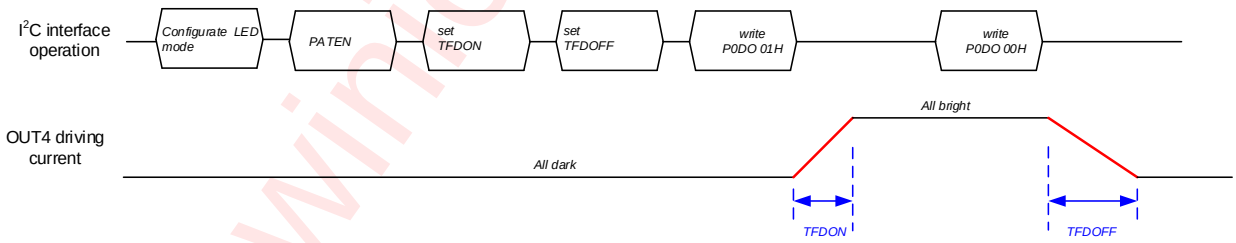
Configure SMART-FADE mode:

1. Set PATEN register and open breathing mode according to the application;
2. Set P0DIR/P1DIR (View table 13,14, pay attention to the switch of GPIO and breathing function), SMART-FADE mode is default;
3. Set P0DO/P1DO bit to complete fade-on or fade-off (View Table 11,12, pay attention to the switch of GPIO and breathing function).

The time of fade-on and fade-off in SMART-FADE mode is controlled by FDTMR. **These parameters must not be all zero and not be modified during fading on or off**.

During fading, it is not allowed to switch fade mode. For example, writing “0” to corresponding P0DO/P1DO is not allowed when fading on. Until reaching the maximum brightness, it is allowed to writing “0” to corresponding P0DO/P1DO.

AW9110C exits SMART-FADE mode by disable PATEN.



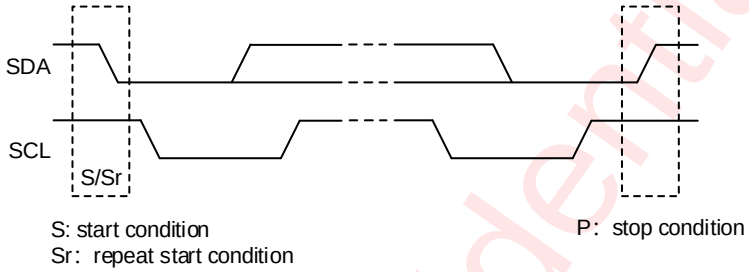
I²C INTERFACE

AW9110C supports the I²C serial bus and data transmission protocol at 400 KHz and 1MHz. AW9110C operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. AW9110C can support different high level (1.8V~3.3V) of this I²C interface.

Start And Stop Condition

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

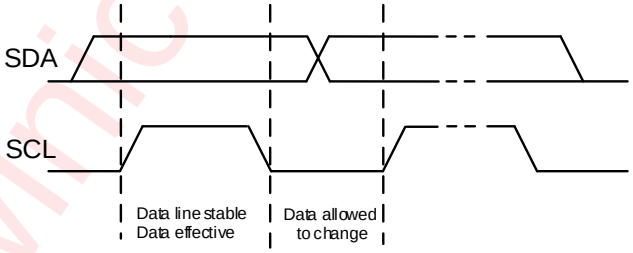


Data Transmission

After the start condition, I²C bus sent an address of slave. AW9110C wait to receive slave address When receiving start condition. If the address from I²C bus is same as the address of AW9110C, the slave pull SDA to acknowledge.

Data Validity

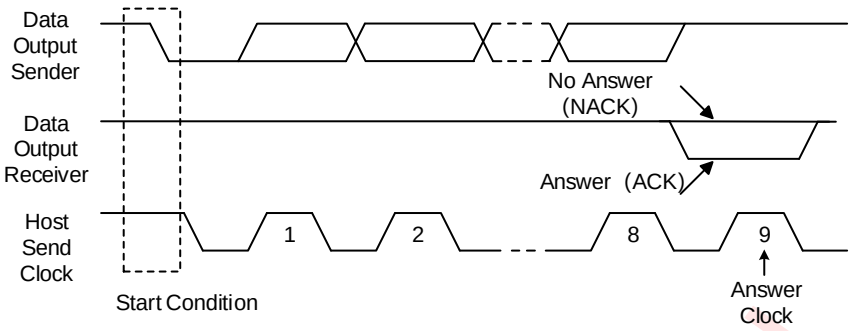
When SCL is in high level, SDA must remain one level stationary .Except start condition and stop condition, SDA level can change just in low level of SCL.



Acknowledge

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is sent and I²C stop is not sent by master, slave device sends the next data. If ACK is not sent by master, slave device stops to send data and waits for I²C stop.



Address

AW9110C supply two address pins AD1,AD0. This allows single I²C bus can use four AW9110C at the same time. The high five bit of slave address is “10110”, the bit2 is AD1, and the bit1 is AD0. The bit0(LSB) is writing and reading flag bit, which define the next operation writing or reading. ‘1’ is read and ‘0’ is write.

1	0	1	1	0	AD1	AD0	R/$\overline{W}$

(The value of AD1 and AD0 is same as AD1 and AD0 PIN)

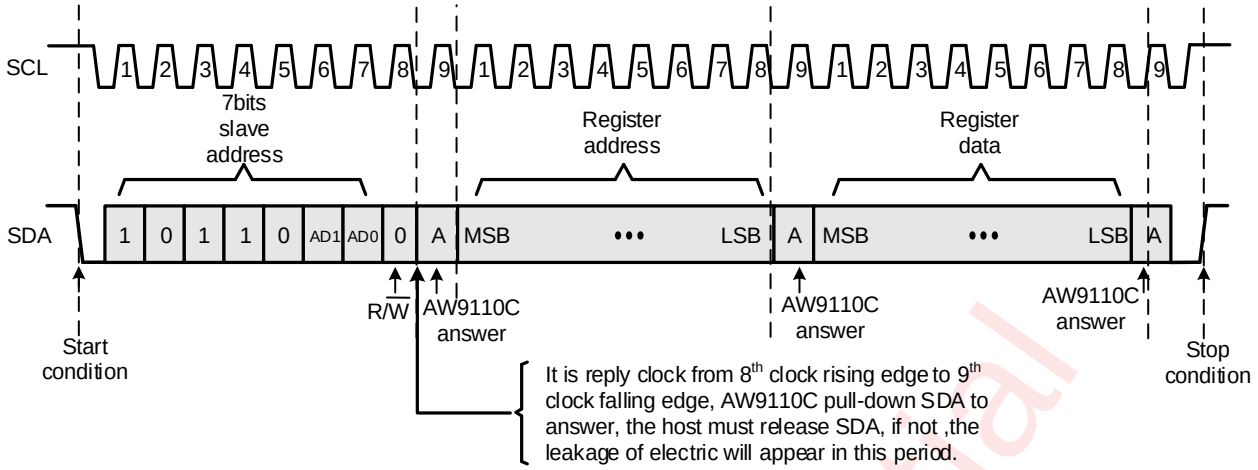
Writing Operation

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock’s high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit firstly. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

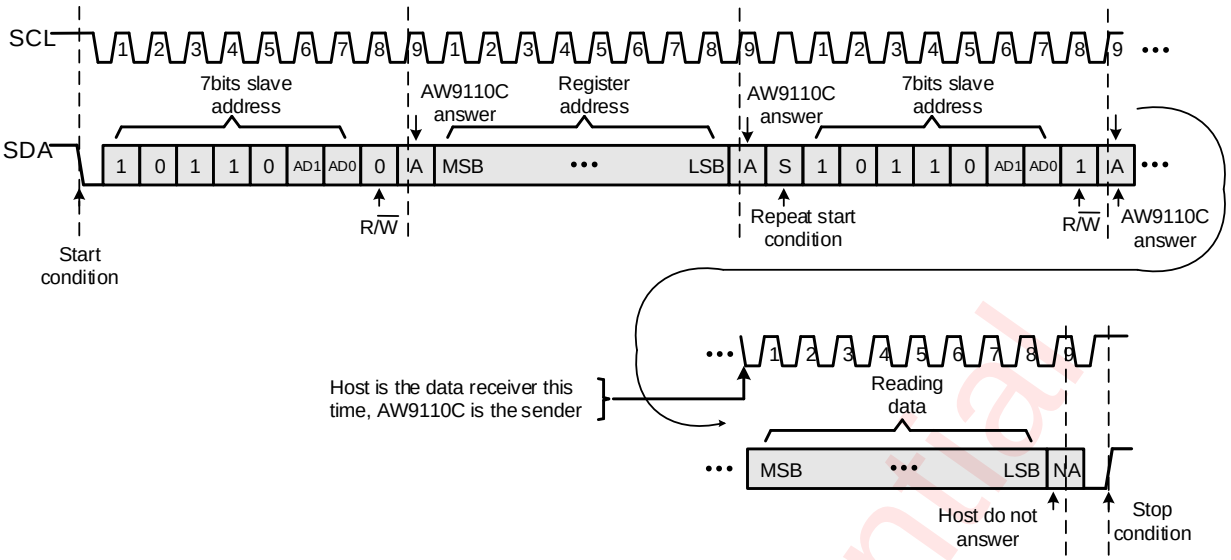
1) Master device generates START condition. The “START” signal is generated by lowering the SDA signal while the SCL signal is high.
2) Master device sends slave address (7-bit) and the data direction bit (w = 0).
3) Slave device sends acknowledge signal if the slave address is correct.
4) Master sends control register address (8-bit)
5) Slave sends acknowledge signal
6) Master sends 8Bit data to be written to the addressed register
7) Slave sends acknowledge signal
8) Master generates STOP condition to indicate write cycle end



Reading Operation

In a read cycle, the following steps should be followed:

1) Master device generates START condition
2) Master device sends slave address (7-bit) and the data direction bit (w = 0).
3) Slave device sends acknowledge signal if the slave address is correct.
4) Master sends control register address (8-bit)
5) Slave sends acknowledge signal
6) Master generates STOP condition followed with START condition or REPEAT START condition
7) Master device sends slave address (7-bit) and the data direction bit (r = 1).
8) Slave device sends acknowledge signal if the slave address is correct.
9) Slave sends 8Bit data from addressed register.
10) Master sends acknowledge signal
11) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register. If master sends no acknowledge signal, the slave device stop to send data and wait for STOP condition.
12) If the master device generates STOP condition, the read cycle is ended.



REGISTER DESCRIPTION

Register Overview

Table 1. AW9110C registers list

Address (HEX)	W/R	Default Value (HEX)	Name	Description
00H	R	xxH	P0DI	OUT4～OUT9 port GPIO input state
01H	R	xxH	P1DI	OUT0～OUT3 port GPIO input state
02H	W/R	Depend on AD1/ AD0	P0DO	OUT4～OUT9 port GPIO output state; In SMART-FADE mode, OUT4~OUT5 can be used for “fade-on” and “fade-off” dimming control.
03H	W/R	Depend on AD1/ AD0	P1DO	OUT0～OUT3 port GPIO output state; In SMART-FADE mode, OUT0~OUT3 can be used for “fade-on” and “fade-off” dimming control.
04H	W/R	00H	P0DIR	OUT4～OUT9 port GPIO input and output direction control; In breathing mode, control OUT4~OUT5 to enter into BLINK mode or SMART-FADE mode.
05H	W/R	00H	P1DIR	OUT0～OUT3 port GPIO input and output direction control; In breathing mode, control OUT0～OUT3 to enter into BLINK mode or SMART-FADE mode.
06H	W/R	00H	P0MSK	OUT4～OUT9 enable interrupt function

07H	W/R	00H	P1MSK	OUT0～OUT3 enable interrupt function
08H~09H	-	-	-	Reserved
10H	R	23H	ID	ID code
11H	W/R	00H	GCR	Global Control
12H	W/R	FFH	P0WKMD	Switch OUT4～OUT9 LED driver mode or GPIO mode
13H	W/R	FFH	P1WKMD	Switch OUT0～OUT3 LED driver mode or GPIO mode
14H	W/R	00H	PATEN	Enable LED breathing mode
15H	W/R	00H	FDTMR	In BLINK or SMART-FADE mode, LED “fade-on” or “fade-off” time parameter
16H	W/R	00H	FLTMR	In BLINK mode, LED light all on or all off time parameter
17H~1FH	-	-	-	Reserved
20H	W	00H	DIM0	OUT0 port 256 steps dimming control
21H	W	00H	DIM1	OUT1 port 256 steps dimming control
22H	W	00H	DIM2	OUT2 port 256 steps dimming control
23H	W	00H	DIM3	OUT3 port 256 steps dimming control
24H	W	00H	DIM4	OUT4 port 256 steps dimming control
25H	W	00H	DIM5	OUT5 port 256 steps dimming control
26H	W	00H	DIM6	OUT6 port 256 steps dimming control
27H	W	00H	DIM7	OUT7 port 256 steps dimming control
28H	W	00H	DIM8	OUT8 port 256 steps dimming control
29H	W	00H	DIM9	OUT9 port 256 steps dimming control
2AH~7EH	-	-	-	Reserve
7FH	W/R	03H	RESET	Write 00H,reset by software, 03H is read as device ID.

Register Detail

Table 2. DIM0~DIM5(20H~29H),256 steps dimming configuration register

Bit	Symbol	Description	Default
D[7:0]	DIM	256 steps dimming level choice 20H~29H corresponding to OUT0~OUT9 dimmer instruction; D[7:0] code from 0 to 255 corresponding to the current 0~I_{MAX}	00H

Table 3. GCR(11H),Global control register

Bit	Symbol	Description	Default
D7	GO	Writing 1 to enable breathing in BLINK mode.	0
D[6:5]	-	-	Remain
D4	GPMD0	OUT4～OUT9 driver option in GPIO mode 0：OPEN-DRAIN 1：PUSH-PULL	0
D[3:2]	-	-	Remain
D[1:0]	GCC	256 dimming range option 00：0～I_{MAX4} 01：0～I_{MAX3} 10：0～I_{MAX2} 11：0～I_{MAX1}	00

Table 4. P0WKMD(12H), GPIO control switch to LED driver register

Bit	Symbol	Description	Default
D[7:6]	-	-	Remain
D5	P0WKMD[5]	OUT9 mode control 0：LED mode 1：GPIO mode	1
D4	P0WKMD[4]	OUT8 mode control 0：LED mode 1：GPIO mode	1
D3	P0WKMD[3]	OUT7 mode control 0：LED mode 1：GPIO mode	1
D2	P0WKMD[2]	OUT6 mode control 0：LED mode 1：GPIO mode	1
D1	P0WKMD[1]	OUT5 mode control 0：LED mode 1：GPIO mode	1
D0	P0WKMD[0]	OUT4 mode control	1

		0：LED mode 1：GPIO mode	

Table 5. P1WKMD(13H), GPIO control switch to LED driver register

Bit	Symbol	Description	Default
D[7:4]	-	-	Remain
D3	P1WKMD[3]	OUT3 mode control 0：LED mode 1：GPIO mode	1
D2	P1WKMD[2]	OUT2 mode control 0：LED mode 1：GPIO mode	1
D1	P1WKMD[1]	OUT1 mode control 0：LED mode 1：GPIO mode	1
D0	P1WKMD[0]	OUT0 mode control 0：LED mode 1：GPIO mode	1

Table 6. PATEN(14H), Enable Breathing REGISTER

Bit	Symbol	Description	Default
D[7:6]	-	-	Remain
D5	PATEN[5]	OUT5 enable breath mode 0：disable 1：enable	0
D4	PATEN[4]	OUT4 enable breath mode 0：disable 1：enable	0
D3	PATEN[3]	OUT3 enable breath mode 0：disable 1：enable	0
D2	PATEN[2]	OUT2 enable breath mode 0：disable	0

		1：enable	
D1	PATEN[1]	OUT1 enable breath mode 0：disable 1：enable	0
D0	PATEN[0]	OUT0 enable breath mode 0：disable 1：enable	0

Table 7. FDTMR(15H),Fade-on or fade-off time setting register in BLINK or SMART-FADE

Bit	Symbol	Description	Default
D[7:6]	-	-	Remain
D[5:3]	TFDOFF	Fade-off time setting 001：315ms 010：630ms 011：1260ms 100：2520ms 101：5040ms others：Must not be configured	000
D[2:0]	TFDON	Fade-on time setting 001：315ms 010：630ms 011：1260ms 100：2520ms 101：5040ms others：Must not be configured	000

Table 8. FULL_TMR(16H),All-on or all-off time setting register in BLINK mode.

Bit	Symbol	Description	Default
D[7:6]	-	-	Remain
D[5:3]	TFLOFF	All-off time setting 001：315ms 010：630ms 011：1260ms 100：2520ms 101：5040ms	000

		others：Must not be configured	
D[2:0]	TFLON	All-on time setting 001：315ms 010：630ms 011：1260ms 100：2520ms 101：5040ms others：Must not be configured	000

Table 9. P0DI(00H),GPIO input state register

Bit	Symbol	Description	Default
D[7:6]	-	-	Remain
D5	P0DI[5]	OUT9 pin state 0：Low level 1：High level	x
D4	P0DI[4]	OUT8 pin state 0：Low level 1：High level	x
D3	P0DI[3]	OUT7 pin state 0：Low level 1：High level	x
D2	P0DI[2]	OUT6 pin state 0：Low level 1：High level	x
D1	P0DI[1]	OUT5 pin state 0：Low level 1：High level	x
D0	P0DI[0]	OUT4 pin state 0：Low level 1：High level	x

Table 10. P1DI(01H),GPIO input state register

Bit	Symbol	Description	Default

D[7:4]	-	-	Remain
D3	P1DI[3]	OUT3 pin state 0：Low level 1：High level	x
D2	P1DI[2]	OUT2 pin state 0：Low level 1：High level	x
D1	P1DI[1]	OUT1 pin state 0：Low level 1：High level	x
D0	P1DI[0]	OUT0 pin state 0：Low level 1：High level	x

Table 11. P0DO(02H),GPIO output state register or as driver control in SMART-FADE mode

Bit	Symbol	Description	Default
D[7:6]	-	-	Remain
D5	P0DO[5]	OUT9 pin state 0：Low level 1：High level	Depend on AD0 and AD1
D4	P0DO[4]	OUT8 pin state 0：Low level 1：High level	
D3	P0DO[3]	OUT7 pin state 0：Low level 1：High level	
D2	P0DO[2]	OUT6 pin state 0：Low level 1：High level	
D1	P0DO[1]	P0WKMD[1]=1,as driving OUT5 pin state 0：Low level 1：High level P0WKMD[0]=0 & PATEN[5]=1, OUT5 in SMART-FADE mode	

		0->1：fade-on 1->0：fade-off	
D0	P0DO[0]	P0WKMD[0]=1,as driving OUT4 pin state 0：Low level 1：High level P0WKMD[0]=0 & PATEN[4]=1, OUT4 in SMART-FADE mode 0->1：fade-on 1->0：fade-off	

Table 12. P1DO(03H),GPIO output state register or as driver control in SMART-FADE mode

Bit	Symbol	Description	Default
D[7:4]	-	-	Remain
D3	P1DO[3]	P1WKMD[3]=1,as driving OUT3 pin state 0：Low level 1：High level P1WKMD[3]=0 &PATEN[3]=1,OUT3 in SMART-FADE mode 0->1：fade-on 1->0：fade-off	Depend on AD0 and AD1
D2	P1DO[2]	P1WKMD[2]=1,as driving OUT2 pin state 0：Low level 1：High level P1WKMD[2]=0 &PATEN[2]=1,OUT2 in SMART-FADE mode 0->1：fade-on 1->0：fade-off	
D1	P1DO[1]	P1WKMD[1]=1,as driving OUT1 pin state 0：Low level 1：High level P1WKMD[1]=0 &PATEN[1]=1,OUT1 in SMART-FADE mode 0->1：fade-on 1->0：fade-off	
D0	P1DO[0]	P1WKMD[0]=1,as driving OUT0 pin state 0：Low level 1：High level P1WKMD[0]=0 &PATEN[0]=1,OUT0 in SMART-FADE mode	

		0->1：fade-on 1->0：fade-off	

Table 13. P0DIR(04H),GPIO input or output select register or as BLINK,SMART-FADE Mode select

Bit	Symbol	Description	Default
D[7:6]	-	-	Remain
D5	P0DIR[5]	OUT9 input or output choice 0：output 1：input	0
D4	P0DIR[4]	OUT8 input or output choice 0：output 1：input	0
D3	P0DIR[3]	OUT7 input or output choice 0：output 1：input	0
D2	P0DIR[2]	OUT6 input or output choice 0：output 1：input	0
D1	P0DIR[1]	P0WKMD[1]=1, OUT5 input or output choice 0：output 1：input P0WKMD[1] =0 & PATEN[5]=1, OUT5 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	0
D0	P0DIR[0]	P0WKMD[0] =1, OUT4 input or output choice 0：output 1：input P0WKMD[0] =0 & PATEN[4]=1, OUT4 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	0

Table 14. P1DIR(05H),GPIO input or output selection register, or used for BLINK,SMART-FADE mode choice

Bit	Symbol	Description	Default
D[7:4]	-	-	Remain
D3	P1DIR[3]	P0WKMD[3] =1 , OUT3 input or output choice 0：output 1：input P0WKMD[3]=0 & PATEN[3]=1, OUT3 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	0
D2	P1DIR[2]	P0WKMD[2] =1 , OUT2 input or output choice 0：output 1：input P0WKMD[2]=0 & PATEN[2]=1, OUT2 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	0
D1	P1DIR[1]	P0WKMD[1] =1 , OUT1 input or output choice 0：output 1：input P0WKMD[1]=0 & PATEN[1]=1, OUT1 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	0
D0	P1DIR[0]	P0WKMD[0] =1 , OUT0 input or output choice 0：output 1：input P0WKMD[0]=0 & PATEN[0]=1, OUT0 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	0

Table 15. P0MSK(06H),GPIO Mask Interrupt Register

Bit	Symbol	Description	Default
D[7:2]	-	-	Remain
D5	P0MSK[5]	OUT9 enable interrupt 0：enable	0

		1：disable	
D4	P0MSK[4]	OUT8 enable interrupt 0：enable 1：disable	0
D3	P0MSK[3]	OUT7 enable interrupt 0：enable 1：disable	0
D2	P0MSK[2]	OUT6 enable interrupt 0：enable 1：disable	0
D1	P0MSK[1]	OUT5 enable interrupt 0：enable 1：disable	0
D0	P0MSK[0]	OUT4 enable interrupt 0：enable 1：disable	0

Table 16. P1MSK (07H),GPIO Mask Interrupt Register

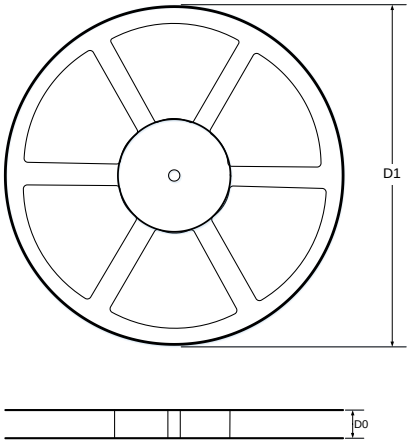
Bit	Symbol	Description	Default
D[7:4]	-	-	Remain
D3	P1MSK[3]	OUT3 enable interrupt 0：enable 1：disable	0
D2	P1MSK[2]	OUT2 enable interrupt 0：enable 1：disable	0
D1	P1MSK[1]	OUT1 enable interrupt 0：enable 1：disable	0
D0	P1MSK[0]	OUT0 enable interrupt 0：enable 1：disable	0

Table 17. RESETN(7FH), Software Reset Register

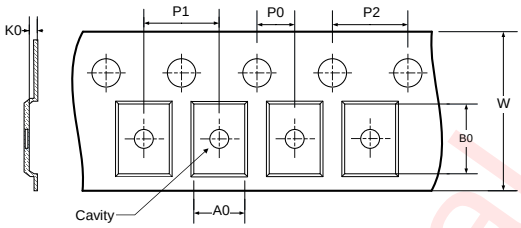
Bit	Symbol	Description	Default
D[7:0]	RESETN	Write 00H,reset by software 03H is read as chip ID	03H

TAPE AND REEL INFORMATION

REEL DIMENSIONS

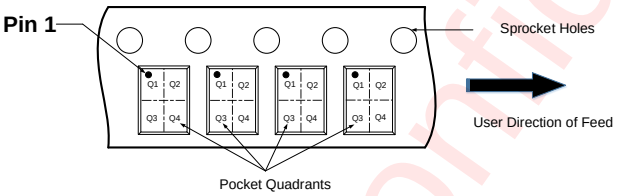


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



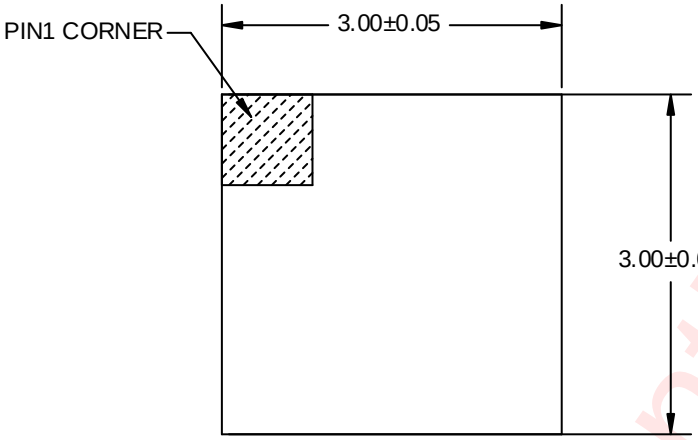
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

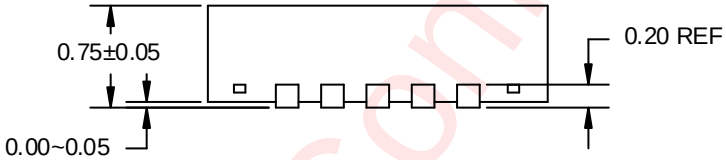
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	3.3	3.3	1.1	2	8	4	12	Q1

All dimensions are nominal

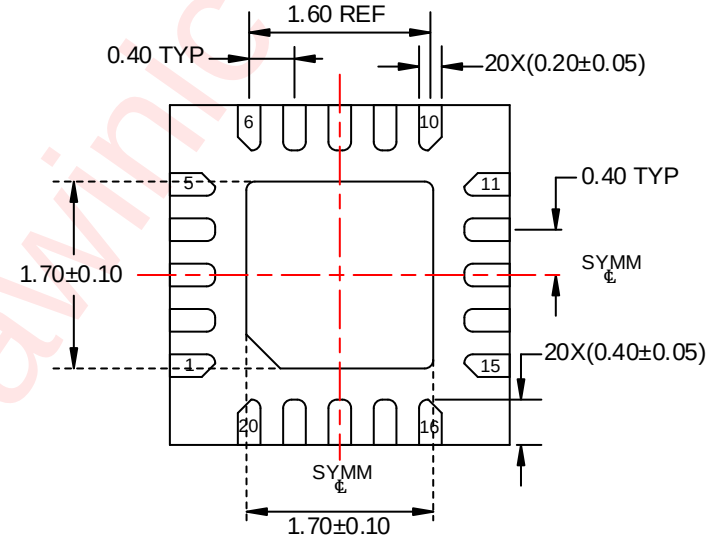
PACKAGE DESCRIPTION



TOP VIEW



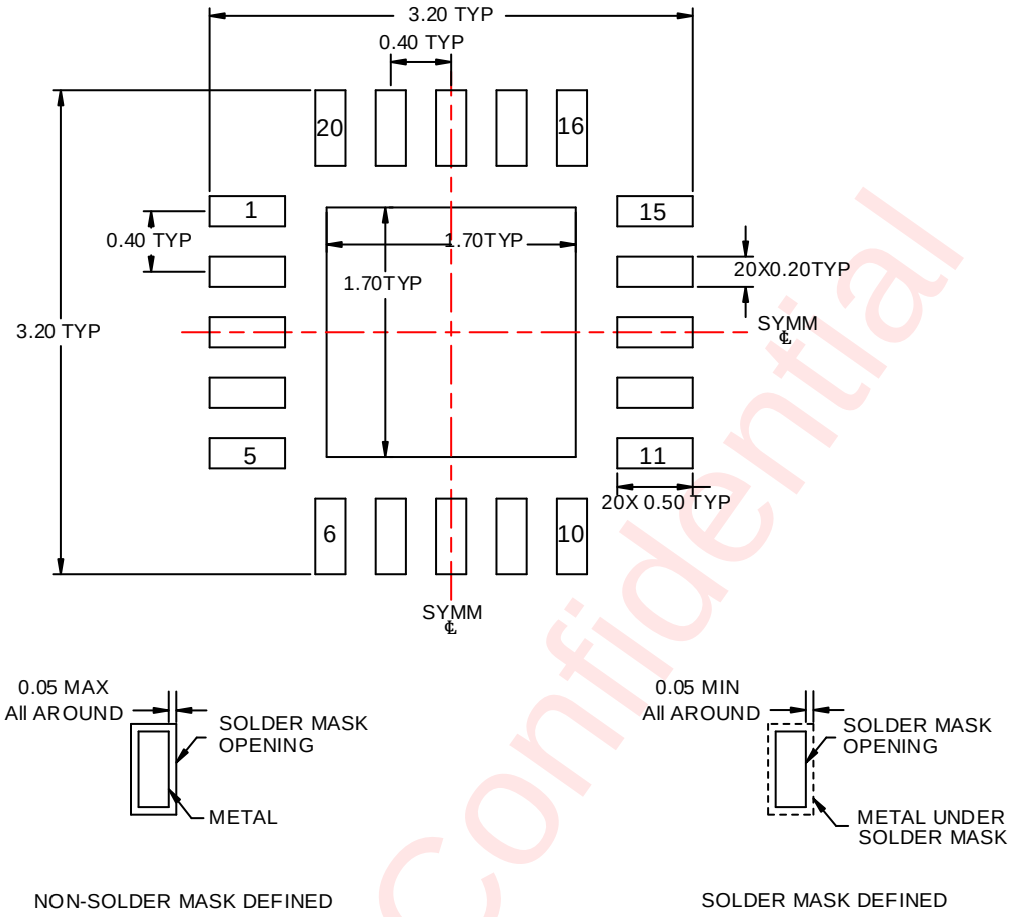
SIDE VIEW



BOTTOM VIEW

Unit：mm

RECOMMENDED LAND PATTERN



Unit: mm

REVISION HISTORY

Version	Date	Revision Record
V1.0	May 2021	First officially release
V1.1	Nov 2021	Correct GCC Register
V1.2	May 2022	1. Modified the way of clear INTERRUPT 2. Modified Register Detail of *FDTMR* and *FULL_TMR*
V1.3	Sep 2022	Correct POD
V1.4	Dec 2023	1 Delete typical application images ---P4 2 Delete REFLOW ---P30 3 package description changed ---P1 and P4 4 correct the mode test condition ---P5
V1.5	Mar 2024	1 Correct the Imax of LED driver ---P5

DISCLAIMER

Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.
All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.