

DPDT USB Switch With Over Voltage Protection

Features

- USB 2.0 Hi-speed DPDT switch
- Typical -3dB bandwidth: 1.0 GHz
- Over voltage protection : 4.8V typical
- 20V DC protection on D+ and D- Ports
- +25V surge protection on D+ and D-
- Supply voltage range: 2.7V to 5.5V
- 5Ω switch on-resistance typical
- C_{ON}: 6pF typical
- I_{CC}: 35μA typical
- WLCSP 1.57mmX1.17mmX0.574mm-12B package

Applications

- Smartphones
- Tablets

General Description

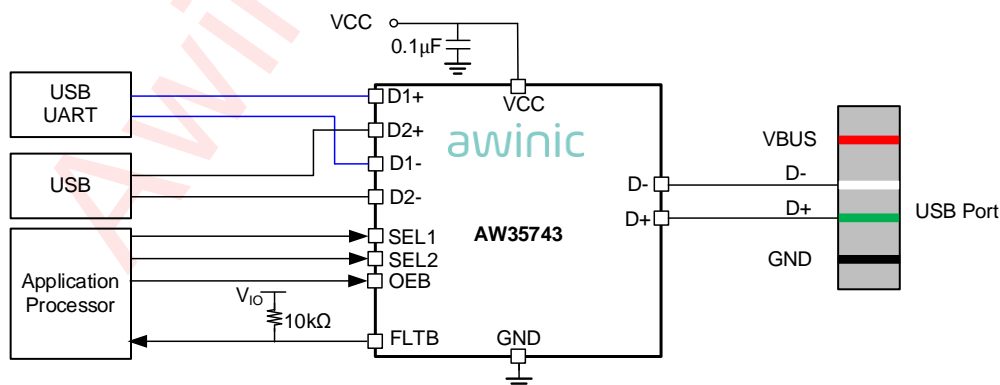
The AW35743 is a Hi-Speed USB 2.0(480Mbps) DPDT (Double Pole Double Throw) switch with integrated protection for USB D+ and D-, it can be configured as a dual 1:2 or 2:1 switch.

The AW35743 protection on the D+/D- pins can tolerate up to 20V DC, when D+ or D- voltage is greater than the OVP(Over-Voltage Protection) threshold, the switch will be automatically shutoff to protect downstream devices.

The device operates over 2.7V to 5.5V supply range with independent control bits for each switch pair and an on/off enable pin for shutdown mode. Additional features include low switch on resistance and capacitance along with a fault flag to alert the system processor to overvoltage fault events.

The AW35743 is available in a WLCSP 1.57mmX1.17mmX0.574mm-12B package.

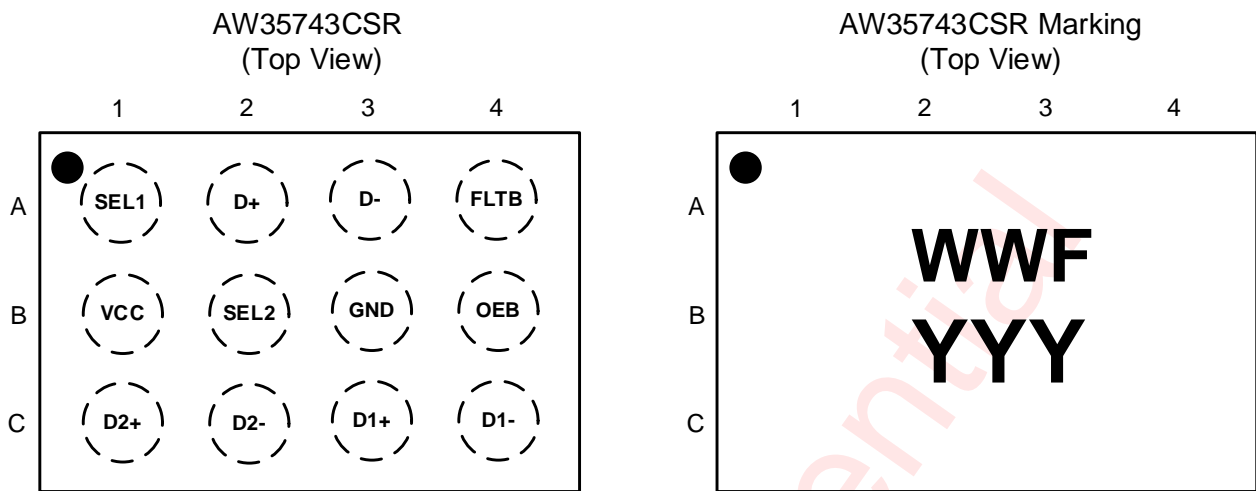
Typical Application Circuit



Typical Application Circuit of AW35743

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Pin Configuration And Top Mark



WWF – AW35743CSR
YYY – Production Tracing Code

Pin Configuration And Top Mark

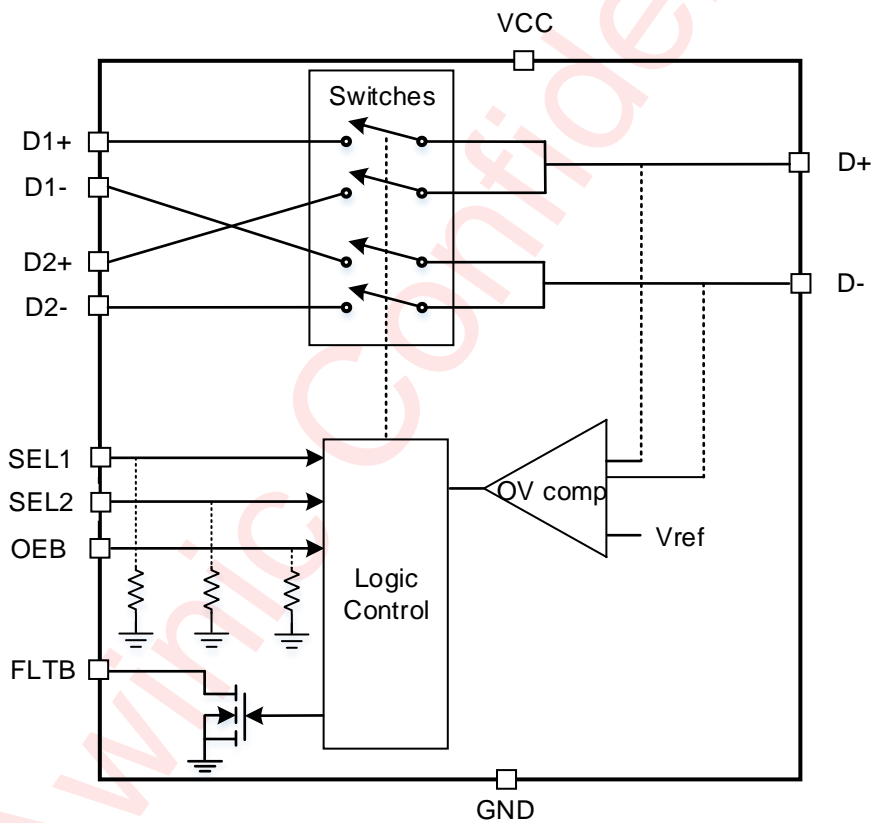
Pin Definition

PIN	NAME	DESCRIPTION
A1	SEL1	Switch select1, active high
A2	D+	Common high speed data port, differential +
A3	D-	Common high speed data port, differential -
A4	FLTB	Fault indicator output, active low, open drain
B1	VCC	Supply voltage
B2	SEL2	Switch select2, active high
B3	GND	Ground
B4	OEB	Output enable, active low
C1	D2+	Multiplexed high speed data port2, differential +
C2	D2-	Multiplexed high speed data port2, differential -
C3	D1+	Multiplexed high speed data port1, differential +
C4	D1-	Multiplexed high speed data port1, differential -

Pin Functions

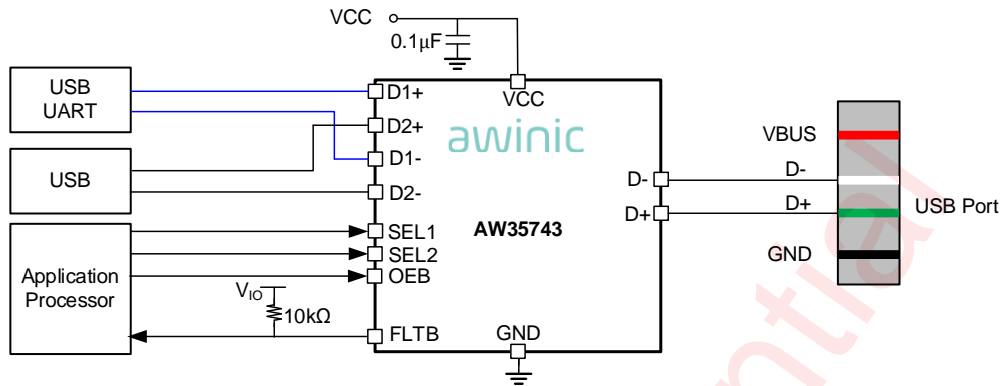
OEB	SEL1	SEL2	D- CONNECTION	D+ CONNECTION
H	X	X	High-Z	High-Z
L	L	L	D- to D1-	D+ to D1+
L	L	H	D- to D1-	D+ to D2+
L	H	L	D- to D2-	D+ to D1+
L	H	H	D- to D2-	D+ to D2+

Functional Block Diagram



Functional Block Diagram

Typical Application Circuits



Typical Application Circuit of AW35743

Notice for Typical Application Circuits:

1. The AW35743 has internal 7-MΩ pull down resistors on SEL1, SEL2, and OEB, so no external resistors are required on the logic pins.
2. Internal pull-down resistor on SEL1 and SEL2 pins ensures the D1+ and D1- channels are selected by default.
3. If FLTB is not used, it can be left floating.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW35743CSR	-40°C~85°C	WLCSP 1.57mmX1.17mm X0.574mm-12B	WWF	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage range VCC		-0.3V to 6V
Input/Output DC voltage(D+, D-)		-0.3V to 20V
Input/Output DC voltage(D1+, D1-, D2+, D2-)		-0.3V to 6V
Input voltage range	SEL1, SEL2, OEB	-0.3V to 6V
Output voltage range	FLT B	-0.3V to 6V
Junction-to-ambient thermal resistance θ_{JA}		95°C/W
Maximum operating junction temperature T_{JMAX}		150°C
Operating free-air temperature range		-40°C to 85°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD		
Human Body Model (All pins, per ESDA/JEDEC JS-001)		±2kV
Charged Device Model (All pins, per ESDA/JEDEC JS-002)		±1kV
Latch-Up		
Test condition: JESD78E		±200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

Electrical Characteristics

T_A = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V_{CC}=3.3V T_A = 25°C.

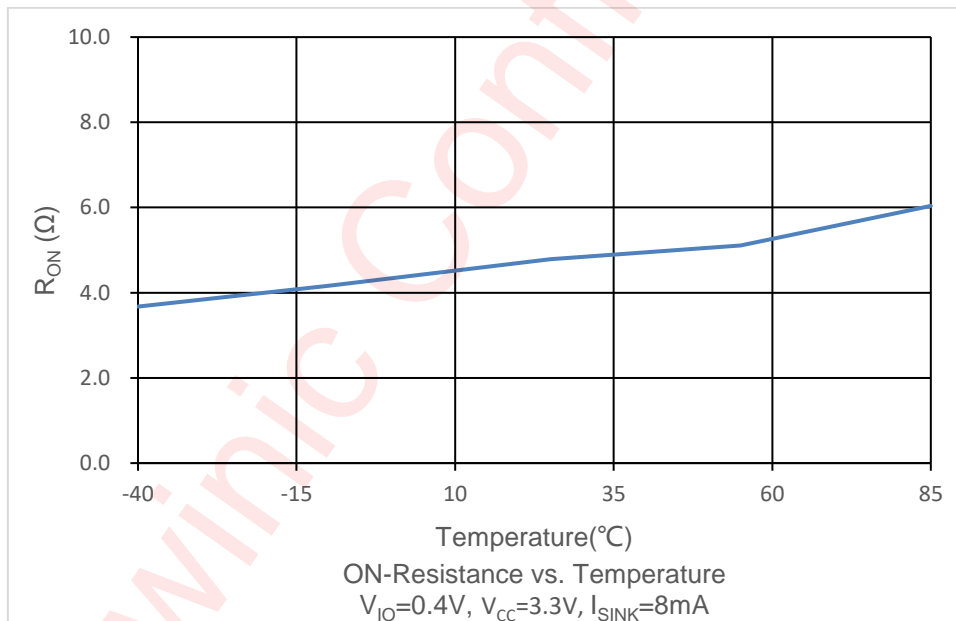
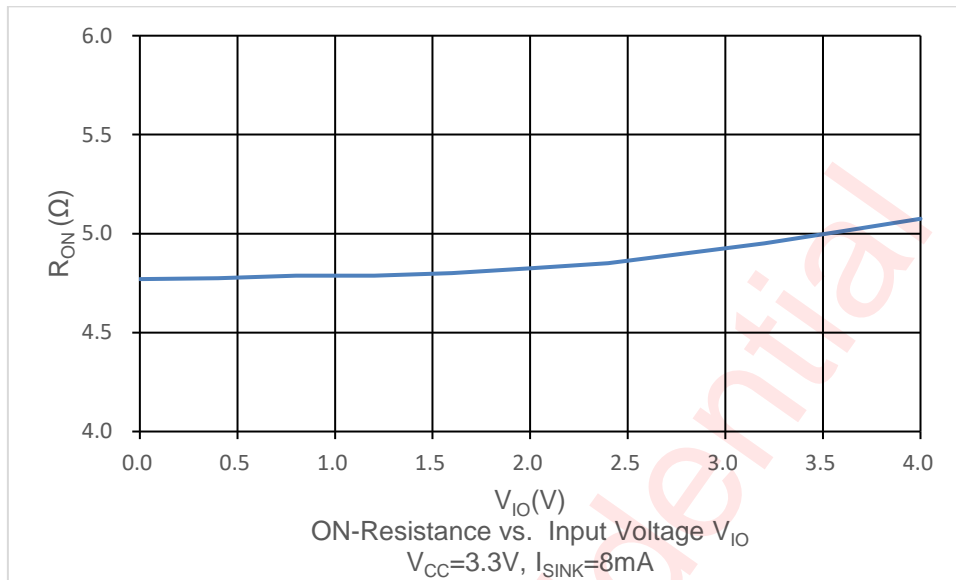
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V _{CC}	Supply voltage		2.7	3.3	5.5	V
I _{CC}	Active supply current	OEB=0V SEL1, SEL2=0V 0V < V _{D±} < 3.6V		35	50	μA
I _{CC_PD}	Standby supply current	OEB= V _{CC} SEL1, SEL2=0V		0.5		μA
DC Characteristics						
R _{ON}	On-state resistance	V _{I/O} =0.4V, I _{SINK} =8mA		5		Ω
ΔR _{ON}	On-state resistance match between channels	V _{I/O} =0.4V, I _{SINK} =8mA		0.1		Ω
R _{ON(FLAT)}	ON-state resistance flatness	V _{I/O} =0V to 0.4V, I _{SINK} =8mA		0.1		Ω
I _{OFF}	I/O pin OFF leakage current on D+/D-	V _{D±} = 0 V or 3.6 V V _{D1±} or V _{D2±} = 3.6 V or 0 V			10	μA
I _{ON}	ON leakage current on D+/D-	V _{D±} = 0 V or 3.6 V V _{D1±} and V _{D2±} = high-Z		2	10	μA
Digital Characteristics						
V _{IH}	Input logic high	SEL1, SEL2, OEB	1.4		V _{CC}	V
V _{IL}	Input logic low	SEL1, SEL2, OEB			0.4	V
V _{OL}	Output logic low	FLTB I _{OL} = 1 mA			0.5	V
R _{PD}	Internal pull-down resistor on digital input pins			7		MΩ
Protection						
V _{OVP_TH}	OVP threshold	D+/D- rising	4.4	4.8	5.4	V
V _{OVP_HYST}	OVP threshold hysteresis			60		mV
V _{CLAMP_V}	Clamping voltage on D _{1±} and D _{2±} pins during surge	8/20 μs surge test, OEB=0V, R _L = open			9	V
t _{CLAMP}	Clamp time during OVP	8/20 μs surge test, OEB=0V, R _L = open		2	5	μs

Electrical Characteristics (Continued)

T_A = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V_{CC}=3.3V T_A = 25°C.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Dynamic Characteristics					
C _{ON}	IO pins ON capacitance	V _{D±} = 0 or 3.3 V, f = 240 MHz, switch ON		6	pF
O _{ISO}	Differential off isolation	R _L = 50 Ω C _L = 5 pF f = 100 kHz, switch OFF		-60	dB
		R _L = 50 Ω C _L = 5 pF f = 240MHz, switch OFF		-20	dB
X _{TALK}	Channel to channel crosstalk	R _L = 50 Ω C _L = 5 pF f = 100 kHz, switch ON		-60	dB
BW	-3dB bandwidth	R _L = 50 Ω, switch ON		1.0	GHz
t _{switch}	Switching time between channels (SEL1, SEL2 to output)	V _{D±} = 0.8 V R _L = 50 Ω		1.5	5 μs
t _{on}	Device turn on time (OEB to output)	C _L = 5 pF, V _{CC} = 2.7 V to 5.5 V		15	μs
t _{off}	Device turn off time (OEB to output)			1.5	μs
t _{pd}	Propagation delay	V _{D±} = 0.4 V R _L = 50 Ω, C _L = 5 pF, V _{CC} = 2.7 V to 5.5 V		200	ps

Typical Characteristics



Detailed Functional Description

The AW35743 is a Hi-Speed USB 2.0 DPDT switch with integrated protection for USB D+ and D-, it can be configured as a dual 1:2 or 2:1 switch. The AW35743 will protect D+ and D- pins when stressed with voltages up to 20V. The device can pass signals with bandwidth 1GHz to maintain signal integrity and eye compliance.

Over-Voltage Protection

AW35743 is designed to protect the system from damage. Over-voltage event happens when voltage on D+/D- exceeds 4.8V(typ.), and device will activate OVP to disconnect the switches, the FLTB will also be pulled low to indicate there is OV event to the system.

High Impedance Mode

When OEB is logic high, the AW35743 is in high impedance mode, all the signal paths are in Hi-Z state.

OEB	SEL1	SEL2	D- Connection	D+ Connection
H	X	X	High-Z	High-Z
L	L	L	D- to D1-	D+ to D1+
L	L	H	D- to D1-	D+ to D2+
L	H	L	D- to D2-	D+ to D1+
L	H	H	D- to D2-	D+ to D2+

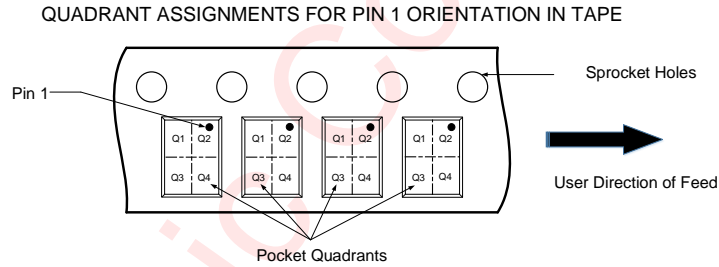
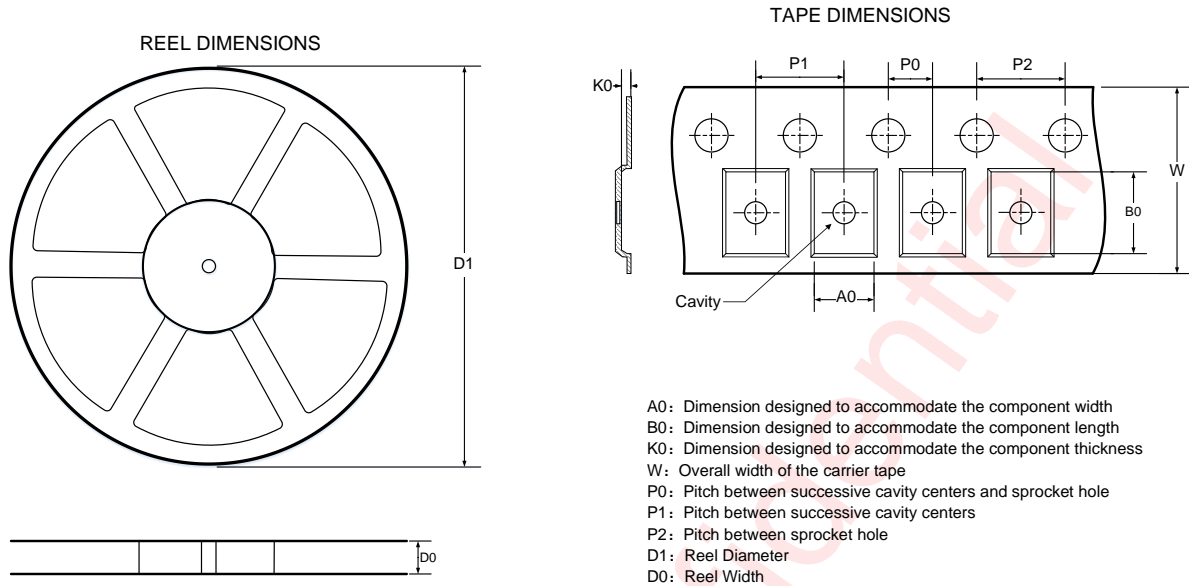
PCB Layout Consideration

To obtain the optimal performance of AW35743, PCB layout should be considered carefully. Here are some guidelines:

1. Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass capacitors near the D+/D- traces.
2. The differential characteristic impedance of D+ and D- traces is suggested to be 90Ω , and it's better to shield D+ and D- traces by ground planes.
3. Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes.
4. Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
5. Avoid stubs on the high-speed USB signals because they cause signal reflections.
6. Route all high-speed USB signal traces over continuous GND planes, with no interruptions.

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Tape And Reel Information

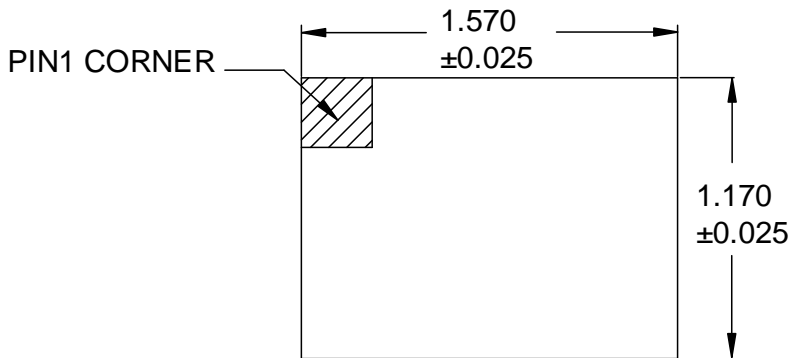


Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

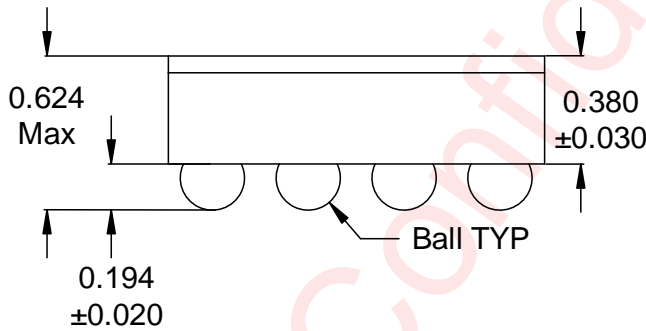
All dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00±2	9.00±2	1.29±0.06	1.69±0.06	0.73±0.05	2.00±0.05	4.00±0.1	4.00±0.1	8.00 (+0.03-0.01)	Q2

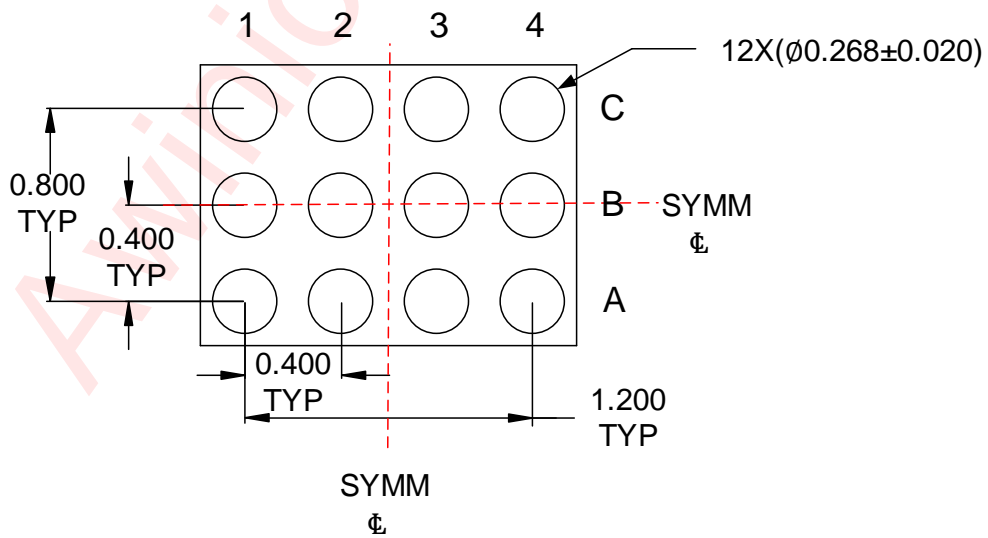
Package Description



Top View



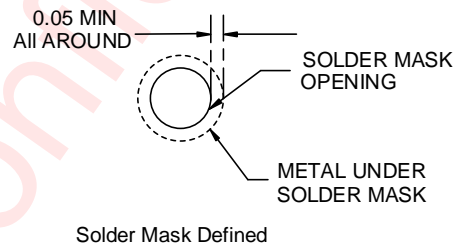
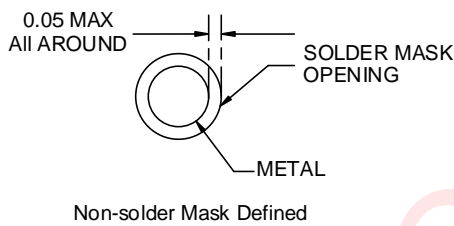
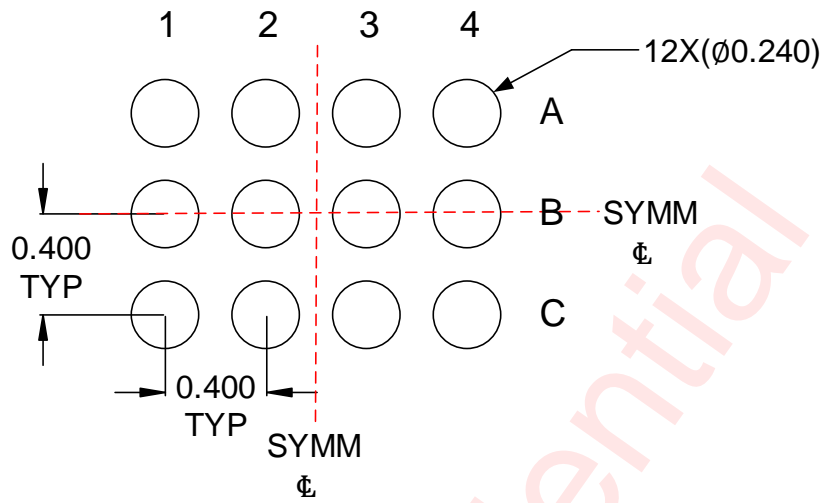
Side View



Bottom View

Unit: mm

Land Pattern Data



Unit: mm

Revision History

Version	Date	Change Record
V1.0	Feb 2019	Datasheet V1.0 released
V1.1	Sept 2019	Update Description of feature(P1)
V1.2	Mar 2020	Update Description of typical values from(P1,P4)
V1.3	May 2020	Update DC Voltage of D+ and D-(P1,P5,P9)
V1.4	May 2024	Update Tape And Reel Information(P11) and Package Description(P12)

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