MCP1081S

Ten Channel Multi-Mode Wideband Digital Capacitive Processor Sensor

1. Overview

MCP1081S (Mysentech Capacitive Processor) is a new generation of capacitive sensing microprocessor SOC chip launched by Minyuan Sensing, which integrates ten channel, multi-mode, wideband capacitive analog front-end sensing circuit, microprocessor, storage, and rich I/O interfaces. The capacitance measurement frequency can be configured within the range of 0.1~30MHz, and the output is a 16 bit digital signal with a maximum resolution of 1fF. The chip supports various operating modes, enabling the measurement of single-ended capacitance, dual-ended capacitance, and mutual capacitance. The chip integrates a 16 bit high-precision digital temperature sensor, which can be used in scenarios that require temperature compensation and other temperature composite sensing.

To address the requirements of embedded capacitive sensing processing across various industries, the SOC chip integrates a microprocessor based on the Arm® Cortex®-M0 core, which enables edge computing of various sensing algorithms. It converts the raw measured oscillation frequency values into capacitance values and specific physical quantities including liquid level, moisture content, displacement, and proximity distance. The chip is equipped with 16KB Flash memory and 2KB SRAM, allowing developers to write application software and store sensor calibration and application data. The chip integrates hardware resources such as ADC, advanced timer, universal timer, 16 bit basic timer, as well as interfaces such as USART and I2C.

2. Features

- Capacitance detection front-end
  - Measurement of 10 single-ended capacitance and 5 dual-ended capacitance
  - Capacitance measurement range: 1pF~10nF
  - Capacitance detection frequency: 100KHz~30MHz
  - Capacitance or frequency resolution: 16 bits
  - Supports active shielding and adjacent mutual capacitance measurement
- Kernel and System
  - 32-bit Arm ® Cortex ®- M0

  The working frequency can reach 48MHz
- Memory
  - 16KB Flash memory
  - 2KB SRAM
- Clock, reset, and power management
  - 2.3V~5.5V power supply

  Power on/off reset (POR/PDR), programmable voltage monitor (PVD)
  - Embedded 48MHz HSI high-speed oscillator
  - Embedded 40KHz LSI low-speed oscillator
- low power consumption
  - Supports low-power modes, including Sleep and Deep Sleep
  - Average power consumption: 12uA@1Hz
- Five timers

  -One 16 bit 4-channel advanced control timer (TIM1)

  -One 16 bit 4-channel universal timer (TIM3)

  -One 16 bit basic timer (TIM14)

  One independent clock hardware

watchdog timer (IWDG)
-One Systick timer: 24 bit self decreasing counter

- Nine fast I/O ports
  - All I/O ports can be mapped to external interrupts
  - All ports are capable of inputting and outputting signals with a voltage not exceeding VDD
- Three communication interfaces
  - Two USART interfaces
  - One I2C interface
- One 12 bits analog-to-digital converter (ADC), supporting a conversion time of up to 1 μ s (1MSPS sampling rate), configured with 4 external channels and 1 internal channel capable of collecting built-in reference voltage
- CRC calculation unit
- 96 bits chip unique ID (UID)
- Debugging Mode - Serial Debugging Interface (SWD) Interface
- Working temperature range -40 ℃ ~+85 ℃
- Single channel conversion time: configurable from 0.1ms to 23.5ms
- Built in 16 bit high-precision digital temperature measurement

3. Applications

- Liquid level measurement
- Moisture content measurement
- Dry-Wet analysis
- Water immersion sensing
- Dielectric Detection
- Proximity sensing
- Touch button

Product Information

Part Number	Package	Dimensions
MCP1081S	QFN24	4.0*4.0*0.75mm

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4. Package Pin Description and Reuse Function

4.1 MCP1081S Package Pin Diagram (QFN24)

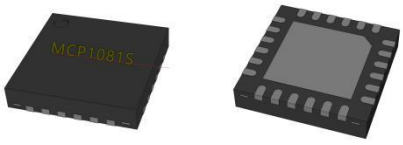


Table 4.1 MCP1081S Pin Definition

QFN24	Name	Type(1)	I/O level(2)	Main function	Multiplex function	Additional function
1	PA1/U2TX	I/O	TC	PA1	USART1_SCK USART2_TX I2C1_SDA	-
2	VDD	P	-	Power	-	-
3	GNDA	G	-	Analog Ground	-	-
4	C9	A	-	Channel 9 capacitor input	-	-
5	C8	A	-	Channel 8 capacitor input	-	-
6	C7	A	-	Channel 7 capacitor input	-	-
7	C6	A	-	Channel 6 capacitor input	-	-
8	C5	A	-	Channel 5 capacitor input	-	-
9	C4	A	-	Channel 4 capacitor input	-	-
10	C3	A	-	Channel 3 capacitor input	-	-
11	C2	A	-	Channel 2 capacitor input	-	-
12	C1	A	-	Channel 1 capacitor input	-	-
13	C0	A	-	Channel 0 capacitor input	-	-
14	SHLD	O	-	Conditional output	-	-

				shielding		
15	PA5/SCL	I/O	TC	PA5	TIM1_CH1N I2C1_SCL	-
16	GND	G	-	Ground	-	-
17	PA8/SDA	I/O	TC	PA8	TIM1_CH2 I2C1_SDA TIM3_CH1	-
18	PA13	I/O	TC	PA13	SWDIO USART1_RX USART2_RX I2C1_SCL	-
19	GND	G	-	Ground	-	-
20	PA11	I/O	TC	PA11	USART1_SCK TIM1_CH2 TIM14_CH1 TIM3_CH1	ADC1_VIN[4]
21	PA12	I/O	TC	PA12	USART1_TX	ADC1_VIN[3]
22	PA3	I/O	TC	PA3	USART1_RX USART2_SCK	ADC1_VIN[2]
23	PA14(NRST)[3]	I/O	TC	PA14	SWCLK USART1_TX	-
24	PB1	I/O	TC	PB1	USART2_RX	ADC1_VIN[0]

Note 1: I=input, O=output, P=power supply, G=ground, A=analog

Note 2: TC: Standard IO, input signal does not exceed VDD voltage.

Note 3: When the SFT_NRST_RMP bit of RCC_SYSCFG is set to 1, PA14 is mapped to NRST external reset, and the low level is maintained at least 4us during reset.

4.2 Pin Multiplexing

Table 4.2-1 PA port multiplexing AF0-AF4

Pin	AF0	AF1	AF2	AF3	AF4
PA1	-	USART1_SCK	USART2_TX	I2C1_SDA	
PA3	-	USART1_RX	USART2_SCK	-	
PA5		TIM1_CH1N	-	I2C1_SCL	-
PA8		TIM1_CH2		I2C1_SDA	TIM3_CH1
PA11	-	USART1_SCK	TIM1_CH2	TIM14_CH1	TIM3_CH1
PA12	-	USART1_TX	-	-	-
PA13	SWDIO	USART1_RX	USART2_RX	I2C1_SCL	
PA14	SWCLK	USART1_TX	-	-	

Table 4.2-2 PB port multiplexing AF0-AF4

Pin	AF0	AF1	AF2	AF3	AF4
PB1	-	-	USART2_RX	-	-

5. Typical Application Circuit Diagram

The typical application circuit of MCP1081S single-ended mode is as follows:

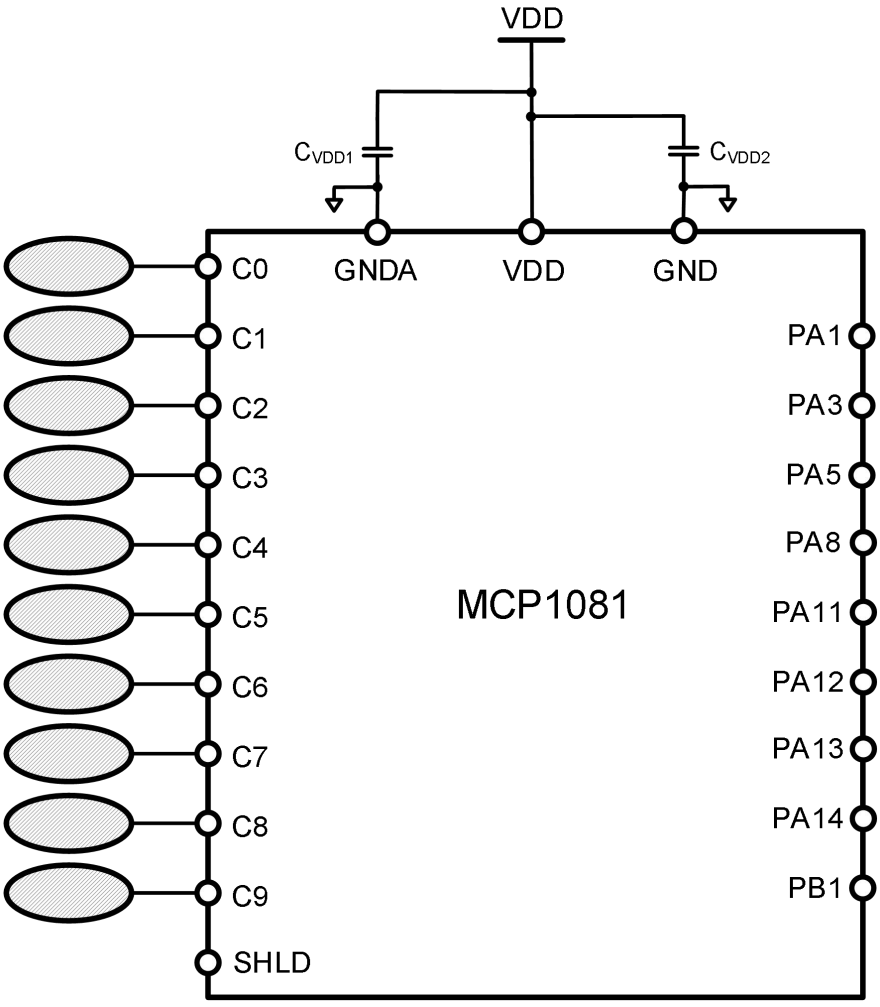


Figure 5.1 Typical Application Circuit of Single ended Mode

Among them, pins C0 to C9 are connected to a single ended electrode, and an internal 20pF is selected as the reference capacitor. The pin allocation in the figure is only an example. In practical applications, pins can be allocated to connect single ended electrodes, mutual capacitance electrodes, or external capacitors as needed. Please refer to section 8.3 for specific instructions. The values of VDD filtering capacitors CVDD1 and CVDD2 in the figure range from 100nF to 10uF, and both GND pins need to be grounded.

The typical application circuit of MCP1081's double terminal mode is as follows:

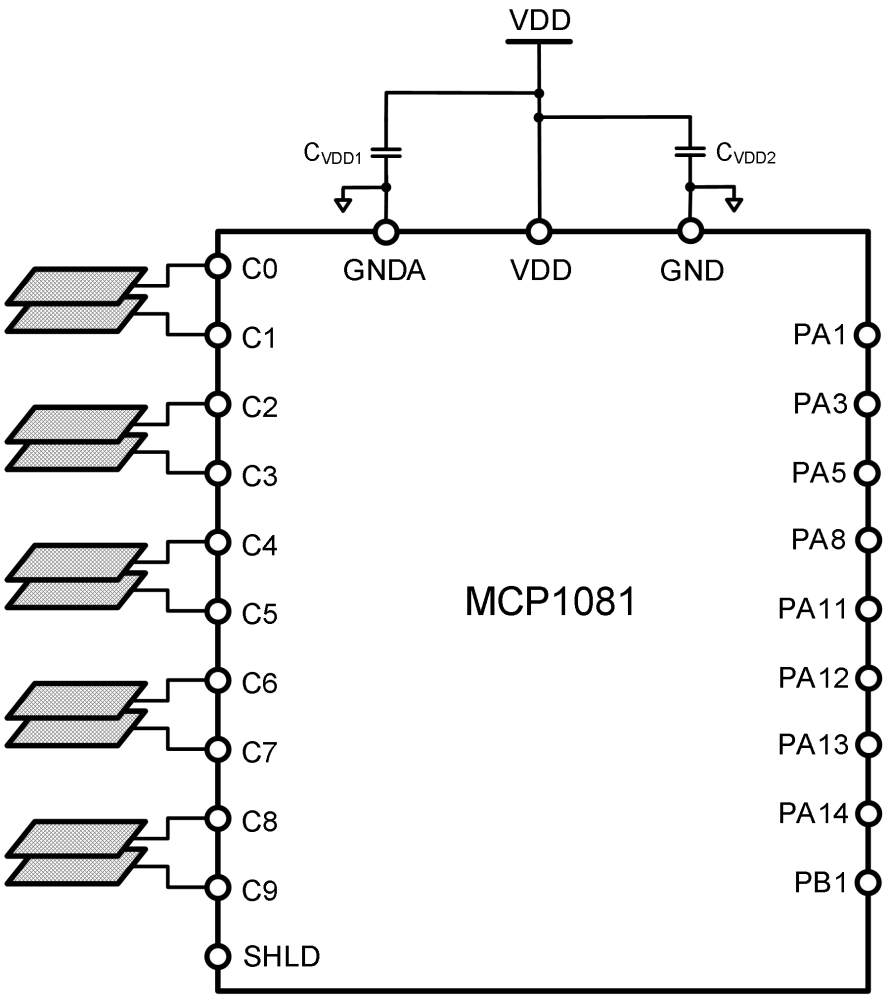


Figure 5.2 Typical Application Circuit of Dual-ended Mode

Among them, pins C0 and C1, C2 and C3, C4 and C5, C6 and C7, C8 and C9 are connected to double ended electrodes, and an internal 20pF is selected as the reference capacitor. In practical applications, pins can be allocated to connect double ended electrodes or external capacitors as needed. Please refer to section 8.3 for specific instructions. The values of VDD filtering capacitors CVDD1 and CVDD2 in the figure range from 100nF to 10uF, and both GND pins need to be grounded.

6. Functional Description

6.1 System Block Diagram

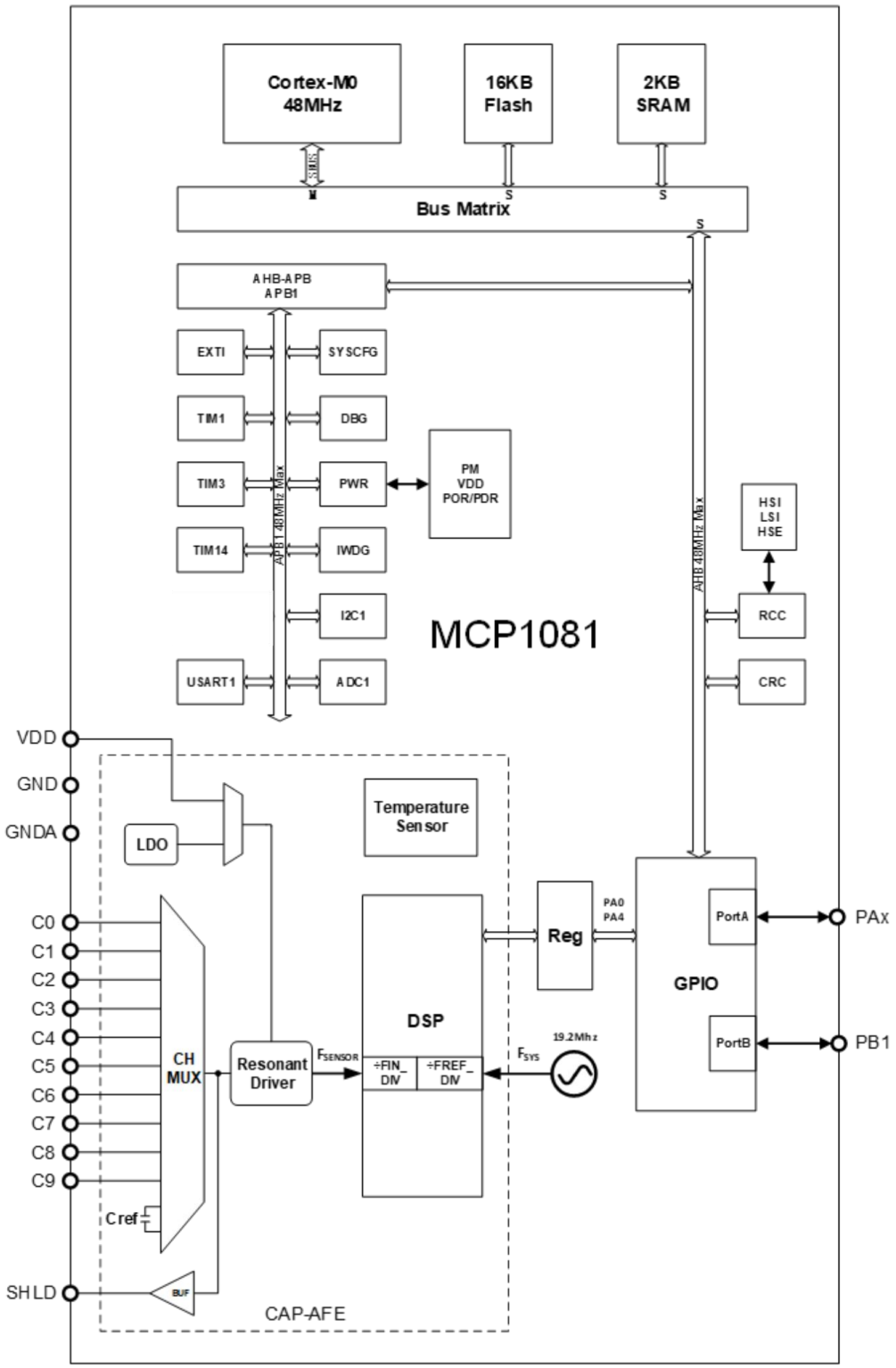


Figure 6.1 System Block Diagram

6.2 CAP-AFE

Referring to Figure 6.1, the chip is equipped with a highly integrated, multi-channel, and wide range capacitive sensing circuit, which can simultaneously measure up to 10 single ended capacitors or 5 double ended capacitors. It can be directly connected to the capacitor plate near the measured object according to application requirements, and the capacitance of the measured target can be calculated by measuring the oscillation frequency. AFE provides a reference by configuring different frequency division ratios through internal analog clock configuration. Internally integrated with a 16 bit high-precision digital temperature sensor, processor ports PA0 and PA4 are used for I2C communication between the chip and the capacitive sensing AFE.

6.3 Storage Image

Table 6.3 Storage Image

BUS	Address range	Size	Peripheral
Flash	0x08000000 - 0x080003FFF	16 KB	Main Flash memory
SRAM	0x20000000 - 0x200007FF	2 KB	SRAM
APB1	0x40000400 - 0x400007FF	1 KB	TIM3
	0x40003000 - 0x400033FF	1 KB	IWDG
	0x40005400 - 0x400057FF	1 KB	I2C1
	0x40007000 - 0x400073FF	1 KB	PWR
	0x40010000 - 0x400103FF	1 KB	SYSCFG
	0x40010400 - 0x400107FF	1 KB	EXTI
	0x40012400 - 0x400127FF	1 KB	ADC1
	0x40012C00 - 0x40012FFF	1 KB	TIM1
	0x40013000 - 0x400133FF	1 KB	Reserved
	0x40013400 - 0x400137FF	1 KB	DBGMCU
	0x40014000 - 0x400143FF	1 KB	TIM14
AHB	0x40021000 - 0x400213FF	1 KB	RCC
	0x40022000 - 0x400223FF	1 KB	Flash Interface
	0x40023000 - 0x400233FF	1 KB	CRC
	0x48000000 - 0x480003FF	1 KB	GPIOA
	0x48000400 - 0x480007FF	1 KB	GPIOB

6.4 NVIC

The chip embeds a Nested vector interrupt controller (NVIC), able to handle multiple maskable interrupt channels (excluding the 16 interrupt lines of the Cortex®-M0) and manage 4 programmable priority levels.

6.5 EXTI

The External Interrupt/Event Controller (EXTI) contains multiple edge detectors to capture the level changes on the I/O ports and generate interrupt/event to CPU. All I/O ports are connected to 16 external interrupt lines. Each interrupt line can be independently enabled or disabled and configured to select the trigger mode (rising edge, falling edge or both edges). A pending register can save all the interrupt request status.The EXTI can detect a pulse width shorter than the internal APB clock period.

6.6 Clock System

As shown in Figure 6.6, the chip contains the following internal or external clock sources:

- HSI 48MHz
- LSI 40KHz
- HSE

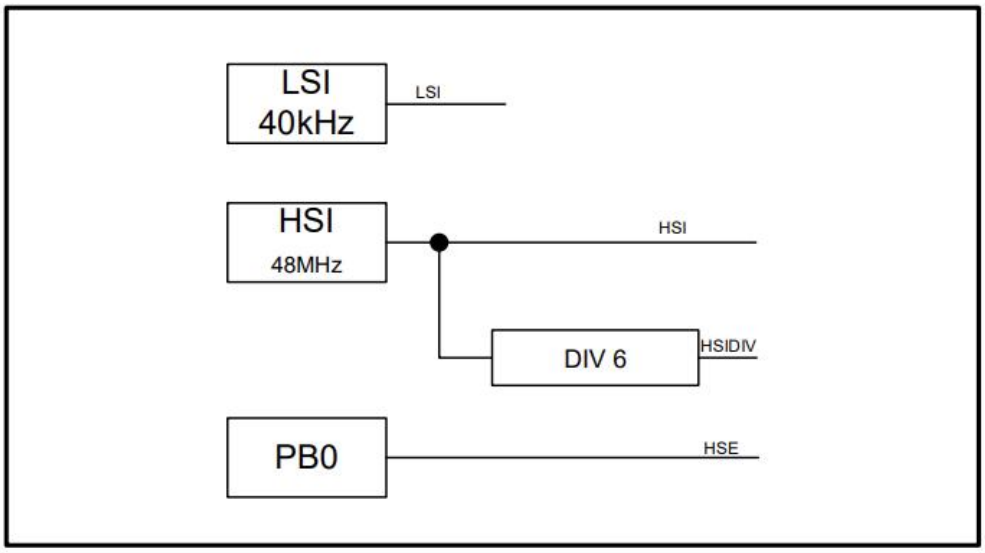


Figure 6.6 System Clock Source

The system clock can be selected from the following internal or external clocks:
HSI - HSI 48MHz output
HSIDIV - HSI 48MHz divide-by-6 output, i.e. 8MHz output
LSI - LSI 40KHz output
HSE - external clock input externally sourced from the OSC_IN (PB0) pin

The system clock is divided into CPU and AHB bus clocks, which operate at a maximum frequency of 48MHz. The maximum operating frequency of the APB bus is the same as that of the AHB bus.
After reset, HSIDIV (8MHz) is first used as the default system clock, followed by the

option to use HSI, LSI, or HSE as the clock source. When an invalid external clock is detected, the system automatically masks the external clock source and uses the internal oscillator instead. In this case, if the relevant interrupt monitoring switch is enabled, a corresponding interrupt request is also generated.

6.7 Timers and Watchdog

The chip has one advanced timer, one universal timer, one basic timer, one watchdog timer and one Systick timer.

Advanced timer (TIM1)
The advanced timer includes a 16-bit counter, four capture/compare channels and three phases complementary PWM generator. This timer supports hardware dead-time insertion when using as complementary PWM generator. This timer can also be used as a full- function general purpose timer.

The universal timer(TIM3) has a 16-bit counter, support both up and down counting, with automatically reload. The timer also has a 16-bit frequency pre-divider and four independent channels. Each channel can be used as input capture, output compare, PWM or single pulse output.

The basic timer (TIM14) has one 16-bit counter, supporting only up counting, with automatically reload. The timer also has one 16-bit frequency pre-divider and one independent channel. Each channel can be used as input capture, output compare, PWM or one pulse mode output.

The Independent Watchdog (IWDG) is based on a 12-bit down counter and an 8-bit prescaler. It is clocked by an internal independent 40KHz oscillator. As it is independent of the main clock, it can run in shutdown and standby modes. It can be used to reset the entire system when a system error occurs or as a free timer to provide timeout management for applications. It can be configured to start the watchdog by software or hardware through the option byte. In debug mode, the counter can be frozen.

The Systick timer is dedicated to the real-time operating system and can also be used as a general down counter. It has the following features:
- 24-bit down counter
- Auto-reload capability
- A maskable interrupt can be generated when counter value is 0
- Programmable clock source

6.8 GPIO

Each GPIO pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripherals function

port. Most GPIO pins are shared with digital or analog functions. If necessary, the peripheral functions of the I/O pins can be locked by specific operation to avoid accidental writing to the I/O register.

6.9 USART

The chip has two Universal Synchronous/Asynchronous Receiver/Transmitter (USART) interfaces. The USART provides flexibility for full-duplex data exchange with peripherals using the industry standard NRZ asynchronous serial data format. This module can support a wide range of baud rates through the integrated baud rate generator (including integer and fraction settings). Support LSB or MSB receive/transmit mode. Support 8- or 9-bit programmable data length. Support 0.5-/1-/1.5-/2-bit stop bit configuration. The USART can support synchronous or asynchronous one-way communication and half-duplex single-wire communication. Support maximum 6Mbps baud rate.

6.10 I2C

The chip is embedded with one I2C interface, which can operate in multiple master or slave modes, supporting standard mode (100Kbps) and fast mode (400Kbps). Supports 7-bit or 10 bit addressing.

6.11 ADC

The chip has one I2C interface. The I2C bus interface can work in multi-master mode or slave mode and supports standard mode (100Kbps) and fast mode (400Kbps). The I2C interface supports 7-bit or 10-bit addressing.

6.12 CRC

The cyclic redundancy check (CRC) module uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. Among many applications, CRC is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC60335-1 standard, it provides a method to detect flash memory errors. The CRC module can be used to calculate the signature of the software package in real time and compare it with the signature generated when the software is linked and generated.

6.13 SWD

This chip equips Arm standard Serial Wire Debug (SWD).

7. Electrical Characteristics

7.1 Capacitance Measurement

The electrical characteristics of the chip capacitor measurement are as shown in the following table. Unless otherwise specified, the data conditions in the table are at T = 25℃.

Table 7.1-1 Power Supply

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
Power						
V_{DD}	Supply voltage	T = -40℃ to +85℃	2.3		5.5	V
I_{VDD}	Measuring peak current (1)	Single-Terminal Mode	0.63		3.35	mA
		Double-Terminals Mode	0.93		2.75	mA
I_{DDAVG}	Average conversion current (2)	V_{DD}=5V		12		uA
I_{DDSL}	Sleep mode current	V_{DD}=5V		7		uA

Note 1: Measuring peak current indicates the operating current during CAP AFE measurement.
Note 2: The test condition for average conversion current is to convert once every 1 second, with a drive current of 4uA and a conversion duration of 1ms. After the conversion is complete, the chip enters sleep mode.

Table 7.1-2 CAP AFE

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
Capacitive sensing						
C_{SENSOR}	Measured capacitance		0.001		10	nF
C_{IN}	Pin parasitic capacitance			5		pF
N_{BITS}	Data bits				16	Bit
f_{cs}	Channel sampling rate		0.01		2	kSPS
Oscillator						
f_{SENSOR}	Oscillator frequency range	T = -40℃ to +85℃	0.1		30	MHz
I_{DRIVE}	Oscillator driving current	single channel	4		2000	uA
Internal clock						
f_{INTCLK}	Internal clock frequency	T = 25℃		19.2		MHz
TC_{INTCLK}	Internal clock temperature drift	T = -40℃ to +85℃		25	100	ppm/℃

7.2 Absolute Maximum Rating

If the load applied to the device exceeds the values given in the "Absolute Group Maximum Rated Values" list (Tables 7.2-1, 7.2-2, 7.2-3), it may cause permanent damage to the device. This only provides the maximum load that can be sustained, and does not mean that the functional operation of the device is correct under

these conditions. Long term operation of the device under maximum conditions can affect its reliability.

Table 7.2-1 Voltage Characteristics

Symbol	Description	Minimum	Maximum	Unit
VDD – GND VDD – GNDA	External main supply voltage	-0.3	5.8	V
VIN (1)	Input voltage on other pins	GND-0.3	VDD+0.3	

Note 1: The maximum value of VIN must always be followed. For information on the maximum allowed injection current values, please refer to the table below.

Table 7.2-2 Current Characteristics

Symbol	Description	Maximum	Unit
I_{VDD} (1)	Total current through VDD power pins (supply current) (1)	+60	mA
I_{GND}/V_{GNDA} (1)	Total current through GDN/GNDA ground pins (outflow current) (1)	-60	
I_{IO}	Output sink current on any I/O and control pins, VDD = 5.0V	+20	
	Output source current on any I/O and control pins, VDD = 5.0V	-20	
	Output sink current on any I/O and control pins, VDD = 3.3V	+15	
	Output source current on any I/O and control pins, VDD = 3.3V	-15	
	Output sink current on any I/O and control pins, VDD = 2.3V	+6	
	Output source current on any I/O and control pins, VDD = 2.3V	-6	
$I_{INJ(PIN)}$ (2)(3)	NRST pin injection current	±5	
	HSE OSC_IN pin injection current	±5	
$\sum I_{INJ(PIN)}$ (5)	Other pins injection current (4)	±25	

Note 1: All main power (VDD) and ground (GND, GNDA) pins must always be connected to an external power supply in the permitted range.

Note 2: This current consumption must be correctly distributed to all I/O and control pins. The total output current must not be injected/pulled between two consecutive power pins of the LQFP package with a reference high pin count.

Note 3: The reverse injection current can interfere with the analog performance of the device.

Note 4: When $V_{IN} > V_{DD}$, a positive injected current is generated; when V_{IN} < GND/GNDA, a reverse injected current is generated. Do not exceed $I_{INJ(PIN)}$.

Note 5: When there is simultaneous injection current for multiple inputs, the maximum value of $\Sigma I_{INJ(PIN)}$ is equal to the sum of the absolute values of the forward injection current and the reverse

injection current (instantaneous value).

Table 7.2-3 Temperature Characteristics

Symbol	Description	Minimum	Maximum	Unit
T_J	Junction temperature	-40	105	℃
T_{stg}	Storage temperature	-40	105	℃

Note: The above parameters are limit values. This specification does not apply to the functional operation of the device in environments beyond these limit conditions. Long-term exposure to such extreme environments may affect the reliability of the device.

7.3 Operating conditions

7.3.1 General operating conditions

Table 7.3.1 General operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	-	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	-	-	48	
V_{DD}	Operating voltage		2.3	3.3	5.5	V
P_D	Power dissipation	QSOP24	-	-	270	mW
T_A	Ambient temperature (Industrial level)	-	-40	-	85	°C

7.3.2 Operating Conditions at power-up/power-down

The parameters given in the following table are tested under the general operating conditions specified in Table 7.3.1.

Table 7.3.2 Operating Conditions at power-up/power-down

Symbol	Conditions	Min.	Typ.	Max.	Unit
t_{VDD}	V_{DD} rise time t_r	0.2	-	∞	us/V
	V_{DD} fall time t_f	60	-	∞	
Vft(3)	Power-down threshold voltage	-	0	-	mV

Note 1: Data based on characterization results, not tested in production.

Note 2: The V_{DD} waveforms of chip power-on and power-down must strictly follow the t_r and t_f phased in the following waveform diagram, and no power-down is allowed during power-on process.

Note 3: To ensure the reliability of chip power-on, all power-on should start from 0V.

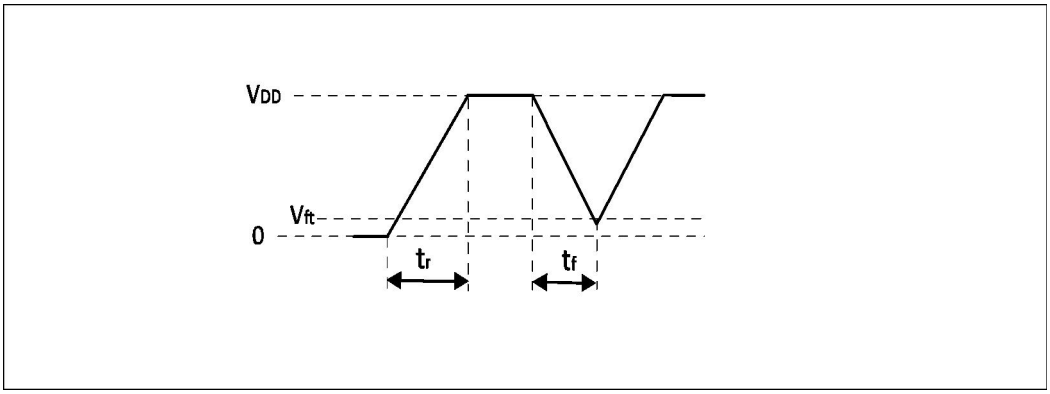


Figure 7.3.2 Power on and power-down waveforms

7.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed in Table 7.3.1.

Table 7.3.3 Embedded reset and power control block characteristics

Symbol	Parameter	Condition	Min.(3)	Typ.	Max.(3)	Unit
V_{PVD}	Level selection of programmable voltage detectors	PLS[3:0]=0000 (Rising edge)	-	1.8	-	V
		PLS[3:0]=0000 (Falling edge)	-	1.7	-	
		PLS[3:0]=0001 (Rising edge)	-	2.1	-	
		PLS[3:0]=0001 (Falling edge)	-	2.0	-	
		PLS[3:0]=0010 (Rising edge)	-	2.4	-	
		PLS[3:0]=0010 (Falling edge)	-	2.3	-	
		PLS[3:0]=0011 (Rising edge)	-	2.7	-	
		PLS[3:0]=0011 (Falling edge)	-	2.6	-	
		PLS[3:0]=0100 (Rising edge)	-	3.0	-	
		PLS[3:0]=0100 (Falling edge)	-	2.9	-	
		PLS[3:0]=0101 (Rising edge)	-	3.3	-	
		PLS[3:0]=0101 (Falling edge)	-	3.2	-	
		PLS[3:0]=0110 (Rising edge)	-	3.6	-	
		PLS[3:0]=0110 (Falling edge)	-	3.5	-	
		PLS[3:0]=0111 (Rising edge)	-	3.9	-	
		PLS[3:0]=0111 (Falling edge)	-	3.8	-	
		PLS[3:0]=1000 (Rising edge)	-	4.2	-	
		PLS[3:0]=1000 (Falling edge)	-	4.1	-	

		PLS[3:0]=1001 (Rising edge)	-	4.5	-	
		PLS[3:0]=1001 (Falling edge)	-	4.4	-	
		PLS[3:0]=1010 (Rising edge)	-	4.8	-	
		PLS[3:0]=1010 (Falling edge)	-	4.7	-	
$V_{POR/PDR}$(1)	Power-on reset	-	-	1.65	-	V
V_{hyst_PDR}	PDR hysteresis	-	-	50	-	mV
$T_{RSTTEMPO}$(2)	Reset duration	-	-	4.7	-	ms

Note 1: 1.The product behavior is guaranteed by design down to the minimum value $V_{POR/PDR}$.
Note 2: Guaranteed by design and not tested during production.
Note 3: Based on comprehensive evaluation. The measurement method for reset duration is from power-on (POR reset) to the moment when the first IO flip of the user's application code occurs.

7.3.4 Built-in voltage reference

The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed in Table 7.3.1

Table 7.3.4 Built-in voltage voltage reference

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{REFINT}	Built-in voltage reference	-40°C<TA<85°C	-	1.2	-	V
$T_{s\_vrefint}$(1)	ADC sampling time when readout build-in voltage	-	-	11.8	-	us

Note 1: The shortest sampling time is obtained through multiple iterations in the application.

7.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. All Run-mode current consumption measurements given in this section are performed with a reduced code. (stopping the capacitance measurement section).

current consumption

The MCU is placed under the following conditions:
All I/O pins are in input mode and connected to a static level - V_{DD} or GND (no load).
All peripherals are disabled except when explicitly mentioned
The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting cycle, 24 ~ 48 MHz is 1 waiting cycle).

The instruction prefetching function is on. When the peripherals are enabled: $f_{PCLK1} = f_{HCLK}$.

Note: The instruction prefetching function must be set before setting the clock and bus frequency division.

The parameters given in the table below are based on the ambient temperature and the VDD supply voltage listed in Table 7.3.1.

Table 7.3.5-1 Typical Current Consumption in Operating Mode

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled					Typical All peripherals disabled					Unit
				-40°C	0°C	25°C	55°C	85°C	- 40° C	0°C	25°C	55°C	85°C	
I_{DD}	Supply current in Run mode	HSI is clock source	48M	4.22	4.36	4.43	4.54	4.63	3.06	3.19	3.25	3.35	3.44	mA
			24M	3.05	3.16	3.23	3.31	3.39	2.34	2.45	2.50	2.58	2.66	
			12M	2.15	2.27	2.32	2.40	2.46	1.81	1.91	1.96	2.04	2.09	
			6M	1.70	1.79	1.85	1.92	2.00	1.53	1.62	1.67	1.74	1.82	
			3M	1.22	1.30	1.35	1.42	1.48	1.13	1.21	1.26	1.33	1.39	
			750K	0.87	0.94	0.98	1.04	1.10	0.84	0.91	0.95	1.01	1.07	
			375K	0.80	0.87	0.91	0.97	1.03	0.79	0.86	0.90	0.96	1.02	
			187.5K	0.77	0.84	0.88	0.94	1.00	0.77	0.84	0.88	0.93	0.99	
			93.75K	0.76	0.83	0.87	0.92	0.98	0.75	0.83	0.86	0.92	0.98	
		HSIDIV is clock source	8M	1.83	1.92	1.70	1.78	1.84	1.63	1.73	1.50	1.57	1.64	
			4M	1.68	1.76	1.79	1.51	1.57	1.56	1.65	1.65	1.39	1.45	
			2M	1.19	1.28	1.32	1.39	1.46	1.13	1.22	1.27	1.33	1.40	
			1M	0.95	1.03	1.07	1.13	1.19	0.92	1.00	1.04	1.10	1.16	
			500K	0.83	0.90	0.94	1.00	1.06	0.81	0.89	0.93	0.99	1.04	
			125K	0.74	0.81	0.85	0.91	0.96	0.73	0.80	0.84	0.90	0.96	
			62.5K	0.72	0.79	0.83	0.89	0.94	0.72	0.79	0.83	0.89	0.94	
			31.25K	0.71	0.78	0.82	0.88	0.93	0.71	0.78	0.82	0.88	0.93	
		LSI is clock source	40K	0.19	0.21	0.21	0.22	0.23	0.19	0.20	0.21	0.22	0.23	

Table 7.3.5-2 Typical Current Consumption in Sleep Mode

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled					Typical All peripherals disabled					Unit
				- 40°C	0°C	25°C	55°C	85°C	- 40°C	0°C	25°C	55°C	85°C	
I_{DD}	Supply current in Sleep mode	HSI is clock source	48M	3.24	3.35	3.41	3.50	3.58	2.09	2.18	2.24	2.32	2.40	mA
			24M	2.18	2.27	2.33	2.40	2.48	1.49	1.57	1.62	1.69	1.76	
			12M	1.51	1.59	1.64	1.71	1.78	1.16	1.24	1.29	1.35	1.42	
			6M	1.67	1.76	1.81	1.89	1.97	1.50	1.58	1.64	1.71	1.78	
			3M	1.20	1.29	1.33	1.39	1.46	1.12	1.20	1.24	1.31	1.37	
			750K	0.86	0.94	0.98	1.04	1.10	0.84	0.91	0.95	1.01	1.07	
			375K	0.80	0.87	0.91	0.97	1.03	0.79	0.86	0.90	0.96	1.02	
			187.5 K	0.77	0.84	0.88	0.94	0.99	0.76	0.84	0.88	0.93	0.99	
			93.75 K	0.76	0.83	0.87	0.92	0.98	0.75	0.82	0.86	0.92	0.98	
		HSIDIV is clock source	8M	1.30	1.39	1.44	1.51	1.58	1.11	1.20	1.24	1.31	1.38	
			4M	1.75	1.81	1.26	1.26	1.33	1.63	1.69	1.11	1.15	1.21	
			2M	1.23	1.32	1.37	1.44	1.50	1.18	1.26	1.31	1.39	1.44	
			1M	0.97	1.05	1.09	1.15	1.21	0.94	1.02	1.06	1.12	1.19	
			500K	0.84	0.91	0.95	1.01	1.07	0.82	0.89	0.94	1.00	1.06	
			125K	0.74	0.81	0.85	0.91	0.96	0.73	0.80	0.84	0.90	0.96	
			62.5K	0.72	0.79	0.83	0.89	0.94	0.72	0.79	0.83	0.89	0.94	
			31.25 K	0.71	0.78	0.82	0.88	0.93	0.71	0.78	0.82	0.88	0.93	
		LSI is clock source	40K	0.19	0.21	0.21	0.22	0.23	0.19	0.20	0.21	0.22	0.23	

Table 7.3.5-3 Typical Current Consumption in Stop Mode (1)

Symbol	Parameter	Conditions	Typical					Unit
			-40°C	0°C	25°C	55°C	85°C	
I_{DD}	Supply current in Stop mode	Enter Stop mode after reset, V_{DD}=3.3V	110.19	117.98	121.73	125.54	113.52	μA
	Supply current in Deep Stop mode	Enter Deep Stop mode after reset, V_{DD}=3.3V	5.75	6.20	6.44	6.79	7.76	

Note 1: The I/O status is analog input.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table.

The MCU is placed under the following conditions:
All I/O pins are in analog input mode and connected to a static level - V_{DD} or GND (no load).
All peripherals are disabled unless otherwise specified.
The given value is calculated by measuring the current consumption.
– When all peripherals are clocked off
– When only one peripheral is clocked on

Table 7.3.5-4 On-chip peripheral current consumption(1)

Symbol	Parameter	Bus	Typical	Unit
I_{DD}	CRC	AHB	0.67	uA/MHz
	GPIOA		0.32	
	GPIOB		0.27	
	TIM1	APB1	5.11	
	I2C1		4.95	
	TIM3		3.13	
	USART1		1.96	
	TIM14		1.50	
	ADC1		0.73	
	PWR		0.10	
	EXTI		0.09	
	SYSCFG		0.09	
	DBG		0.04	
	WWDG		0.03	

Note 1: f_{HCLK}=48MHz, f_{APB1}=f_{HCLK}, the prescale coefficient of each peripheral is the default value.

Wake up time from low power mode

The wake-up time listed in the table below is measured during the wake-up process of the internal clock HSI. The clock source used to wake up the chip depends on the current operating mode:
Stop or Standby mode: the clock source is the oscillator
Sleep mode: the clock source is the clock used when entering the Sleep mode.
The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 7.3.1.

Table 7.3.5-5 Wake up time for low-power mode

Symbol	Parameter	Conditions	Typical	Unit
$t_{WUSLEEP}$	Wake up from Sleep mode	System clock is HSIDIV	3.22	μs
t_{WUSTOP}	Wake up from Stop mode	System clock is HSIDIV	26.65	μs

$t_{WUDEEPSTOP}$	Wake up from Deep Stop mode	System clock is HSIDIV	28.88	μs

7.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristic parameters given in the following table are measured by a high-speed external clock source, and the ambient temperature and power supply voltage meet General operating conditions.

Table 7.3.6 High-speed external user clock characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{HSE_ext}	User external clock source frequency (1)	-	-	8	48	MHz
V_{HSEH}	OSC_IN input high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input low level voltage	GND	GND	-	$0.3V_{DD}$	V
$t_{w(HSE)}$	OSC_IN high or low time (1)	-	20	-	-	ns

Note 1: Guaranteed by design and not tested during production.

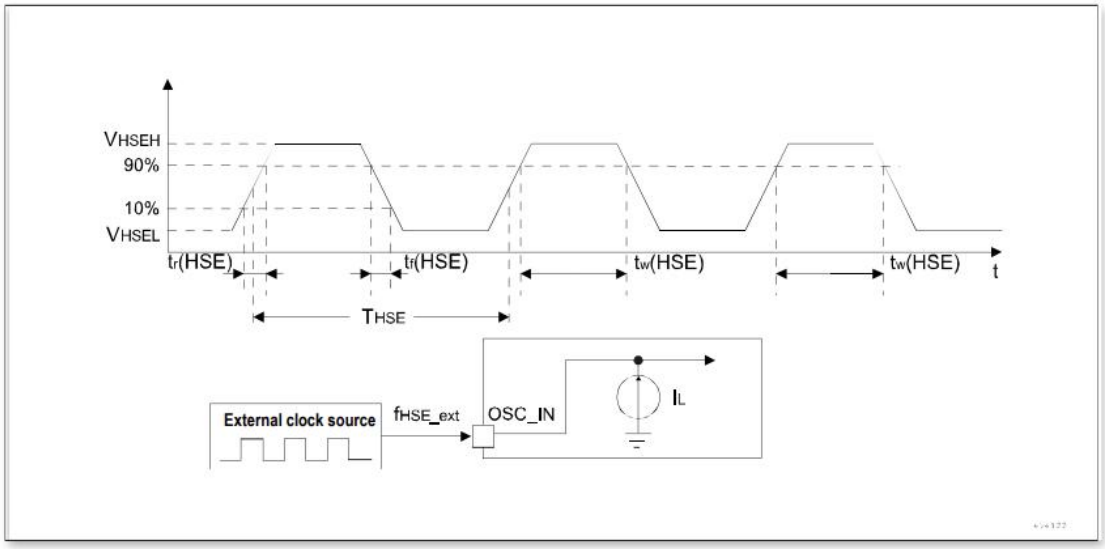


Figure 7.3.6 High-speed external clock source AC timing diagram

7.3.7 Internal clock source characteristics

The characteristic parameters given in the table below are measured using ambient temperature and supply voltage in accordance with general operating conditions.

High speed internal (HSI) oscillator

Table 7.3.7-1 HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	-	-	48	-	MHz
ACC_{HSI}(3)	HSI oscillator deviation	TA = 0°C ~ 55°C	-1	-	1	%
		TA = -40°C ~ 85°C	-2	-	2	%
$T_{stab(HSI)}$(2)	HSI oscillator startup time	-	-	-	20	μs
$I_{DD(HSI)}$(2)	HSI oscillator power consumption	-	-	480	-	μA

Note 1: V_{DD}=3.3V, TA=-40 ℃~85 ℃, unless otherwise specified.
Note 2: Guaranteed by design and not tested during production.
Note 3: Based on comprehensive evaluation.

Low speed internal (LSI) oscillator

Table 7.3.7-2 LSI Oscillators Characteristics(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSI}	Frequency	-	-	40	-	KHz
ACC_{LSI}(3)	LSI oscillator deviation	TA = 0°C ~ 55°C	-15	-	15	%
		TA = -40°C ~ 85°C	-20	-	20	%
$T_{stab(LSI)}$ (2)	LSI oscillator startup time	-	-	-	100	μs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	-	-	1	-	μA

Note 1: VDD=3.3V, TA=-40 ℃~+85 ℃, unless otherwise specified.
Note 2: Guaranteed by design and not tested during production.
Note 3: Obtained from comprehensive evaluation.

7.3.8 Memory Characteristics

Table 7.3.8 Flash Memory Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{prog}	16-bit programming time	-	-	37.24	-	μs
t_{ERASE}	Page (1024 bytes) erase time	-	4	-	6	ms
t_{ME}	Mass erase time	-	30	-	40	ms

I_{DD}	Supply current	Read mode	-	-	1.5	mA
		Write mode	-	-	2	mA
		Erase mode	-	-	1	mA
N_{END}	Endurance	TA = 85°C	100000	-	-	Cycles
T_{DR}	Data retention	TA = 25°C	25	-	-	Years

7.3.9 EMC Characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (Electromagnetic Susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:
Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until functional interference occurs. This test complies with the IEC 61000-4-2 standard.
FTB: A Burst of Fast Transient voltage (positive and negative) is applied to VDD and GND through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 1000-4-4 standard.
The chip reset allows normal operations to be resumed. The test results are given in the following table.

Table 7.3.9 EMS Characteristics

Symbol	Parameter	Conditions	Level/Type
V_{FESD}	Voltage limit applied to any I/O pin, resulting in malfunction	V_{DD} = 3.3V, TA= +25℃, f_{HCLK} = 48MHz. Conforming to IEC61000-4-2	2A
V_{FEFT}	Fast transient voltage burst limits to be applied through 100 pF on VD_D and GND pins to induce a functional disturbance	V_{DD} = 3.3V, TA= +25℃, f_{HCLK} = 48MHz. Conforming to IEC61000-4-4	2A

Design reliable software to avoid the problem of noise.

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software.
Therefore, it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for this application.

Software recommendations

The software process must include control of program execution, such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers, etc.)

Pre-certification tests

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.
To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors.

7.3.10 I/O Port Characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 7.3.1 are used for tests. All I/O ports are CMOS compatible.

Table 7.3.10-1 I/O Static Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IL}	Low level input voltage	-	-	-	0.3 * VD_D	V
V_{IH}	High level input voltage	-	0.7 * VD_D	-	-	V
V_{hy}	Schmitt trigger hysteresis (1)	-	0.1 * VD_D	-	-	V
I_{lkg}	Input leakage current (2)	-	-1	-	1	μA
R_{PU}	Weak pull-up equivalent	V_{IN}= GND	-	60	-	kΩ
R_{PD}	Weak pull-down equivalent	V_{IN}= VD_D	-	60	-	kΩ
C_{IO}	I/O pin capacitance	-	-	-	10	pF

Note 1: Drawn from comprehensive evaluation, not tested in production.
Note 2: If there is reverse current in the adjacent pin, the leakage current may be higher than the maximum value.
Note 3: The pull-up and pull-down resistors are poly resistors.

Output driving current

The GPIOs (General Purpose Input/Output Ports) can sink or source up to ± 20mA current.
In the user application, the number of I/O pins must ensure that the driving current

does not exceed the absolute maximum rated value:

- The sum of the currents sourced by all the I/O pins on V_{DD}, plus the maximum operating current that the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents drawn by all I/O ports and flowing out of GND, plus the maximum operating current of the MCU flowing out on GND, cannot exceed the absolute maximum rating I_{GND}.

Output voltage

Unless otherwise stated, the parameters listed in the table below are provided under the ambient temperature and VDD supply voltage in accordance with the conditions summarized in Table 7.3.1. All I/O ports are CMOS compatible.

Table 7.3.10-2 Output Voltage Characteristics (3)

Symbol	Parameter	Conditions	Typical	Unit
V_{OL} (1)	Output low voltage	|IIO|= 6mA，VDD=2.3V	0.31	V
V_{OH} (2)	Output high voltage		1.90	
V_{OL} (1)	Output low voltage	|IIO|= 6mA，VDD=3.3V	0.2	
V_{OH} (2)	Output high voltage		3.01	
V_{OL} (1)	Output low voltage	|IIO|= 8mA，VDD =3.3V	0.27	
V_{OH} (2)	Output high voltage		2.91	
V_{OL} (1)	Output low voltage	|IIO|= 6mA，VDD=5.0V	0.15	
V_{OH} (2)	Output high voltage		4.75	
V_{OL} (1)	Output low voltage	|IIO|= 8mA，VDD =5.0V	0.2	
V_{OH} (2)	Output high voltage		4.67	
V_{OL} (2)	Output low voltage	|IIO|=20mA，VDD =5.0V	0.54	
V_{OH} (2)	Output high voltage		4.18	

Note 1: The current I_{IO} drawn by the chip must always follow the absolute maximum ratings given in the table, and the sum of IIO (all I/O pins and control pins) cannot exceed I_{GND}.

Note 2: The current I_{IO} output by the chip must always follow the absolute maximum rated value given in the table, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VDD}.

Note 3: Resulted from comprehensive evaluation.

The definitions and values of the input and output AC characteristics are given in the following figure and table, respectively.

Unless otherwise stated, the parameters listed in the following table are provided under the ambient temperature and supply voltage in accordance with the condition Table 7.3.1.

Table 7.3.10-3 I/O AC Characteristics (1)

Symbol	Parameter	Conditions	Typical	Unit
$t_{f(IO)out}$	Output fall time	C_L = 50pF	5.8	ns
$t_{r(IO)out}$	Output rise time	V_{DD} = 3.3V	5.6	ns

Note 1: Guaranteed by design and not tested during production.

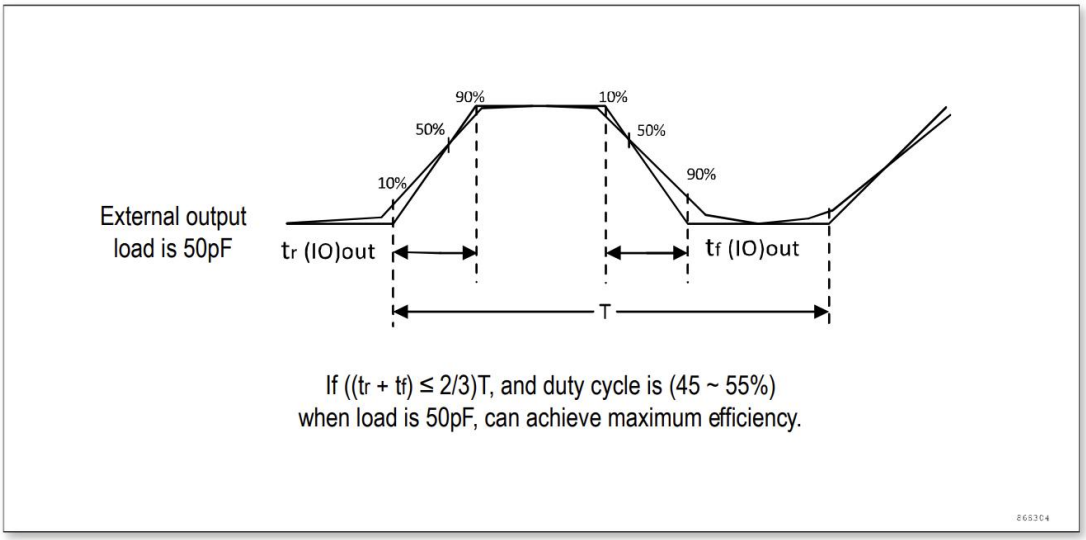


Figure 7.3.10 I/O AC Characteristics

7.3.11 Timer Characteristics

The parameters listed in the following table are guaranteed by design.

Table 7.3.11 TIMx (1) characteristics

Symbol	Parameter	Condition	Minimum	Maximum	Unit
t_{res}(TIM)	Timer resolution	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 48MHz	20.8	-	ns
f_{EXT}	External clock frequency of channel 1 to 4	-	0	-	MHz
		$f_{TIMxCLK}$= 48MHz	0	24	
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 48MHz	0.0208	1365.3	us
t_{MAX_COUNT}	Maximum possible counter value (TIM_PSC adjustable)	-	-	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 48MHz	-	1365.3	us

t_{MAX_IN}	TIM maximum input frequency	-	-	48	MHz

Note 1: Guaranteed by design, not tested in production.

7.3.12 I2C Interface Characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, fPCLK1 frequency and supply voltage conditions summarized in Table 7.3.1.
The I2C interface conforms to the standard I2C communication protocol but has the following limitations: SDA and SCL are not true open-drain pins. When configured as open- drain output, the PMOS transistor between the pin and VDD is disabled, but still present.

Table 7.3.12 I2C Characteristics

Symbol	Parameter	Standard I2C (1)		Fast mode I2C (1)		Unit
		Minimum	Maximum	Minimum	Maximum	
$t_{w(SCLL)}$	SCL clock low time	$9*t_{PCLK}$	-	$9*t_{PCLK}$	-	us
$t_{w(SCLH)}$	SCL clock high time	$18*t_{PCLK}$	-	$18*t_{PCLK}$	-	us
$t_{su(SDA)}$	SDA setup time	$1*t_{PCLK}$	-	$1*t_{PCLK}$	-	ns
$t_{h(SDA)}$	SDA data retention time	0 (3)	- (4)	0 (3)	- (4)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rising time	-	1000	20	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	$20\times(V_{DD}/5.5V)$	300	ns
$t_{vd(DAT)}$ (5)	Data valid time	-	$8*t_{PCLK}$ - 1 (4)	-	$8*t_{PCLK}$ - 0.3 (4)	us
$t_{vd(ACK)}$ (6)	Data valid acknowledge time	-	$8*t_{PCLK}$ - 1 (4)	-	$8*t_{PCLK}$ - 0.3 (4)	us
$t_{h(STA)}$	Start condition hold time	$8*t_{PCLK}$	-	$8*t_{PCLK}$	-	us
$t_{su(STA)}$	Start condition setup time	$19*t_{PCLK}$	-	$17*t_{PCLK}$	-	us
$t_{su(STO)}$	Stop condition setup time	$17*t_{PCLK}$	-	$17*t_{PCLK}$	-	us
$t_{w(STO:STA)}$	Time from Stop condition to Start condition (bus idle)	$484*t_{PCLK}$	-	$144*t_{PCLK}$	-	us
C_b	Capacitive load of each bus	-	400	-	400	pF

Note 1: Guaranteed by design, not tested in production.
Note 2: f_{PCLK1} must be at least 3MHz to achieve standard mode I2C frequencies. It must be at least 12MHz to achieve fast mode I2C frequencies.
Note 3: Ensure SCL drops below $0.3V_{DD}$ on falling edge before SDA crosses into the indeterminate range of $0.3V_{DD}$ to $0.7V_{DD}$.
Note: For controllers that cannot observe the SCL falling edge then independent measurement of the time for the SCL transition from static high (V_{DD}) to $0.3V_{DD}$ should be used to insert a delay of the SDA transition with respect to SCL.
Note 4: The maximum $t_{h(SDA)}$ could be 3.45 us and 0.9 us for Standard mode and Fast mode, but

must be less than the maximum of $t_{vd(DAT)}$ or $t_{vd(ACK)}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period ($t_{w(SCLL)}$)of the SCL signal. If the clock stretches the SCL, the data must be valid by the setup time before it releases the clock.

Note 5: $t_{vd\ (DAT)}$=time for data signal from SCL LOW to SDA output.

Note 6: $t_{vd\ (ACK)}$=time for Acknowledgement signal from SCL LOW to SDA output.

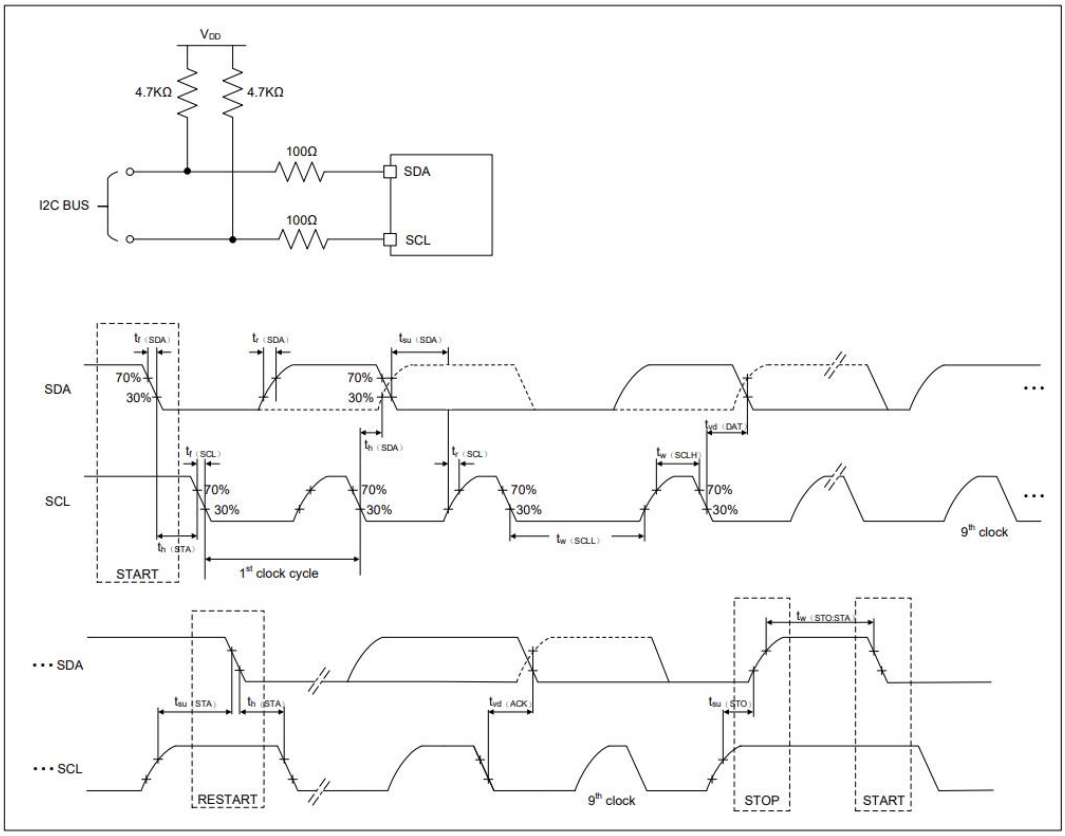


Figure 7.3.12 I2C bus AC waveform and measurement circuit (1)

Note 1: The measurement point is set to CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

7.3.13 USART characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 7.3.1.

Table 7.3.14 USART Characteristics (1)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
f_{SCLK}	USART clock	Master mode, T_A = 25°C	-	6	MHz
$1/t_{c(SCLK)}$	frequency	Slave mode, T_A = 25°C	-	6	
$t_{r(SCLK)}$	SCLK clock rise time	Load capacitance: C = 15pF	-	6	ns

$t_{f(SCLK)}$	SCLK clock fall time	Load capacitance: C =15pF	-	6	ns
$t_{w(SCLKH)}$ (1)	SCLK high time	-	$t_{c(SCLK)}/2 - 6$	$t_{c(SCLK)}/2 + 6$	ns
$t_{w(SCLKL)}$ (1)	SCLK low time	-	$t_{c(SCLK)}/2 - 6$	$t_{c(SCLK)}/2 + 6$	ns
$t_{su(MI)}$ (1)	Data input setup	Master mode, f_{PCLK} = 48MHz, prescaler = 8	5	-	ns
$t_{su(SI)}$ (1)	time	Slave mode	5	-	ns
$t_{h(MI)}$ (1)	Data input hold	Master mode, f_{PCLK} = 48MHz, prescaler = 8	5	-	ns
$t_{h(SI)}$ (1)	time	Slave mode	5	-	ns
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	10	ns
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	26	ns

Note 1: Guaranteed by design and not tested during production.

7.3.14 ADC Characteristics

Unless otherwise specified, the parameters in the table below are measured under the ambient temperature, f_{PCLK2} frequency and V_{DD} supply voltage in accordance with the conditions summarized in Table 7.3.1.

Table 7.3.15 ADC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	-	2.5	3.3	5.5	V
F_{ADC}	ADC clock frequency	-	-	-	16	MHz
F_S(1)	Sampling frequency	-	-	-	1	MHz
F_{TRIG}(1)	External trigger frequency (3)	f_{ADC}=16MHz	-	-	1	MHz
		-	-	-	16	$1/f_{ADC}$
V_{AIN}(2)	Conversion voltage range	-	0	-	VDD	V
R_{AIN} (1)	External input impedance	-	See equation 2			kΩ
R_{ADC}(1)	Sampling switch resistance	-	-	-	1.5	kΩ
C_{ADC} (1)	Internal sample and hold capacitance	-	-	-	10	pF
T_{STAB} (1)	Stabilization time	-	-	-	10	μs
T_{LATR}(1)	Delay between trigger and conversion start	-	-	-	-	1/fADC
T_S(1)	Sampling time	f_{ADC}=16MHz	0.156	-	15.031	μs

		-	2.5	-	240.5	$1/f_{ADC}$
T_{CONV} (1)	Total conversion time (including sampling time)	f_{ADC}=16MHz	0.9375	-	15.8125	μs
		-	15 ~ 253 (sampling ts+ successive approximation			$1/f_{ADC}$
ENOB	Effective number of bits	-	-10.5			bit

Note 1: Guaranteed based on test during characterization. Not tested in production.

Note 2: Guaranteed by design, not tested during production.

Note 3: In this product, V_{REF+} is internally connected to V_{DD}, V_{REF-} is internally connected to GND.

Note 4: Guaranteed by design, not tested during production.

Note 5: For external triggers, a delay of $1/f_{ADC}$ must be added.

8. Feature Description

8.1 Clock System

In the system block diagram of MCP1081, f_{sys}, f_{ref}, f_{sensor}, and f_{in} are four crucial clock signals. Among these, f_{sensor} represents the oscillation frequency of the capacitance measurement circuit. After being divided by FIN_DIV, the measured clock signal fin is obtained. f_{sys} is the system clock inside the chip, with a frequency of 19.2MHz. After being divided by FREF_DIV, the reference clock f_{ref} is obtained. To ensure accurate measurement results, f_{ref} and fin must satisfy the following conditions:

$$f_{in} < \frac{f_{ref}}{4}$$

The following table presents the definitions of clock configuration-related registers.

Table 8.1 Clock Configuration Register Definitions

Clock	Register	Address	Bit	Instructions
f_{in}	DIV_CFG	0x1F	FINDIV[2:0]	000: Frequency division ratio $NDIV_{in}$=1 001: Frequency division ratio $NDIV_{in}$=2 010: Frequency division ratio $NDIV_{in}$=4 011: Frequency division ratio $NDIV_{in}$=8 100: Frequency division ratio $NDIV_{in}$=16 101: Frequency division ratio $NDIV_{in}$=32 110: Frequency division ratio NDV_{in}=64 111: Frequency division ratio

				$NDIV_{in}$=64
f_{ref}	DIV_CFG	0x1F	FREFDIV[1:0]	00: Frequency division ratio $NDIV_{ref}$=1 01: Frequency division ratio $NDIV_{ref}$=2 10: Frequency division ratio $NDIV_{ref}$=4 11: Frequency division ratio $NDIV_{ref}$=8

The relationship between clock signal f_{sensor} and f_{in}, f_{sys} and f_{ref} is shown in the following equation:

$$f_{in} = \frac{f_{sensor}}{NDIV_{in}} \quad (1)$$

$$f_{ref} = \frac{f_{sys}}{NDIV_{ref}} \quad (2)$$

It should be noted that f_{in} must ensure a frequency greater than 100KHz.

8.2 Capacitance Measurement

MCP1081 supports multi-channel and multi-mode capacitance measurement. By configuring the C_CMD register, capacitance measurement modes can be selected: single-ended measurement mode and dual-ended measurement mode. The single-ended measurement mode is suitable for capacitance measurements where one terminal is grounded. The dual-ended measurement mode is suitable for capacitance measurements where both terminals are floating.

Table 8.2 Selection of single-ended and dual-ended Measurement Modes

Register	Address	Bit	Instructions
C_CMD	0x1D	OSC_SEL	0: single-ended measurement mode 1: dual-ended measurement mode

8.3 Capacitance Measurement Mode

8.3.1 Single-Ended Ground Capacitance

To measure the single-ended to ground capacitance, connect the capacitor under test or electrode to any measurement channel of the chip, with the connection method as shown in the figure below. It is required to set OSC_SEL = 0, and select the measurement channel by configuring OSC1_CHS_M and OSC1_CHS_L. Measure the capacitance values of a total of 10 channels, ranging from measurement channel 0 to 9.

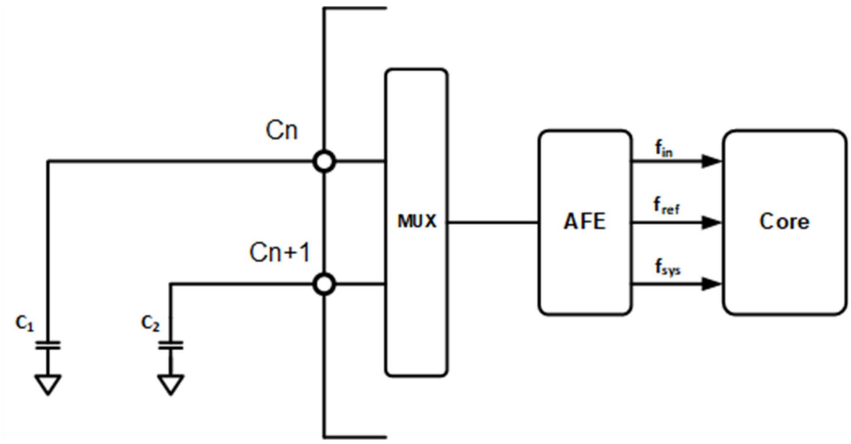


Figure 8.3.1 Measuring Single-ended Capacitance

8.3.2 Dual-ended Floating Capacitance

To measure the dual-ended floating capacitance, the dual-ended measurement mode can be selected. This method is insensitive to ground noise and has a fast measurement speed, making it suitable for situations where the measurement speed is fast and the ground plane interference is large. The connection method is shown in the following figure, where C_{p1} and C_{p2} are parasitic capacitors. Measurement requires configuring OSC_SEL=1 and selecting the measurement channel by configuring OSC2_CHS. There are a total of 5 measurement channels, and each group of double ended floating capacitors needs to occupy two single ended channels.

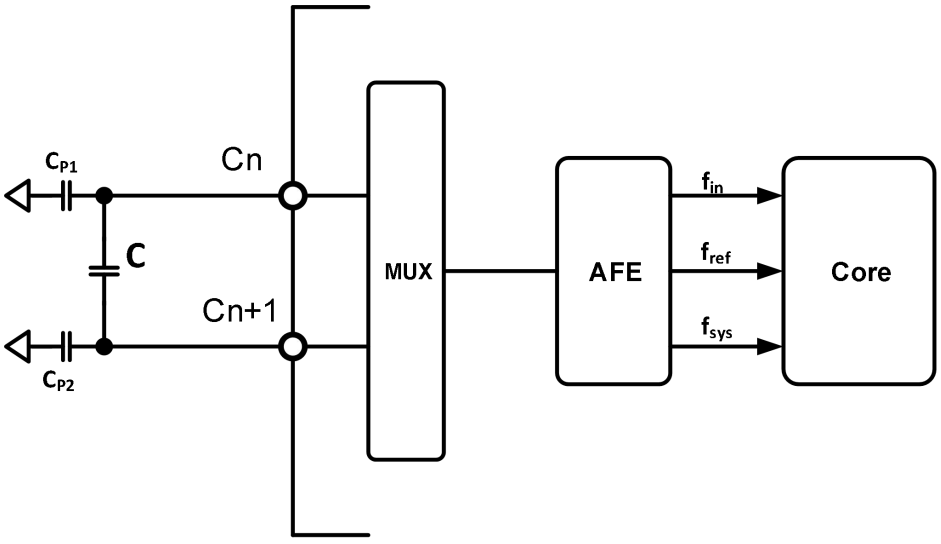


Figure 8.3.2 Measure dual-ended floating capacitance

8.3.3 Mutual Capacitance

Mutual capacitance can eliminate the parasitic capacitance of the channel to ground. Measuring mutual capacitance is based on the single ended measurement mode, and through internal control logic and calculation, the frequency count value reflecting the size of mutual capacitance C_M is obtained. The connection method of mutual capacitance is shown in the following figure, where the values of channel index n are 0, 2, 4, 6, and 8. C_{P1} and C_{P2} in the figure are parasitic capacitors. Measurement requires configuring OSC_SL=0 and selecting the measurement channel by configuring OSC1_CHS_M, OSC1_CHS_L, and OSC1_MCHS. There are a total of 5 measurement channels, and each group of mutual capacitors needs to occupy two single ended channels.

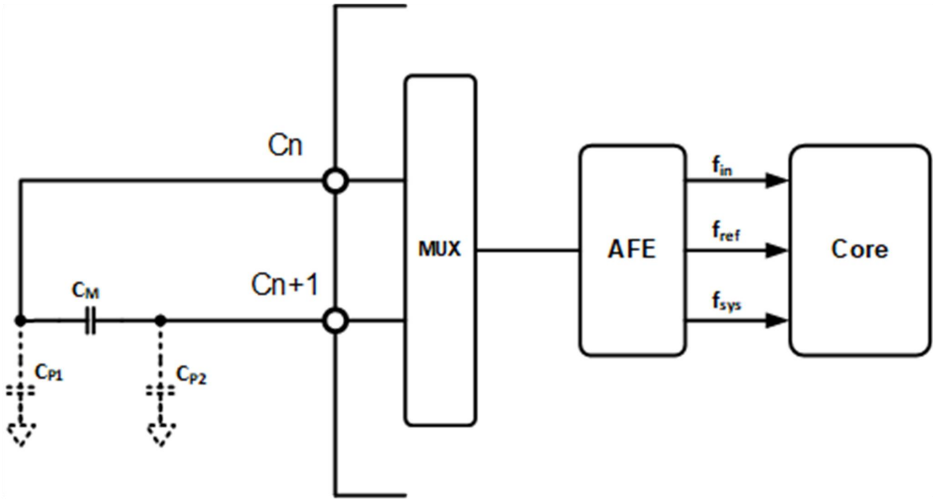
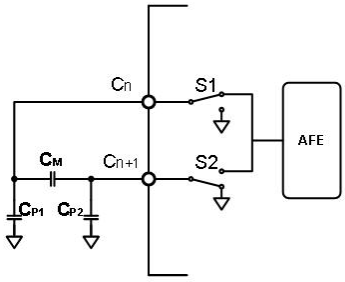
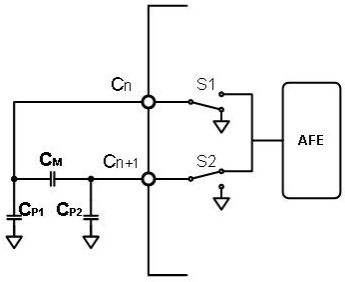


Figure 8.3.3-1 Measure mutual capacitance

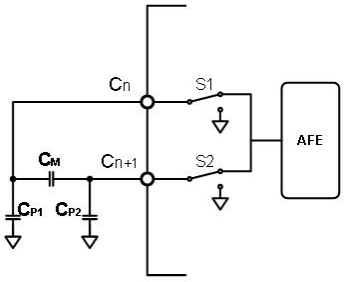
The specific procedure for mutual capacitance measurement is as follows, which is divided into three steps. Step 1 measures the capacitance value C1, Step 2 measures the capacitance value C2, and Step 3 measures the capacitance value C3. Then, through calculation, the mutual capacitance is derived as CM=(C1+C2−C3)/2. As can be seen, the port parasitic capacitances C_{P1} and C_{P2} are eliminated by the above method.



Step 1: Connect switch S1 to AFE, switch S2 to GND, and measure the capacitance to ground of Cn terminal C1=CM+CP1



Step 2: Connect switch S1 to GND, switch S2 to AFE, and measure the capacitance to ground of Cn+1 terminal C2=CM+CP2



Step 3: Connect switch S1 to AFE, switch S2 to AFE, measure the capacitance to ground of Cn and Cn+1 terminals

Figure 8.3.3-2 Steps for Measuring Mutual Capacitance

8.3.4 Capacitance Measurement Process

After determining the type of capacitor to be tested and determining the OSC_SEL configuration, the following steps need to be followed. Section 8.3 includes specific instructions.

i. Channel selection and pin configuration

ii. Drive strength and amplitude configuration

iii. Measurement and configuration conversion time

iv. Read data

v. Capacitance calculation

8.3.5 Single-ended Mode Channel Selection and Port Configuration

In single ended mode (OSC_SEL=0), MCP1081 has a total of 11 measurement channels, including 10 external channels corresponding to channels 0-9, and 1 internal reference channel corresponding to channel 10. Table 8.3.5-1 shows the configuration register description for single ended mode.

Table 8.3.5-1 Single-ended Mode Channel Selection Register

Channels and Corresponding Pins	Register	Address	Bit	Instructions
Channel10:Internal reference capacitor Cref	OSC1_CHS_MSB	0x20	CH_REF	0: Indicates no measurement of the internal reference channel 1: Indicates measurement of the internal reference channel
Channel 9: C9			CH9	0: Indicates no measurement of Channel 9 1: Indicates measurement of Channel 9
Channel 8: C8			CH8	0: Indicates no measurement of Channel 8 1: Indicates measurement of Channel 8
Channel 7: C7	OSC1_CHS_LSB	0x21	CH7	0: Indicates no measurement of Channel 7 1: Indicates measurement of

				Channel 7
Channel 6: C6			CH6	0: Indicates no measurement of Channel 6 1: Indicates measurement of Channel 6
Channel 5: C5			CH5	0: Indicates no measurement of Channel 5 1: Indicates measurement of Channel 5
Channel 4: C4			CH4	0: Indicates no measurement of Channel 4 1: Indicates measurement of Channel 4
Channel 3: C3			CH3	0: Indicates no measurement of Channel 3 1: Indicates measurement of Channel 3
Channel 2: C2			CH2	0: Indicates no measurement of Channel 2 1: Indicates measurement of Channel 2
Channel 1: C1			CH1	0: Indicates no measurement of Channel 1 1: Indicates measurement of Channel 1
Channel 0: C0			CH0	0: Indicates no measurement of Channel 0 1: Indicates measurement of Channel 0

MCP1081 also supports the measurement of mutual capacitance between channels. Table 8.3.5-2 provides a description of the grouping and configuration registers for mutual capacitance measurement channels.

Table 8.3.5-2 Mutual capacitance channel selection register

Channels and Corresponding Pins	Register	Address	Bit	Instructions
Channel 4: C8 and C9	OSC1_MCHS	0x22	MCH4	0: Indicates no measurement of the mutual capacitance between Channel 8 and Channel 9 1: Indicates measurement of the mutual capacitance between

				Channel 8 and Channel 9
Channel 3: C6 and C7			MCH3	0: Indicates no measurement of the mutual capacitance between Channel 6 and Channel 7 1: Indicates measurement of the mutual capacitance between Channel 6 and Channel 7
Channel 2: C4 and C5			MCH2	0: Indicates no measurement of the mutual capacitance between Channel 4 and Channel 5 1: Indicates measurement of the mutual capacitance between Channel 4 and Channel 5
Channel 1: C2 and C3			MCH1	0: Indicates no measurement of the mutual capacitance between Channel 2 and Channel 3 1: Indicates measurement of the mutual capacitance between Channel 2 and Channel 3
Channel 0: C0 and C1			MCH0	0: Indicates no measurement of the mutual capacitance between Channel 0 and Channel 1 1: Indicates measurement of the mutual capacitance between Channel 0 and Channel 1

When configuring mutual capacitance channels, the corresponding CHx and MCHx bits need to be set to 1. For example, when selecting measurement mutual capacitance channel 1, it is necessary to set CH2=1, CH3=1 and MCH1=1 simultaneously. The chip will automatically measure and provide data corresponding to the mutual capacitance C_M.

In single-ended mode, when the channel is not working, the connection method of its pins can be configured through registers, with three modes: high impedance, ground, and active shielding. The specific configurations are shown in the table below.

Table 8.3.5-3 Pin Configuration Register

Register	Address	Bit	Instructions
SHLD_CFG	0x26	CS[1:0]	00: Indicates that the capacitance measurement port is in a high impedance state during non measurement periods. 01: Indicates that the capacitance measurement port is grounded during non measurement periods. 1x: Indicates that the capacitance measurement port

			outputs an active shielding signal during non measurement periods, which is only valid when OSC_ESEL=0 and SHLD_IN=1.

8.3.6 Single-ended Mode Drive Strength and Amplitude Configuration

In single-ended mode, there are 9 configurations for driving strength, and the specific configurations and corresponding driving currents are shown in the table below.

Table 8.3.6-1 Single-ended Mode Driver Strength Configuration Register

Register	Address	Bit	Instructions
OSC1_CFG	0x23	OSC1_I[3:0]	0000: Drive current is 4uA 0001: Drive current is 8uA 0010: The driving current is 16uA 0011: The driving current is 42uA 0100: Drive current is 100uA 0101: Drive current is 250uA 0110: Drive current is 500uA 0111: Drive current is 1000uA 1xxx: Drive current is 2000uA

In single-ended mode, there are 8 configurations for oscillation amplitude: when high requirements are placed on power noise suppression, it is recommended to choose an amplitude configuration of 0.2V-1.2V, and the driving circuit will be powered by an internal LDO; When a large swing excitation drive is required, the configuration amplitude is related to the VDD voltage, as shown in the last four configurations in the table below. At this time, the internal LDO is turned off and the drive circuit is powered by VDD.

Table 8.3.6-2 Single ended mode oscillation amplitude configuration register

Register	Address	Bit	Instructions
OSC1_CFG	0x23	OSC1_LDO	Internal LDO power mode configuration 0: Low power mode, suitable for f_{sensor}<1MHz 1: High power mode, suitable for f_{sensor}>1MHz The above configuration is only valid when using internal LDO power supply

		OSC1_V[2:0]	000:The amplitude is 0.2V (internal LDO power supply) 001: The amplitude is 0.4V (internal LDO power supply) 010: The amplitude is 0.8V (internal LDO power supply) 011: The amplitude is 1.2V (internal LDO power supply) 100: The amplitude is VDD-2.2V (VDD power supply) 101: The amplitude is VDD-1.6V (VDD power supply) 110: The amplitude is VDD-1.2V (VDD power supply) 111: The amplitude is VDD-0.8V (powered by VDD)

8.3.7 Dual-ended Mode Channel Selection and Port Configuration

In dual-ended mode (OSC_SL=1), a dual-ended channel is formed between adjacent capacitance measurement pins of MCP1081. Among them, there are 5 external channels corresponding to channels 0-4, and 1 internal reference channel corresponding to channel 5. The configuration registers are shown in the table below.

Table 8.3.7-1 dual-ended Mode Channel Selection Register

Channels and Corresponding Pins	Register	Address	Bit	Instructions
Channel 5: Internal Reference capacitor CREF	OSC2_DCHS	0x24	DCH_REF	0: Indicates no measurement of the internal reference channel 1: Indicates measurement of the internal reference channel
Channel 4: C8 and C9			DCH4	0: Indicates no measurement of dual channel 4 1: Indicates measurement of dual channel 4
Channel 3: C6 and C7			DCH3	0: Indicates no measurement of dual channel 3 1: Indicates measurement of dual channel 3
Channel 2: C4 and C5			DCH2	0: Indicates no measurement of dual channel 2

				1: Indicates measurement of dual channel 2
Channel 1: C2 and C3			DCH1	0: Indicates no measurement of dual channel 1 1: Indicates measurement of dual channel 1
Channel 0: C0 and C1			DCH0	0: Indicates no measurement of dual channel 0 1: Indicates measurement of dual channel 0

In dual-ended mode, when the channel is not working, the connection method of its pins can be configured through registers. There are two modes: high impedance and ground, and active shielding function is not supported. The specific configuration is shown in the table below.

Table 8.3.7-2 Pin Configuration Register

register	address	Bit	Instructions
SHLD_CFG	0x26	CS[1:0]	00: Indicates that the non measurement channel is in a high impedance state 01: Indicates non measurement channel internal grounding 1x: Invalid (OSC_SEL=1)

8.3.8 Dual-ended Mode Drive Strength and Amplitude Configuration

In dual-ended mode, there are 9 configurations for driving strength, and the specific configurations and corresponding driving currents are shown in the table below.

Table 8.3.8-1 Dual-ended Mode Driver Strength Configuration Register

Register	Address	Bit	Instructions
OSC2_CFG	0x25	OSC2_I[3:0]	0000: Drive current is 4uA 0001: Drive current is 8uA 0010: The driving current is 16uA 0011: The driving current is 42uA 0100: Drive current is 100uA 0101: Drive current is 250uA 0110: Drive current is 500uA 0111: Drive current is 1000uA 1xxx: Drive current is 2000uA

In dual-ended mode, there are 6 configurations for differential oscillation amplitude, all of which will activate the internal LDO of the chip. The specific configurations are shown in the table below.

Table 8.3.8-2 Dual-ended mode oscillation amplitude configuration register

Register	Address	Bit	Instructions
OSC2_CFG	0x25	OSC2_LDO	Internal LDO power mode configuration 0: Low powermode,suitable for f_{sensor}<1MHz 1: High power mode, suitable for f_{sensor}>1MHz
		OSC2_V[2:0]	Dual-ended mode oscillation amplitude configuration 000: The amplitude is 0.4V 001: The amplitude is 0.8V 010: The amplitude is 1.2V 011: The amplitude is 1.6V 100: The amplitude is 2.0V 101: The amplitude is 2.4V 110: The amplitude is 2.4V 111: The amplitude is 2.4V

8.4 Measurement and Conversion Time

MCP1081 supports multi-channel measurement. During a measurement process, all selected channels will be measured sequentially. The measurement modes include single measurement and periodic measurement. The repetition interval of periodic measurement can be configured, which are continuous without interval, 100ms、 1s, and 10s. For periodic measurement mode, if the user modifies the parameters during the measurement period, it will not take effect immediately. They need to first send a stop measurement and then restart the periodic measurement for the new parameters to take effect.

In order to improve measurement accuracy, the function of averaging multiple measurement data is supported, with options of 1, 4, 8, and 32 averages available. In sleep mode (SLEEP_EN=1), the chip enters sleep mode after executing I2C instructions or completing measurements to reduce power consumption. The specific configuration instructions are shown in the table below.

Table 8.4-1 Capacitance Measurement Control Register

Register	Address	Bit	Position Definition	Instructions
C_CMD	0x1D	7	OSC_SEL	Selection of oscillation mode 0: Select single-ended mode;

				1: Choose dual-ended mode
		5	SLEEP_EN	Chip sleep mode switch 0: Sleep mode is turned off; 1: Sleep mode enabled
		5:4	CAVG[1:0]	Frequency count value Dx average number of times 00: 1 time 01: 4 times 10: 8 times 11: 32 times
		3:2	CR[1:0]	Configuration of cycle conversion interval time 00:10s interval measurements 01:1s interval measurements 10: 0.1s interval measurements 11: Continuous and uninterrupted measurement, without any interval
		1:0	OS，SD	Capacitor conversion start position 00: Cycle conversion 10: Cycle conversion 01: Stop Conversion 11: Single conversion

The conversion time for each channel of MCP1081 is determined by the register CNT_CFG. The value of FINCNT is N, indicating the total duration of measuring N cycles of the f_{in} signal. If you want to increase the total measurement time, you can increase the FINCNT value or FINDIV frequency division value. SETTLING represents the initial establishment time of the channel, and signals within this time period are not included in the frequency count value. The specific configuration instructions are shown in the table below.

Table 8.4-2 Measurement cycle number and establishment time configuration register

Register	Address	Bit	Position Definition	Instructions
CNT_CFG	0x1E	7:0	FINCNT[7:0]	Set the number of measurement cycles N for f_{in} 0x00: Measure the duration of one fin cycle 0x01~0xFF: Measure the duration of N fin cycles, N=1~255

DIV_CFG	0x1F	7	SETTLING	Set the number of establishment cycles for f_{in} 0: represents the establishment time of one f_{in} cycle 1: Indicating the establishment time of 4 f_{in} cycles

The following figure shows the workflow of a measurement, taking single ended mode and selecting channel 0, channel 1, and channel 4 as an example.

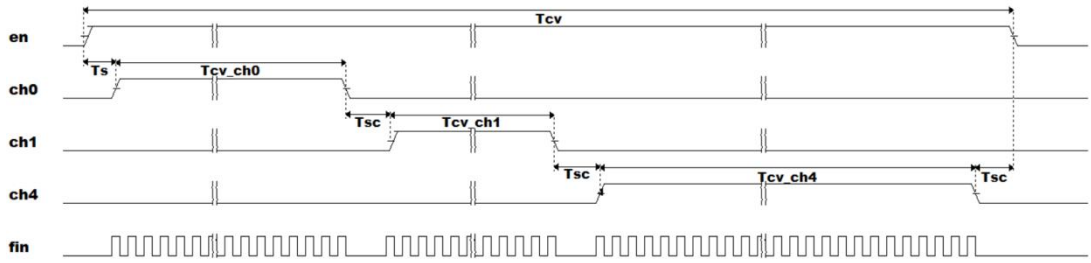


Figure 8.4-1 Measurement Workflow

In the above figure, the en signal represents the en$_{ab}$le of the capacitive sensor. When the measurement starts, the en signal is raised; When the measurement is completed and the en signal is pulled low, the total conversion time is T_{cv}. After en is pulled high, the oscillation circuit is established with a time of T_s (=50us). Afterwards, channel 0 is selected and its conversion time is T_{cv_ch0}. After the channel is completed, switch to channel 1, and the switching time between channels is T_{sc} (=5us). After channel 1 is selected, its conversion time is T_{cv_ch1}. After completing channel 1, switch to channel 4, with a switching time of T_{sc} and a conversion time of T_{cd_ch4}, respectively. After completing channel 4, pass through T_{sc} to complete the entire measurement process. Adding one channel x increases the total conversion time (T_{cc_chx}+T_{cc}). The expression for the total conversion time T_{cv} is:

$$T_{cv} = T_s + \left(T_{cv\_ch1} + T_{sc}\right) + \left(T_{cv\_ch2} + T_{sc}\right) + \left(T_{cv\_ch4} + T_{sc}\right) \quad (3)$$

$$T_{cv\_chx} = \frac{FIN\_CNT * C\_AVG + N_S}{f_{inx}} = \frac{(FREF\_DIV * D_X) * \left(C\_AVG + \frac{N_S}{FIN\_CNT}\right)}{f_{sys}} \quad (4)$$

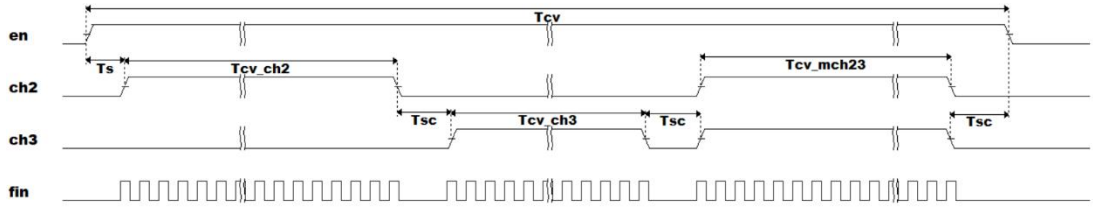
In equation (4):

- FIN_CNT is the number of measurement cycles for fin, as shown in Table 8.4-2 for measurement cycle numbers and establishment time configuration registers;
- C_AVG is the average number of internal sampling times, as shown in Table

8.4-1 for capacitance measurement control registers;

- N_s is the number of establishment cycles for fin, which can be set to 1 or 4 according to SETTLING settings;
- FREF_DIV is the system clock division coefficient, please refer to Table 8.1 Clock Configuration Register for details;
- D_x is the frequency count value read from each channel data register (x represents the selected channel), as shown in Table 8.7 Data Register for details;
- F_{inx} is the oscillation frequency of channel x after being divided by FIN-DIN;
- F_{sys} is the internal system clock of the chip, with a frequency of 19.2MHz.

The timing of measuring the mutual capacitance of MCP1081 is divided into 3 steps. Taking the mutual capacitance between channels 2-3 as an example, as shown in



the following figure:

Figure 8.4-2 Workflow of Mutual Capacitance Measurement

The first step is to measure channel 2, with a conversion time of T_{cv_ch2};The second step is to measure channel 3, with a conversion time of T_{cv_ch3}; The third step is to measure channels 2 and 3 simultaneously, with a conversion time of T_{cv_mch23}. Ts is the establishment time of the oscillation circuit, and T_{sc} is the channel switching time. The expression for the total conversion time T_{cv} is:

$$T_{cv} = T_s + \left(T_{cv\_ch2} + T_{sc}\right) + \left(T_{cv\_ch3} + T_{sc}\right) + \left(T_{cv\_mch23} + T_{sc}\right) \qquad (5)$$

In equation (5):

The calculation of T_{cv_chx} is detailed in formula (4).

8.5 Status and Overflow

The status register is used to query the current working status of the chip. When it is in the process of capacitor conversion and temperature conversion, the relevant flag position is 1. The chip also has data overflow protection function. Due to the upper limit of the DATA register value being 65535, when the frequency of the f_{in} is low and the FINCNT value is large, there may be a situation of count overflow. It is possible to determine whether data has overflowed by checking the overflow flag register. Clear the data overflow flag by writing 1 to the OF_CEAR bit of the status

register. The relevant registers are shown in the table below.

Table 8.5-1 Overflow Flag Bit Register

Register	Address	Bit	Instructions
OSC1_OF_MSB	0x18	MOF[4:0] OFREF OF[9:8]	MOFX: 1 represents mutual capacitance channel x count overflow, with x values ranging from 0 to 4 OFREF: 1 indicates overflow of single ended reference channel count OFx: 1 represents a single ended channel x count overflow, with x values ranging from 0 to 9
OSC1_OF_LSB	0x19	OF[7:0]	OFx: 1 represents a single ended channel x count overflow, with x values ranging from 0 to 7
OSC2_OF	0x1A	DOFREF DOF[4:0]	DOFREF: 1 indicates overflow of dual end reference channel count DOFx: 1 indicates overflow of the double ended channel x count, with x values ranging from 0 to 4

Table 8.5-2 Status Register

Register	Address	Bit	Instructions
STATUS	0x1B	OF_CLEAR	Writing 1 to this bit will clear all overflow flag bits. The read value is 0.
		FLAG_TCVT	1 indicates that temperature conversion is in progress. 0 indicates stopping temperature conversion.
		FLAG_CCVT	1 indicates that capacitance conversion is in progress. In cycle mode, this flag remains high until a stop command is issued. 0 indicates stopping capacitor conversion.

8.6 Clock Configuration

The registers related to MCP1081 clock configuration include CNT_CFG and DIV_CFG. The configuration process is as follows:

i. According to the application requirements, confirm the conversion time T_{cv}. Generally speaking, the longer the conversion time, the higher the measurement accuracy. It is also possible to reduce noise levels and improve effective resolution by increasing the average frequency.

ii. Estimate the oscillation frequency f_{sensor} based on the maximum value of the measured capacitance, circuit connection method, oscillation method, driving strength, and oscillation amplitude (due to the influence of non ideal factors, the estimated value may differ from the measured frequency value). The

estimation formula for the oscillation frequency f_{sensor} is as follows:

$$T_{half} = K_r \cdot (C + C_p) \cdot ln\left(\frac{v_{drv}+v_{amp}}{v_{drv}-v_{amp}}\right) + 8 \times 10^{-9} \quad (6)$$

$$f_{sensor} = 1/2T_{half} \quad (7)$$

In equations (6) and (7):

- T_{half} is the oscillation half cycle;
- C is the estimated measured capacitance value;
- C_p is the equivalent parasitic capacitance of the chip IO, generally estimated at 6pF;
- The values of driving voltage amplitude V_{drv}, oscillation amplitude V_{amp}, and current coefficient K_r are related to the configuration.

As shown inthe table below, OSC1_VTH [2:0] and OSC_2VTH [2:0] represent the amplitude configuration of the oscillation register.

Single ended mode: OSC_SEL=0			**Dual ended mode: OSC_SEL=1**		
OSC1_VTH[2:0]	V_{amp}	V_{drv}	OSC2_VTH[2:0]	V_{amp}	V_{drv}
000	0.2	2	000	0.2	2
001	0.4	2	001	0.4	2
010	0.8	2	010	0.6	2
011	1.2	2	011	0.8	2
100	VDD-2.2	VDD	100	1.0	2
101	VDD-1.6	VDD	101	1.2	2
110	VDD-1.2	VDD	110	1.2	2
111	VDD-0.8	VDD	111	1.2	2

Note: VDD is the power supply voltage of the chip.

I[3:0]	K_r	drive current
0000	2.56e5	4uA
0001	1.28e5	8uA
0010	6.4e4	16uA
0011	2.4e4	42uA
0100	1e4	100uA
0101	4e3	250uA
0110	2e3	500uA
0111	1e3	1000uA
1xxx	5e2	2000uA

iii. Due to the upper limit of the count value for DATA being 65535, $FINCNT_{MAX}$ can

be estimated using the following equation after determining $NDIV_{in}$, $NDIV_{Ref}$, and f_{sensor}. Generally, FINCNT=0.5·$FINCNT_{MAX}$ is taken. Taking 0.5 times here is to leave design margin for the influence of non ideal factors such as parasitism and temperature drift. In order to achieve high accuracy, the data average frequency C_AVG can also be configured to be 32.

$$FINCNT_{MAX} = (FREF\_DIV \cdot Dx \cdot f_{sensorx}) / (FIN\_DIV \cdot f_{sys}) \quad (8)$$

In equation (8):

- $FINCNT_{MAX}$ is the maximum value of the number of measurement cycles for f_{in};
- FREF_DIV is the system clock division ratio, please refer to Table 8.1 Clock Configuration Register for details;
- FIN_DIV is the frequency division ratio of the measured signal.

iv. If the conversion time is limited, it is generally set to $NDIV_{ref}$=1, C_AVG=1, and the measured signal establishment configuration SETTLING=0. $FINCNT_{MAX}$ can be estimated using the following equation. Generally, FINCNT=0.5 $FINCNT_{MAX}$ is taken. Note that T_{cvchx} in the following equation is only the conversion time of a single channel, not the total duration Tcv. The calculation of T_{cv_chx} is shown in formula (4).

$$FINCNT_{MAX} = \left(T_{cv_{chx}} \cdot f_{sensorx}\right) / NDIV_{in} - N_s, \quad N_s = 1 \quad (9)$$

In equation (9),

N_s is the number of cycles established for the measured signal. Please refer to Table 8.4-2 for the measurement cycle number and establishment time configuration register.

SETTLING is the configuration for establishing the measured signal, and N_s is the number of cycles for establishing the measured signal, as described in section 8.4.

v. Based on the results of iii and iv, select FINCNT with smaller values. Simultaneously determine parameters such as $NDIV_{in}$, $NDIV_{ref}$, SETTLING, and CAVG.

vi. If measuring mutual capacitance, three measurements are required. When setting FINCNT, select the minimum value. The measurement duration of a mutual capacitance channel is the sum of three measurements.

8.7 Data Reading and Capacitance Calculation

The data for each channel is shown in the table below.

Table 8.7 Data Register

Register	Address	Bit	Instructions		
			Single-Ended (OSC_SEL=0)	Mutual capacitance (OSC_SEL=0)	Bilateral (OSC_SEL=1)
D0_MSB D0_LSB	0x02 0x03	DATA[15:8] DATA[7:0]	Channel CH0 data		Channel DCH0 data
D1_MSB D1_LSB	0x04 0x05	DATA[15:8] DATA[7:0]	Channel CH1 data	Channel MCH0 data	Channel DCH1 data
D2_MSB D2_LSB	0x06 0x07	DATA[15:8] DATA[7:0]	Channel CH2 data		Channel DCH2 data
D3_MSB D3_LSB	0x08 0x09	DATA[15:8] DATA[7:0]	Channel CH3 data	Channel MCH1 data	Channel DCH3 data
D4_MSB D4_LSB	0x0A 0x0B	DATA[15:8] DATA[7:0]	Channel CH4 data		Channel DCH4 data
D5_MSB D5_LSB	0x0C 0x0D	DATA[15:8] DATA[7:0]	Channel CH5 data	Channel MCH2 data	invalid
D6_MSB D6_LSB	0x0E 0x0F	DATA[15:8] DATA[7:0]	Channel CH6 data		invalid
D7_MSB D7_LSB	0x10 0x11	DATA[15:8] DATA[7:0]	Channel CH7 data	Channel MCH3 data	invalid
D8_MSB D8_LSB	0x12 0x13	DATA[15:8] DATA[7:0]	Channel CH8 data		invalid
D9_MSB D9_LSB	0x14 0x15	DATA[15:8] DATA[7:0]	Channel CH9 data	Channel MCH4 data	invalid
DREF_MSB DREF_LSB	0x16 0x17	DATA[15:8] DATA[7:0]	Channel CHREF data		Channel CHREF data

It should be noted that in single ended mode, when mutual capacitance measurement is enabled, the valid data representing MCHx are located in registers D1, D3, D5, D7, and D9, respectively; In dual ended mode, the valid data representing DCHx are located in D0, D1, D2, D3, D4, and DREF registers.

The data read from the table above is the count value of the channel, and the corresponding frequency conversion formula is as follows.

$$f_{sensorx} = \left(FIN\_DIV \cdot f_{sys} \cdot FIN\_CNT\right) / \left(FREF\_DIV \cdot Dx\right) \quad (10)$$

In equation (10):

- FIN_DIV is the internal frequency division coefficient for measuring the oscillation frequency of the measurement channel, as shown in Table 8.1 Clock Configuration Register;

- f_{sys} is the internal system clock of the chip, with a frequency of 19.2MHz;

- FIN_CNT i_s $_t$he number of measurement cycles for fin, as shown in Table 8.4-2 for measurement cycle numbers and establishment time configuration registers;

- FREF_DIV is the system clock division coefficient, please refer to Table 8.1 Clock Configuration Register for details;

- D_x is the frequency count value read from the data registers of each channel (x represents the selected channel, applicable to single ended capacitors, mutual capacitors, and double ended capacitors), as shown in Table 8.7 for data registers.

In order to read the correct data in a single measurement, it is necessary to read the data after the conversion is completed. For a single measurement, the completion of the current measurement can be determined by checking the FLAG_CCVT bit of the status register. For periodic and continuous measurements, the chip will measure at fixed intervals on its own, and users only need to read the data at the appropriate time.

In practical applications, the method of reference measurement is adopted to eliminate the influence of non ideal factors such as drift. This method requires that the configuration of the measurement channel and the reference channel be the same. For the selection of reference channels, please refer to section 8.8.

The specific measurement and calculation method is as follows:

Method 1: Use an internal reference capacitor channel (applicable to single ended capacitors, mutual capacitors, and double ended capacitors)

i. Measure and read the frequency count value D_x of channel x

ii. Measure and read the frequency count value DREF of the internal reference channel under the same configuration

iii. Calculate the capacitance value C_x according to the following formula. The internal reference capacitance C_{ref} is 20pF.

$$C_x = \left(C_{ref} \cdot Dx\right) / DREF \qquad (11)$$

Method 2: Use an external reference capacitor (suitable for single ended capacitors and mutual capacitors)

i. Select one channel (such as single-ended channel CH7, corresponding to

pin C7), connect the reference capacitor C_{ref} externally, and connect the other channels to electrodes or the measured capacitor. The size of the external reference capacitor should be as close as possible to the measured capacitor.

ii. Measure and read the frequency count value Dx of channel x

iii. Measure and read the frequency count value D7 of channel CH7

iv. Calculate the capacitance value according to the following formula

$$C_x = (C_{ref} \cdot Dx)/D7$$

Method 3: Use an external reference capacitor (suitable for dual-ended capacitors)

i. Select one channel (such as dual-ended channel DCH3, corresponding to pins C6 and C7), connect the reference capacitor C_{ref} externally, and connect the other channels to electrodes or the measured capacitor. The size of the external reference capacitor should be as close as possible to the measured capacitor.

ii. Measure and read the frequency count value Dx of channel x

iii. Measure and read the frequency count value D3 of channel DCH3

iv. Calculate the capacitance value according to the following formula

$$C_x = (C_{ref} \cdot Dx)/D3$$

Method 4: Use two external reference capacitors (applicable to single ended capacitors and mutual capacitors)

i. Select a channel (such as single-ended channel CH6, corresponding to pin C6) and connect an external reference capacitor C_{ref1}; Select the second channel (e.g. single ended channel CH7, corresponding to pin C7), connect the reference capacitor C_{ref2} externally, and connect the other channels to the electrodes or the measured capacitor. Require $C_{ref1}=2 * C_{ref2}$. The size of the external reference capacitor C_{ref1} should be as close as possible to the measured capacitance.

ii. Measure and calculate the period of channel x $T_{sensorx} = 1/f_{sensorx}$

iii. Measure and calculate the period of reference channel CH6 $T_{cref1} = 1/f_{sensor6}$

iv. Measure and calculate the period of reference channel CH7 $T_{cref2} = 1/f_{sensor7}$

v. Calculate time correction parameters,$T_{fix} = 2T_{cref2} - T_{cref1}$

vi. Adjust the period of reference channel CH6, $T_{cref1\_fix} = T_{cref1} - T_{fix}$

vii. Adjust the cycle of the measurement channel $T_{sensorx\_fix} = T_{sensorx} - T_{fix}$

viii. Calculate the capacitance value according to the following formula

$$C_x = \left(C_{ref1} \cdot T_{sensorx\_fix}\right) / T_{cref1\_fix}$$

Method 5: Use two external reference capacitors (applicable to dual-ended capacitors)

i. Select one channel (such as dual-ended channel DCH3, corresponding to pins C6 and C7) and connect an external reference capacitor C_{ref1}; Select the second channel (such as the dual-ended channel DCH4, corresponding to pins C8 and C9), connect the reference capacitor C_{ref2} externally, and connect the other channels to the electrodes or the measured capacitor. Require C_{ref1}=2 * C_{ref2}. The size of the external reference capacitor C_{ref1} should be as close as possible to the measured capacitance.

ii. Measure and calculate the period of channel x $T_{sensorx} = 1/f_{sensorx}$

iii. Measure and calculate the period of the reference channel DCH3 $T_{cref1} = 1/f_{sensor3}$

iv. Measure and calculate the period of the reference channel DCH4 $T_{cref2} = 1/f_{sensor4}$

v. Calculate time correction parameters $T_{fix} = 2T_{cref2} - T_{cref1}$

vi. Adjust the period of reference channel DCH3 $T_{cref1\_fix} = T_{cref1} - T_{fix}$

vii. Adjust the cycle of the measurement channel $T_{sensorx\_fix} = T_{sensorx} - T_{fix}$

viii. Calculate the capacitance value according to the following formula

$$C_x = \left(C_{ref1} \cdot T_{sensorx\_fix}\right) / T_{cref1\_fix}$$

Among the above 5 methods, methods 1, 2, and 4 are applicable to single ended capacitors and mutual capacitors; Methods 1, 3, and 5 are applicable to double ended capacitors. Methods 1, 2, and 3 will be affected by parasitic capacitance. Methods 4 and 5 have the highest measurement accuracy.

8.8 Selection of Reference Capacitor

The reference capacitor of MCP1081 can be either an internal capacitor, an external capacitor, or an electrode structure.

For general application scenarios, the built-in 20pf capacitor Cref can be chosen as the reference capacitor, and in this case, all 10 external single ended or 5 dual

ended capacitors can be used for measurement.

For applications that require the elimination of temperature drift, external capacitors or electrode structures can be chosen as references. For single ended, it is recommended to choose channel CH7 as the reference channel. For both ends, it is recommended to choose channel DCH3 as the reference channel.

For applications that require high-precision measurement, two external capacitors can be selected as references. For single ended, it is recommended to choose channels CH6 and CH7 as reference channels. For both ends, it is recommended to choose channels DCH3 and DCH4 as reference channels.

8.9 Active Shielding

MCP1081 provides active shielding function, which can eliminate the influence of peripheral parasitic capacitance. Because when the tested electrode is at the same potential as the surrounding shielding layer, there is no charge movement between them, and parasitic capacitance has no effect on the tested electrode. As shown in Figure 6.3.3-1, cap1 is the tested electrode, and cap0, cap2, and the metal layer (shield) constitute the active shielding layer. The shield driving circuit (BUF) is formed by the unit gain operational amplifier inside the chip. The SHLD, C_n, and C_{n+2} pins output the same waveform, that is, Vcap1=Vshield=Vcap0=Vcap2. This can effectively resist the interference problem on the electrode surface without affecting the sensitivity of the electrode.

Configure SHLD_CFG register bit CS [1:0]=1X, and SHLD_EN=1 to enable active shielding function. If the capacitance load of the shielding electrode is relatively large, SHLD_HP=1 can be configured to enable high-power driving mode.

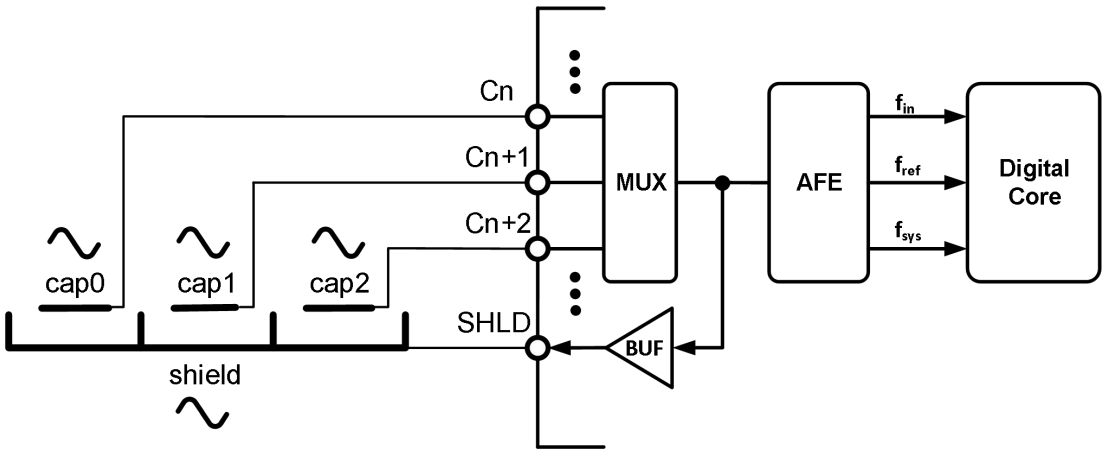


Figure 8.9 Active shielding function

When using the active shielding function, there are the following precautions:

i. The active shielding function can only be activated in single ended capacitor mode. Mutual capacitance and double ended capacitance do not support

active shielding function.

ii. The maximum signal frequency supported by active shielding is f_{sensor}=500KHz.

iii. Active shield driving is divided into high-power mode and low-power mode, with differences in the maximum capacitance and minimum resistance load that can be driven.

The register for configuring active shielding is SHLD_CFG, and the specific register description is shown in the table below.

Table 8.9 Active Shielding Configuration Register

Register	Address	Bit	Instructions
SHLD_CFG	0x26	CS[1:0]	Status bit of capacitance measurement port during non measurement period 00: Indicates that the capacitance measurement port is in a high resistance state during non measurement periods 01: Indicates that the capacitance measurement port is grounded during non measurement periods 1x: Indicates that the capacitance measurement port outputs an active shielding signal during non measurement periods
		SHLD_HP	0: indicates low-power mode, driving a maximum load of 30pF 1: Indicates high-power mode, driving a maximum load of 60pF
		SHLD_EN	0: Turn off active shielding 1: Activate active shielding

8.10 Temperature Measurement

MCP1081 includes high-precision temperature sensing function, with a temperature measurement range of -40 ℃ ~+85 ℃ , and a temperature measurement accuracy of ± 2 ℃ over the entire temperature range. The temperature value can be used for temperature drift compensation in capacitive sensing channels.

8.10.1 Temperature Measurement Parameter Configuration

The chip generates a voltage signal proportional to temperature internally, which is converted by a 16 bit ADC and output to the temperature data register. By configuring the STC position 1 of the temperature measurement register, a

temperature conversion process can be initiated; By configuring the TCV bit, the time for a single temperature conversion can be set, and the longer the conversion time, the higher the effective resolution. The temperature conversion process and the capacitance conversion process operate independently of each other and do not interfere with each other. The description of the temperature measurement configuration register is as follows:

Table 8.10-1 Temperature Measurement Configuration Register

Register	Address	Bit	Instructions
T_CMD	0x1C	TCV	Temperature conversion time configuration bit 0：3.0ms， Effective resolution 0.02 ℃ 1：1.7ms， Effective resolution 0.03 ℃
		STC	Temperature conversion start position 0: Stop conversion 1: Start a single conversion and read a value of 0

8.10.2 Temperature Data Format and Calculation Formula

The format of temperature data is a 16 bit signed number with TLSB=0.0039 ℃. The register description is as follows:

Table 8.10-2 Temperature Data Register

Register	Address	Bit	Instructions
T_MSB T_LSB	0x0 0x1	TDATA[15:8] TDATA[7:0]	Temperature data, 16 bit signed number

The calculation formula for temperature value is:

$$Temperature = \frac{TDATA[15:0]}{255} + 28.7℃$$

8.11 Power Consumption Mode

MCP1081 has three power consumption states: standby mode, working mode, and sleep mode.

When powered on, MCP1081 will automatically configure the registers to default values and enter standby mode. At this time, the internal power supply and system clock of the chip are in the on state, waiting for the user to send parameter configuration and measurement conversion instructions through I2C.

MCP1081 will automatically enter sleep mode after each I2C read/write operation. At this time, the internal power supply and system clock of the chip are turned off, which is the lowest power consumption mode.

When the host issues a valid I2C command, the chip will automatically wake up and perform the corresponding operation, entering the working mode. It should be noted that in cycle measurement mode, MCP1081 will enter standby mode after each conversion and will not enter sleep mode.

8.12 Software Reset

MCP1081 provides software reset function (Softreset). By writing 0x7A to the reset register, the software reset function is activated, the sensor is restored to its initial power on state, and all registers are restored to their default values.

Table 8.12 Definition of Reset Register

Register	Address	Bit	Instructions
RESET	0x69	RESET[7:0]	B01110100: Start software reset, sensors return to their initial power on state, and all registers return to their default values. Other values: Invalid. The read value is 0x00.

9. functional mode

9.1 Power on start-up

After power on, MCP1081 enters standby mode and can perform operations including parameter modification, single conversion, and cycle conversion.

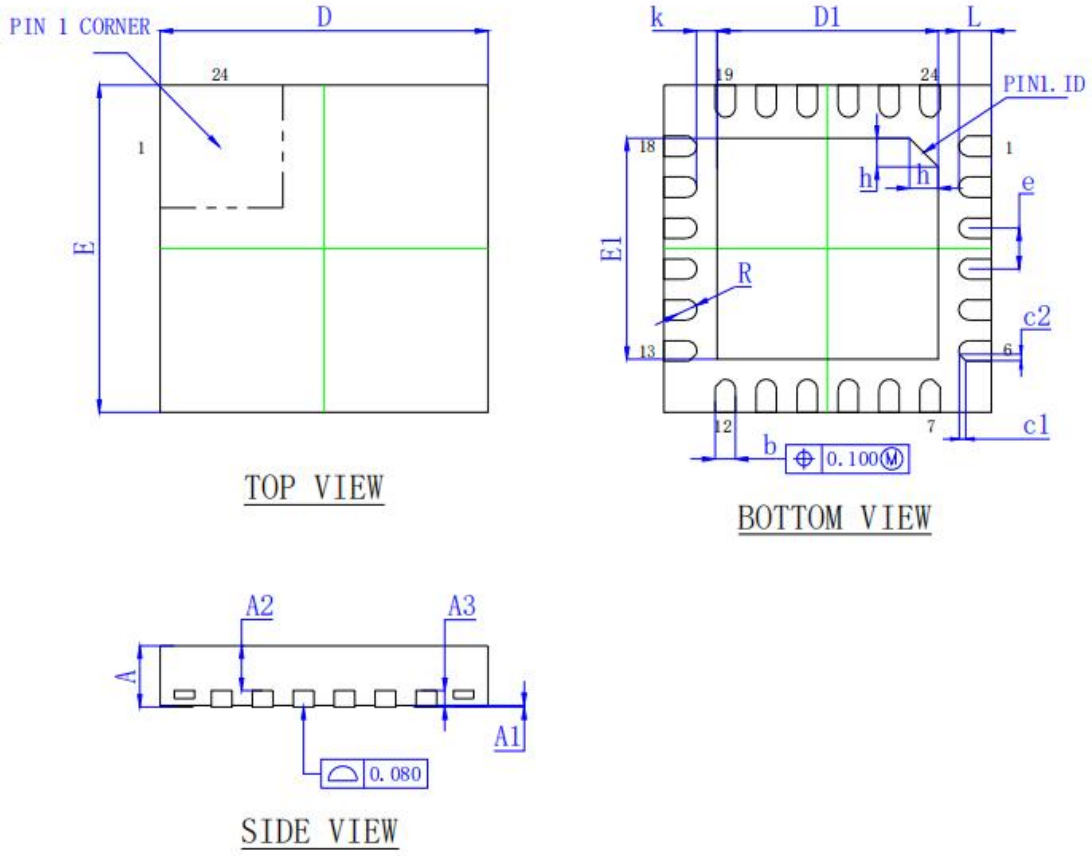
9.2 Conversion Mode

The conversion modes of MCP1081 are divided into single conversion mode and periodic conversion mode, which are configured through CFG registers. Please refer to section 8.4 for details.

9.3 Sleep Mode

MCP1081 will automatically enter sleep mode (low-power mode) after each I2C instruction operation. When the host issues a valid I2C command, the chip will automatically wake up and perform the corresponding operation.

10. Package



Symbol	DIMENSION In Millimeters (MM)			DIMENSION In Inches		
	Min.	Normal	Max.	Min.	Normal	Max.
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	--	0.020	0.050	--	0.001	0.002
A2	--	0.550	--	--	0.022	—
A3	0.203 REF			0.008 REF		
D	3.900	4.000	4.100	0.154	0.157	0.161
E	3.900	4.000	4.100	0.154	0.157	0.161
D1	2.600	2.700	2.800	0.102	0.106	0.110
E1	2.600	2.700	2.800	0.102	0.106	0.110
b	0.200	0.250	0.300	0.008	0.010	0.012
L	0.350	0.400	0.450	0.014	0.016	0.018
e	0.500 BSC			0.020 BSC		
k	0.200	---	---	0.008	---	---
R	0.090	---	---	0.004	---	---
c1	---	0.080	---	---	0.003	---
c2	---	0.080	---	---	0.003	---
h	0.350 REF			0.014 REF		

Figure 10 MCP1081S QFN24 4.0 * 4.0 * 0.75mm product size specification diagram

11. Ordering Information

Part Number	Package Type	Package Qty
MCP1081S	QFN24	5000