钍地半导体
Tudi Semiconductor

Product Specification

TUDI- 93AA56AT-I/SN

2-Kbit Microwire Compatible Serial EEPROM

网址 www.sztdbdt.com

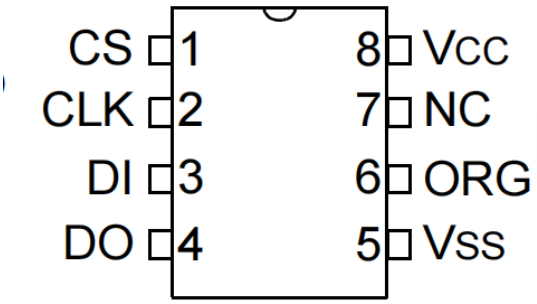
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

●Low-Power CMOS Technology
●ORG Pin to Select Word Size for 56C'Version
●256×8-bit Organization ‘ A'Version(no ORG)
●128×16-bit Organization 'B'Version(no ORG)
●Sel-Timed EraseWrite Cycles(including Auto-Erase)
●Automatic Erase All(ERAL)before Write All (WRAL)
●Power-On/Off Data Protection Circuitry
●Industry Standard Three-Wire Seria I/O
●Device Status Signal(Ready/Busy)
●Sequential Read Function
●·High Reliability:
-Endurance:1,000,000 erase/write cycles
-Data retention:>200 years
-ESD protection:>4000V
●RoHS Compliant:
●Automotive AEC-Q100 Qualified
●Temperature Ranges Supported:
-Industrial(I)-40℃ to+85℃
-Extended(E)-40℃ to+125℃



SOP8

Description

The Microchip Technology Inc.93XX56A/B/C devicesare 2-Kbit low-voltage serial Electrically ErasablePROMs(EEPROM).Word-selectable devices such asthe 93AA56C,93LC56C or 93C56C are dependentupon external logic levels driving the ORG pin to setword size.For dedicated 8-bit communication,the93XX56A devices are available,while the 93XX56Bdevices provide dedicated 16-bit communication.Advanced CMOS technology makes these devicesideal for low-power, nonvolatile memory applications.

Pin Function Table

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VSS	Ground
NC	No internal connection
ORG	Memory Configuration
VCC	Power Supply

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC.....7.0V

All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-40°C to +125°C

ESD protection on all pins .....≥ 4 kV

†NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

All parameters apply over the specified ranges unless otherwise noted.			Industrial (I): T_A = -40°C to +85°C, V_{CC} = +1.8V to +5.5V Extended (E): T_A = -40°C to +125°C, V_{CC} = +2.5V to +5.5V				
Param. No.	**Symbol**	**Parameter**	**Minimum**	**Typical**	**Maximum**	**Units**	**Conditions**
D1	$V_{IH}1$	High-level Input Voltage	2.0	—	V_{CC} +1	V	$V_{CC} \geq$ 2.7V
	$V_{IH}2$		0.7 V_{CC}	—	V_{CC} +1	V	V_{CC} < 2.7V
D2	$V_{IL}1$	Low-level Input Voltage	-0.3	—	0.8	V	$V_{CC} \geq$ 2.7V
	$V_{IL}2$		-0.3	—	0.2 V_{CC}	V	V_{CC} < 2.7V
D3	Vol1	Low-level Output Voltage	—	—	0.4	V	I_{OL} = 2.1 mA, V_{CC} = 4.5V
	Vol2		—	—	0.2	V	I_{OL} = 100 µA, V_{CC} = 2.5V
D4	$V_{OH}1$	High-level Output Voltage	2.4	—	—	V	I_{OH} = -400 µA, V_{CC} = 4.5V
	$V_{OH}2$		V_{CC} - 0.2	—	—	V	I_{OH} = -100 µA, V_{CC} = 2.5V
D5	I_{LI}	Input Leakage Current	—	—	±1	µA	V_{IN} = V_{SS} or V_{CC}
D6	I_{LO}	Output Leakage Current	—	—	±1	µA	V_{OUT} = V_{SS} or V_{CC}
D7	C_{IN}, C_{OUT}	Pin Capacitance (all inputs/outputs)	—	—	7	pF	V_{IN}/V_{OUT} = 0V **(Note 1)** T_A = +25°C, F_{CLK} = 1 MHz
D8	I_{CC} write	Write Current	—	—	2	mA	F_{CLK} = 3 MHz, Vcc = 5.5V F_{CLK} = 2 MHz, Vcc = 2.5V
			—	500	—	µA	
D9	I_{CC} read	Read Current	—	—	1	mA	F_{CLK} = 3 MHz, V_{CC} = 5.5V
			—	—	500	µA	F_{CLK} = 2 MHz, V_{CC} = 3.0V
			—	100	—	µA	F_{CLK} = 2 MHz, V_{CC} = 2.5V
D10	I_{CCS}	Standby Current	—	—	1	µA	I – Temp CLK = CS = 0V ORG = DI = V_{SS} or V_{CC} **(Note 2) (Note 3)**
			—	—	5	µA	E – Temp CLK = CS = 0V ORG = DI = V_{SS} or V_{CC} **(Note 2) (Note 3)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: ORG pin not available on 'A' or 'B' versions.

3: Ready/$\overline{\text{Busy}}$ status must be cleared from DO; see **Section 3.4 "Data Out (DO)"**.

TABLE 1-1: DC CHARACTERISTICS

All parameters apply over the specified ranges unless otherwise noted.			Industrial (I): TA = -40°C to +85°C, VCC = +1.8V to +5.5V Extended (E): TA = -40°C to +125°C, VCC = +2.5V to +5.5V				
Param. No.	**Symbol**	**Parameter**	**Minimum**	**Typical**	**Maximum**	**Units**	**Conditions**
D11	VPOR	VCC Voltage Detect	—	1.5	—	V	93AA56A/B/C,93LC56A/B/C **(Note 1)**
			—	3.8	—	V	93C56A/B/C**(Note 1)**

Note 1: This parameter is periodically sampled and not 100% tested.
2: ORG pin not available on 'A' or 'B' versions.
3: Ready/$\overline{\text{Busy}}$ status must be cleared from DO; see **Section 3.4 "Data Out (DO)"**.

TABLE 1-2: AC CHARACTERISTICS

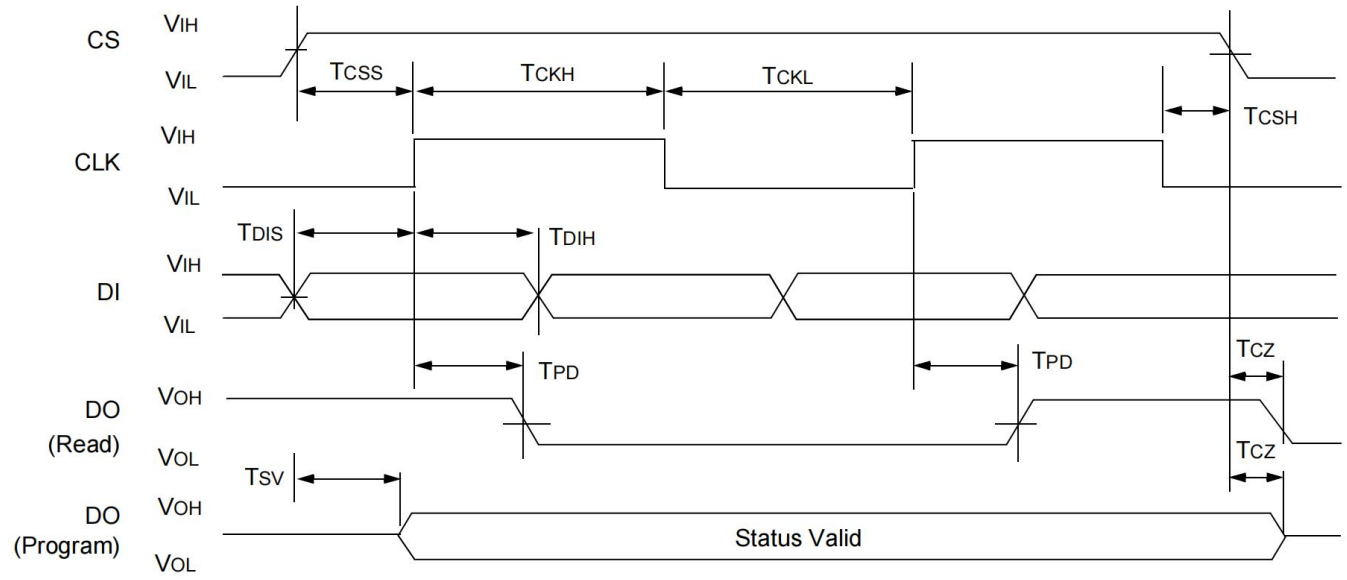
All parameters apply over the specified ranges unless otherwise noted.			Industrial (I): TA = -40°C to +85°C, VCC = +1.8V TO +5.5V Extended (E): TA = -40°C to +125°C, VCC = +2.5V TO +5.5V			
Param. No.	**Symbol**	**Parameter**	**Minimum**	**Maximum**	**Units**	**Conditions**
A1	FCLK	Clock frequency	—	3	MHz	4.5V ≤ VCC < 5.5V, 93XX56C only
			—	2	MHz	2.5V ≤ VCC < 5.5V
			—	1	MHz	1.8V ≤ VCC < 2.5V
A2	TCKH	Clock high time	200	—	ns	4.5V ≤ VCC < 5.5V, 93XX56C only
			250	—	ns	2.5V ≤ VCC < 5.5V
			450	—	ns	1.8V ≤ VCC < 2.5V
A3	TCKL	Clock low time	100	—	ns	4.5V ≤ VCC < 5.5V, 93XX56C only
			200	—	ns	2.5V ≤ VCC < 5.5V
			450	—	ns	1.8V ≤ VCC < 2.5V
A4	TCSS	Chip Select setup time	50	—	ns	4.5V ≤ VCC < 5.5V
			100	—	ns	2.5V ≤ VCC < 4.5V
			250	—	ns	1.8V ≤ VCC < 2.5V
A5	TCSH	Chip Select hold time	0	—	ns	1.8V ≤ VCC < 5.5V
A6	TCSL	Chip Select low time	250	—	ns	1.8V ≤ VCC < 5.5V
A7	TDIS	Data input setup time	50	—	ns	4.5V ≤ VCC < 5.5V, 93XX56C only
			100	—	ns	2.5V ≤ VCC < 5.5V
			250	—	ns	1.8V ≤ VCC < 2.5V
A8	TDIH	Data input hold time	50	—	ns	4.5V ≤ VCC < 5.5V, 93XX56C only
			100	—	ns	2.5V ≤ VCC < 5.5V
			250	—	ns	1.8V ≤ VCC < 2.5V
A9	TPD	Data output delay time	—	200	ns	4.5V ≤ VCC < 5.5V, CL = 100 pF
			—	250	ns	2.5V ≤ VCC < 4.5V, CL = 100 pF
			—	400	ns	1.8V ≤ VCC < 2.5V, CL = 100 pF
A10	TCZ	Data output disable time	—	100	ns	4.5V ≤ VCC < 5.5V, **(Note 1)**
			—	200	ns	1.8V ≤ VCC < 4.5V, **(Note 1)**
A11	TSV	Status valid time	—	200	ns	4.5V ≤ VCC < 5.5V, CL = 100 pF
			—	300	ns	2.5V ≤ VCC < 4.5V, CL = 100 pF
			—	500	ns	1.8V ≤ VCC < 2.5V, CL = 100 pF

All parameters apply over the specified ranges unless otherwise noted.			Industrial (I): TA = -40°C to +85°C, VCC = +1.8V TO +5.5V Extended (E): TA = -40°C to +125°C, VCC = +2.5V TO +5.5V			
Param. No.	**Symbol**	**Parameter**	**Minimum**	**Maximum**	**Units**	**Conditions**
A12	TWC	Program cycle time	—	6	ms	Erase/Write mode (AA and LC versions)
A13	TWC		—	2	ms	Erase/Write mode (93C versions)
A14	TEC		—	6	ms	ERAL mode, 4.5V ≤ VCC ≤ 5.5V
A15	TWL		—	15	ms	WRAL mode, 4.5V ≤ VCC ≤ 5.5V
A16		Endurance	1M	—	cycles	+25°C, VCC = 5.0V, **(Note 2)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but ensured by characterization.

FIGURE 1-1: SYNCHRONOUS DATA TIMING



Note 1: TSV is relative to CS.

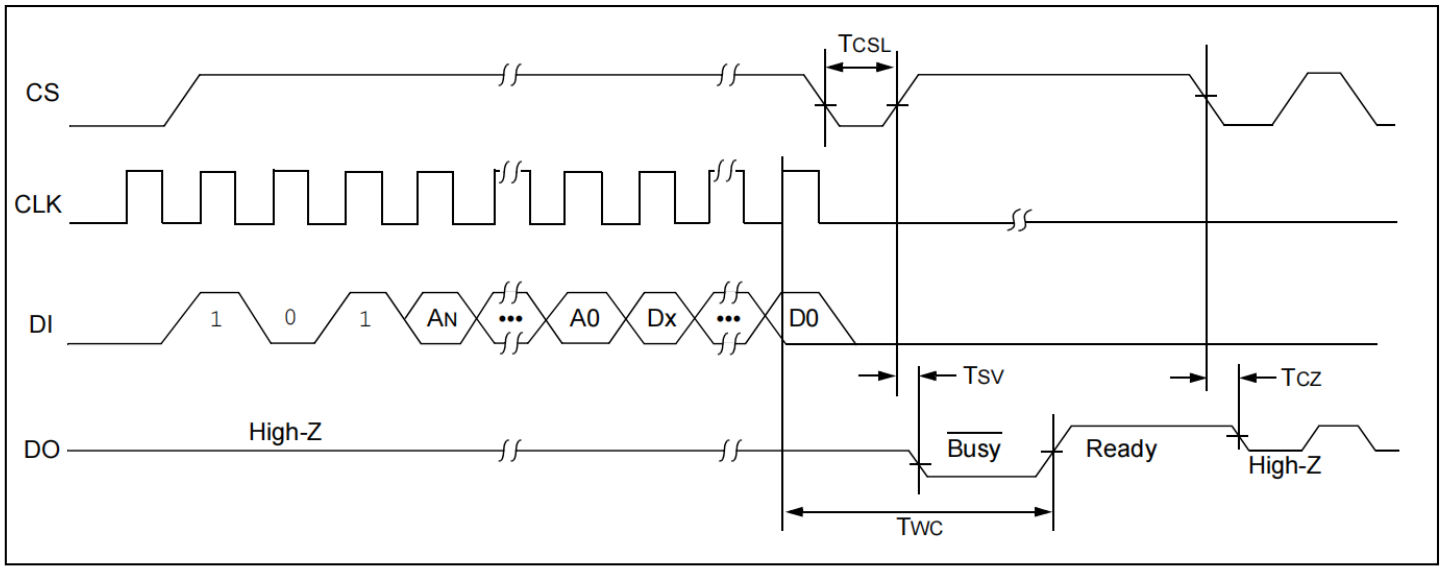
TABLE 1-3: INSTRUCTION SET FOR X16 ORGANIZATION (93XX56B OR 93XX56C WITH ORG = 1)

Instruction	SB	Opcode	Address								Data In	Data Out	Req. CLK Cycles
ERASE	1	11	X	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00	1	0	X	X	X	X	X	X	—	(RDY/$\overline{BSY}$)	11
EWDS	1	00	0	0	X	X	X	X	X	X	—	High-Z	11
EWEN	1	00	1	1	X	X	X	X	X	X	—	High-Z	11
READ	1	10	X	A6	A5	A4	A3	A2	A1	A0	—	D15 – D0	27
WRITE	1	01	X	A6	A5	A4	A3	A2	A1	A0	D15 – D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00	0	1	X	X	X	X	X	X	D15 – D0	(RDY/$\overline{BSY}$)	27

TABLE 1-4: INSTRUCTION SET FOR X8 ORGANIZATION (93XX56A OR 93XX56C WITH ORG = 0)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
ERASE	1	11	X A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	12
ERAL	1	00	1 0 X X X X X X X	—	(RDY/$\overline{BSY}$)	12
EWDS	1	00	0 0 X X X X X X X	—	High-Z	12
EWEN	1	00	1 1 X X X X X X X	—	High-Z	12
READ	1	10	X A7 A6 A5 A4 A3 A2 A1 A0	—	D7 – D0	20
WRITE	1	01	X A7 A6 A5 A4 A3 A2 A1 A0	D7 – D0	(RDY/$\overline{BSY}$)	20
WRAL	1	00	0 1 X X X X X X X	D7 – D0	(RDY/$\overline{BSY}$)	20

FIGURE 2-9: WRITE TIMING FOR 93C DEVICES



2.0 FUNCTIONAL DESCRIPTION

When the ORG pin (93XX56C) pin is connected to VCC, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a High-Z state except when reading data from the device, or when checking the Ready/Busy status during a programming operation. The Ready/Busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. DO will enter the High-Z state on the falling edge of CS.

2.1 Start Condition

The Start bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a Start condition is detected, CS, CLK and DI may change in any combination (except to that of a Start condition), without resulting in any device operation (Read, Write, Erase, EWEN, EWDS, ERAL or WRAL). As soon as CS is high, the device is no longer in Standby mode.

An instruction following a Start condition will only be executed if the required opcode, address and data bits for any particular instruction are clocked in.

Note:	When preparing to transmit an instruction, either the CLK or DI signal levels must be at a logic low as CS is toggled active high.

2.2 Data In/Data Out (DI/DO)

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a “bus conflict” to occur during the “dummy zero” that precedes the read operation if A0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin. In order to limit this current, a resistor should be connected between DI and DO.

2.3 Data Protection

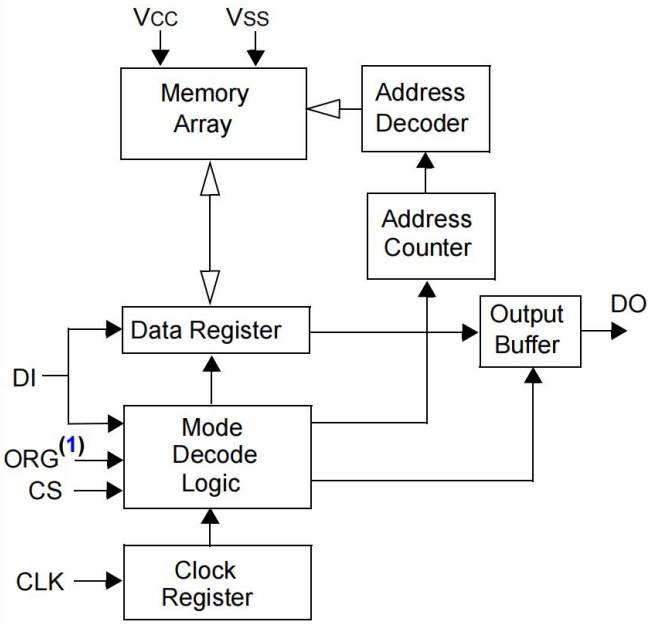
All modes of operation are inhibited when VCC is below a typical voltage of 1.5V for ‘93AA’ and ‘93LC’ devices or 3.8V for ‘93C’ devices.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

Note:	For added protection, an EWDS command should be performed after every write operation and an external 10 kΩ pull-down protection resistor should be added to the CS pin.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before the initial ERASE or WRITE instruction can be executed.

Block Diagram



Note 1: ORG input is not available on A/B devices.

2.4 Erase

The ERASE instruction forces all data bits of the specified address to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle, except on '93C' devices where the rising edge of CLK before the last address bit initiates the write cycle.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical '0' indicates that programming is still in progress. DO at logical '1' indicates that the register at the specified address has been erased and the device is ready for another instruction.

Note:	After the Erase cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/$\overline{\text{Busy}}$ status from DO.

FIGURE 2-1: ERASE TIMING FOR 93AA AND 93LC DEVICES

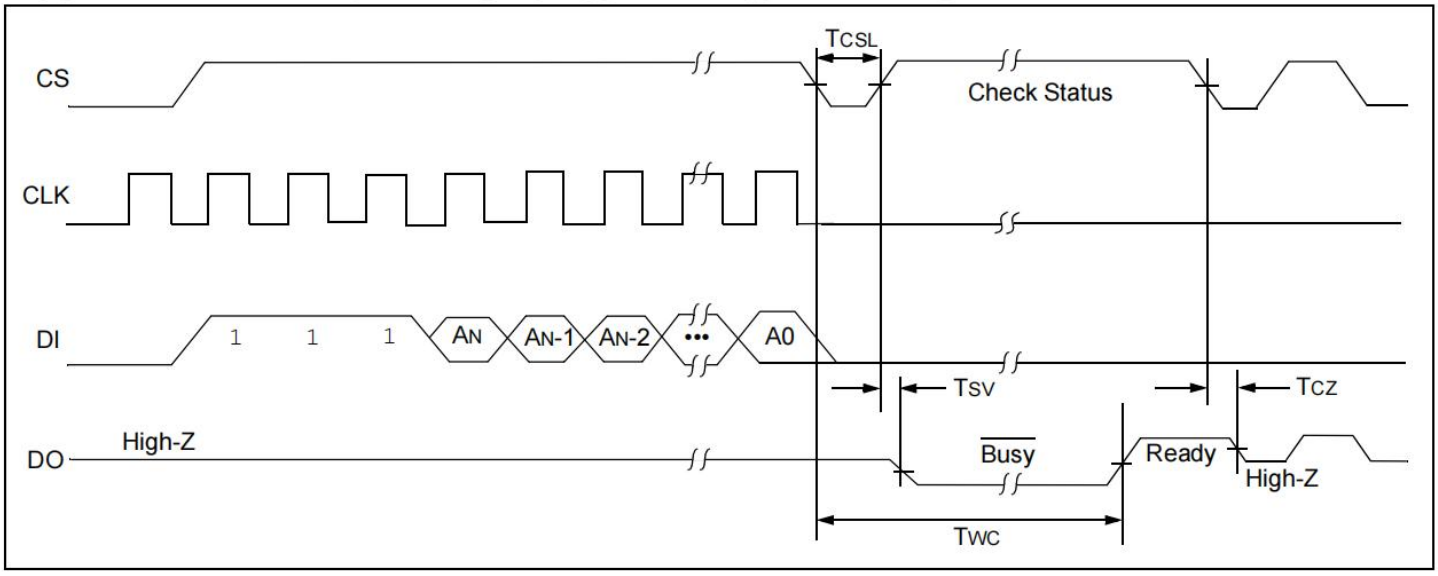
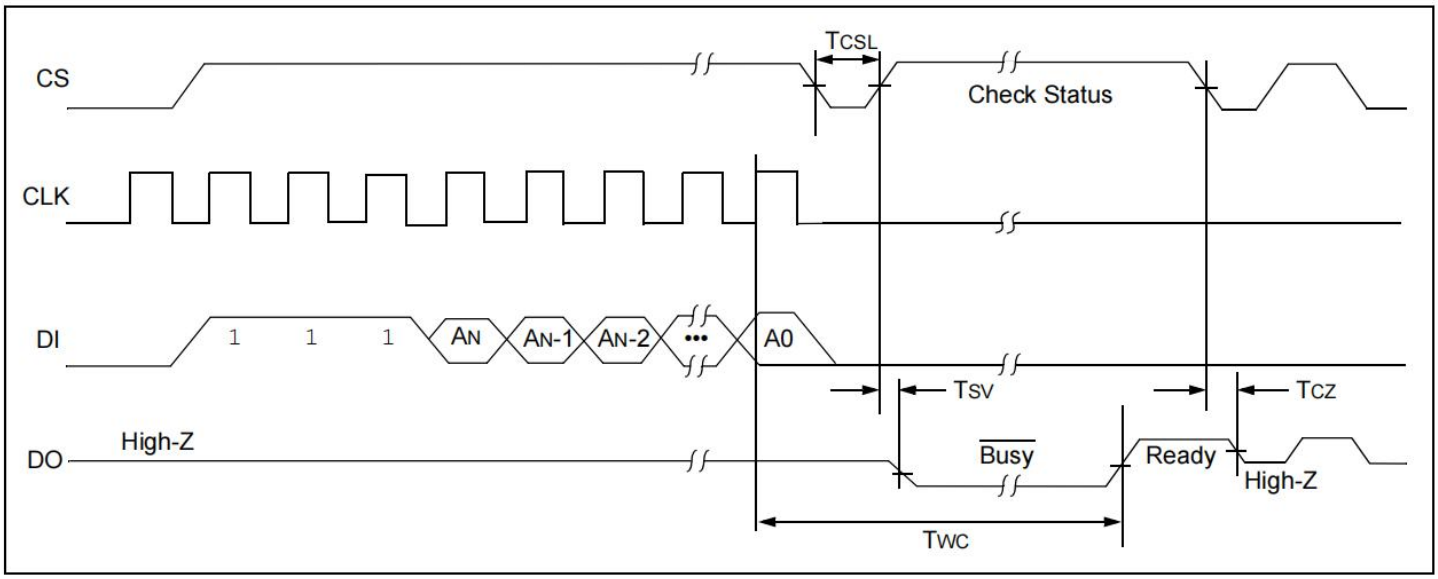


FIGURE 2-2: ERASE TIMING FOR 93C DEVICES



2.5 Erase All (ERAL)

The Erase All (ERAL) instruction will erase the entire memory array to the logical '1' state. The ERAL cycle is identical to the erase cycle, except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS, except on '93C' devices where the rising edge of CLK before the last data bit initiates the write cycle. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device, if CS is brought high after a minimum of 250 ns low (TCSL).

Note:	After the ERAL command is complete, issuing a Start bit and then taking CS low will clear the Ready/$\overline{\text{Busy}}$ status from DO.

VCC must be ≥4.5V for proper operation of ERAL.

FIGURE 2-3: ERAL TIMING FOR 93AA AND 93LC DEVICES

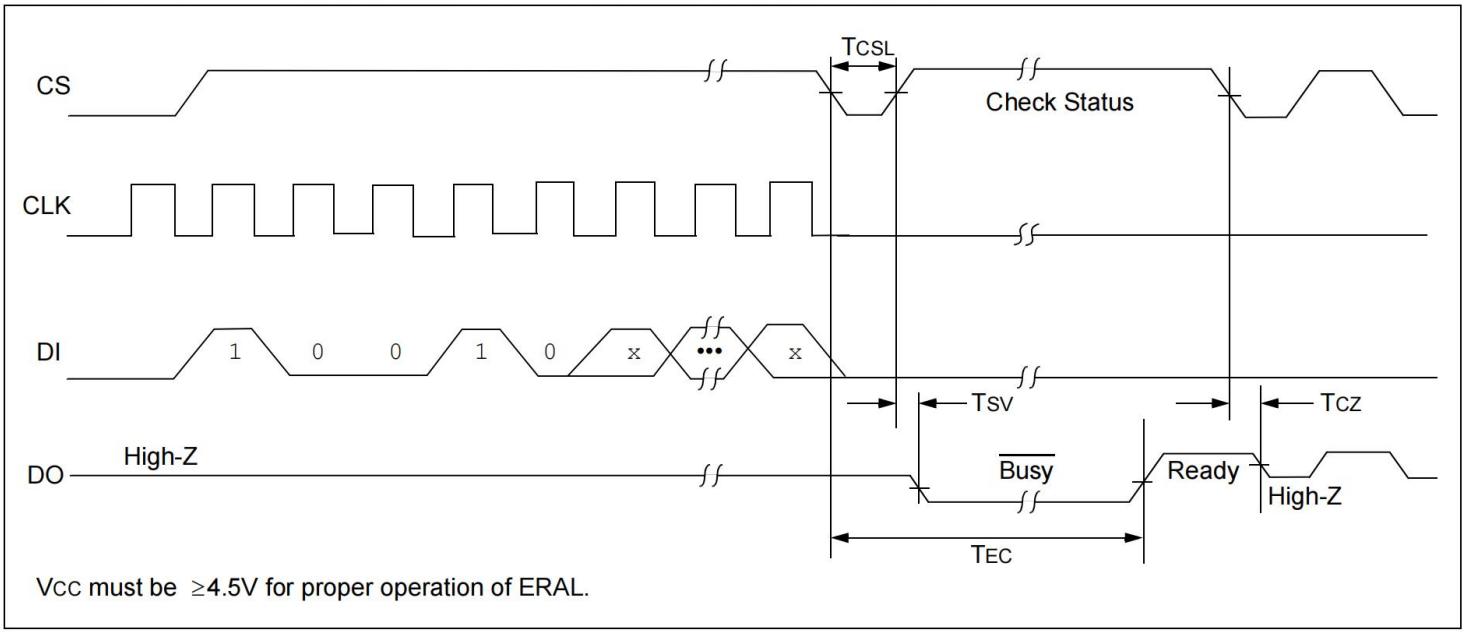
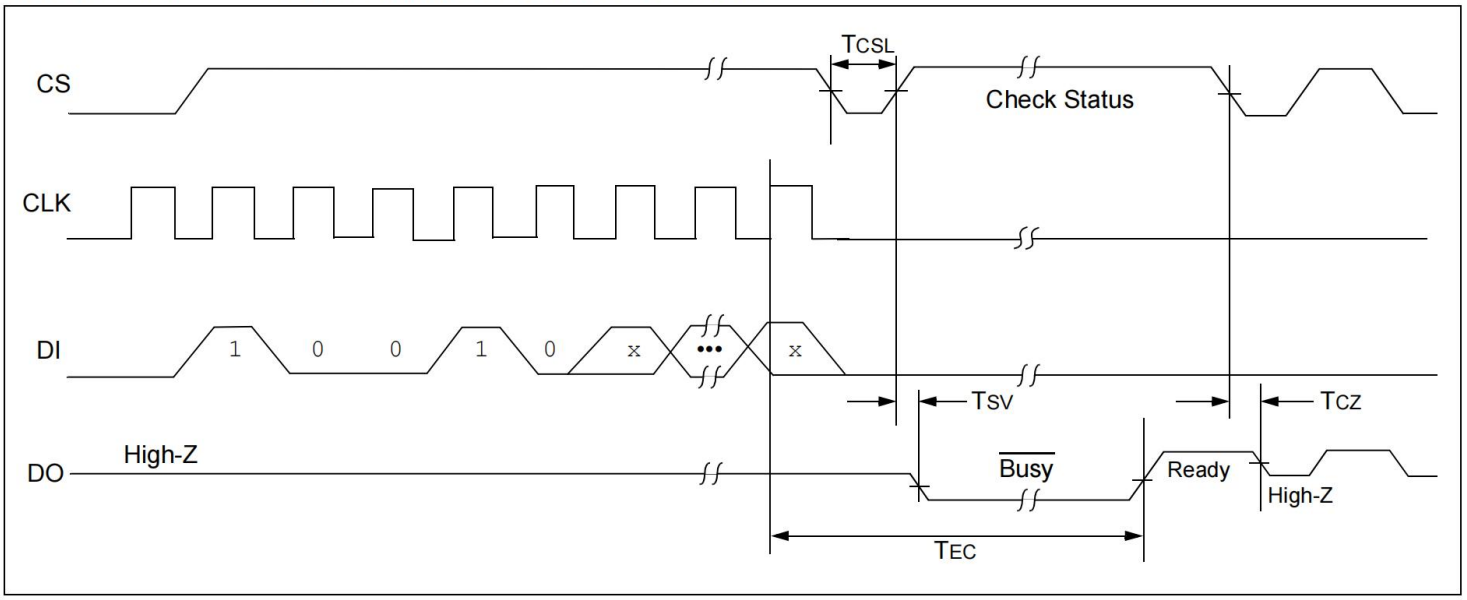


FIGURE 2-4: ERAL TIMING FOR 93C DEVICES



2.6 Erase/Write Disable and Enable (EWDS/EWEN)

The 93XX56A/B/C powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction.

Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device.

To protect against accidental data disturbance, the EWDS instruction can be used to disable all erase/write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

FIGURE 2-5: EWDS TIMING

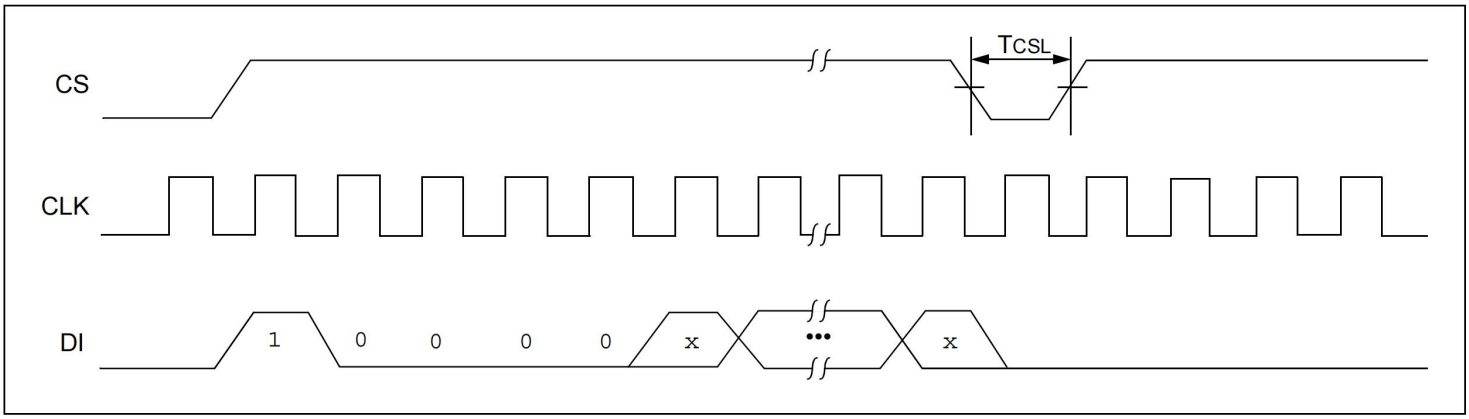
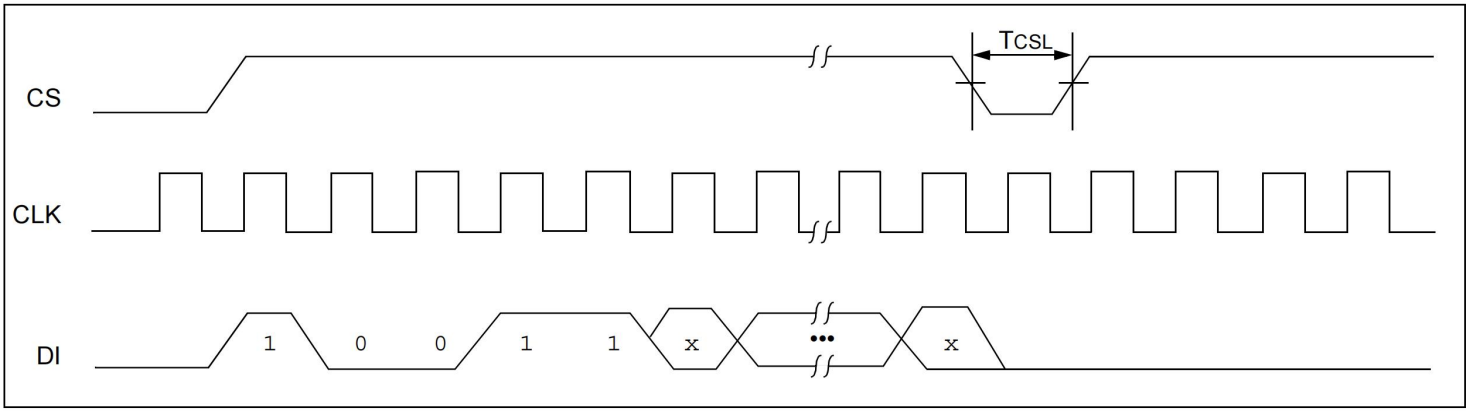


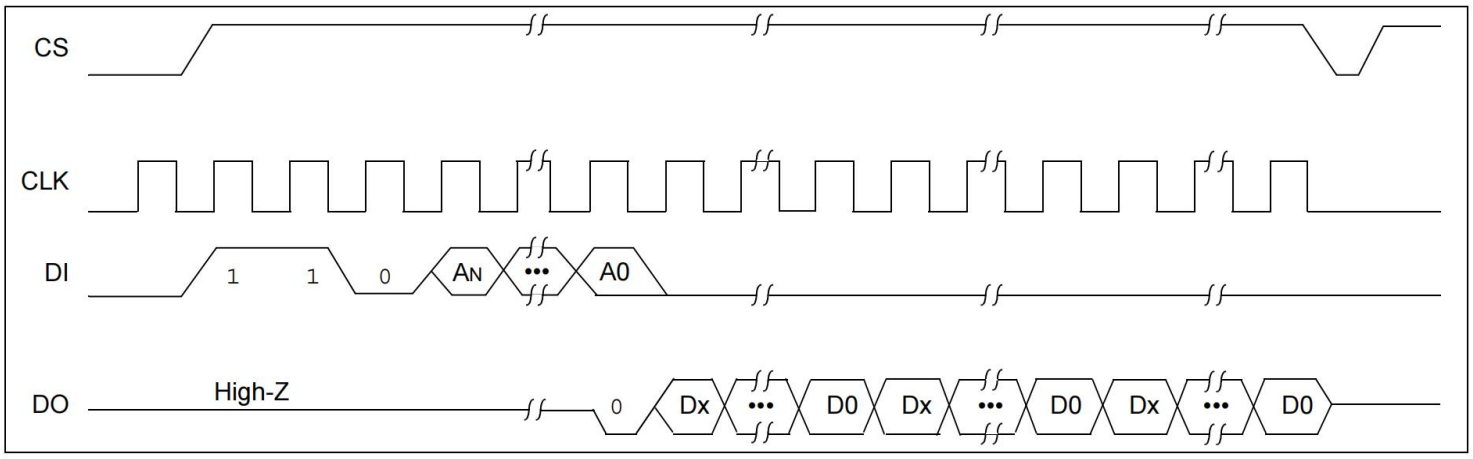
FIGURE 2-6: EWEN TIMING



2.7 Read

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit (if ORG pin is low or A-version devices) or 16-bit (if ORG pin is high or B-version devices) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

FIGURE 2-7: READ TIMING



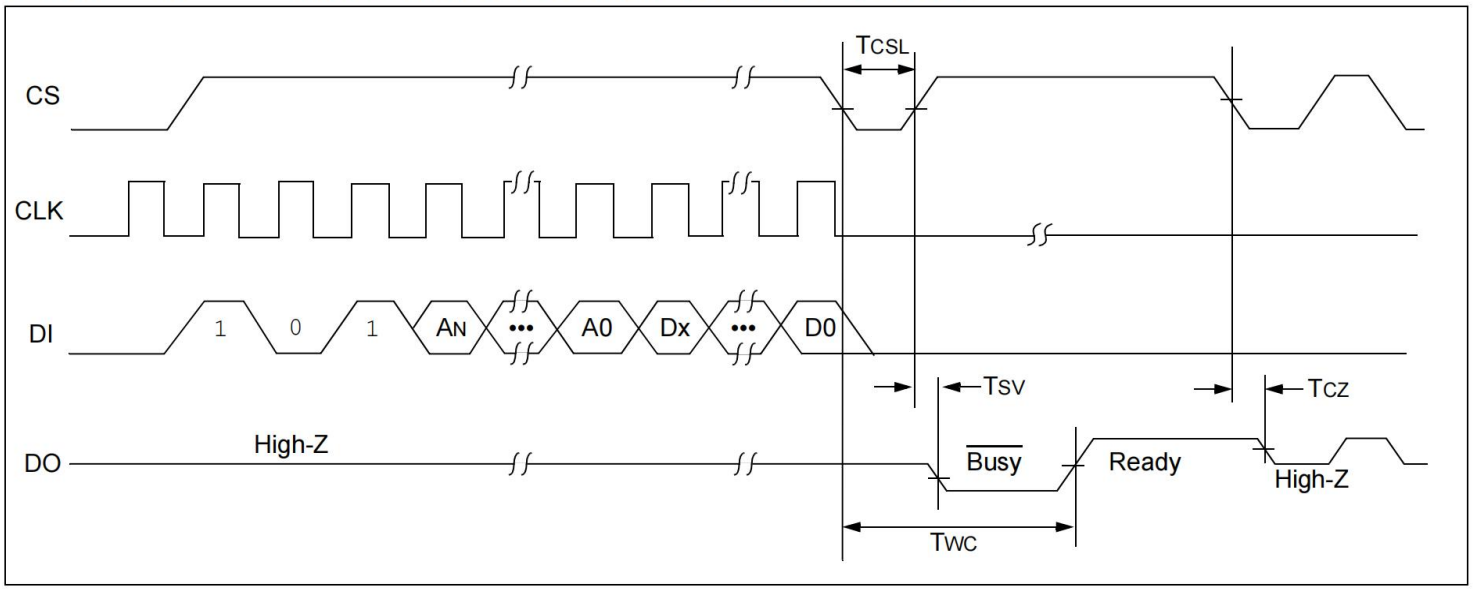
2.8 Write

The WRITE instruction is followed by 8 bits (if ORG is low or A-version devices) or 16 bits (if ORG pin is high or B-version devices) of data which are written into the specified address. For 93AA56A/B/C and 93LC56A/B/C devices, after the last data bit is clocked into DI, the falling edge of CS initiates the self-timed auto-erase and programming cycle. For 93C56A/B/C devices, the self-timed auto-erase and programming cycle is initiated by the rising edge of CLK on the last data bit.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device, if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical '0' indicates that programming is still in progress. DO at logical '1' indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

Note:	After the Write cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/$\overline{\text{Busy}}$ status from DO.

FIGURE 2-8: WRITE TIMING FOR 93AA AND 93LC DEVICES



2.9 Write All (WRAL)

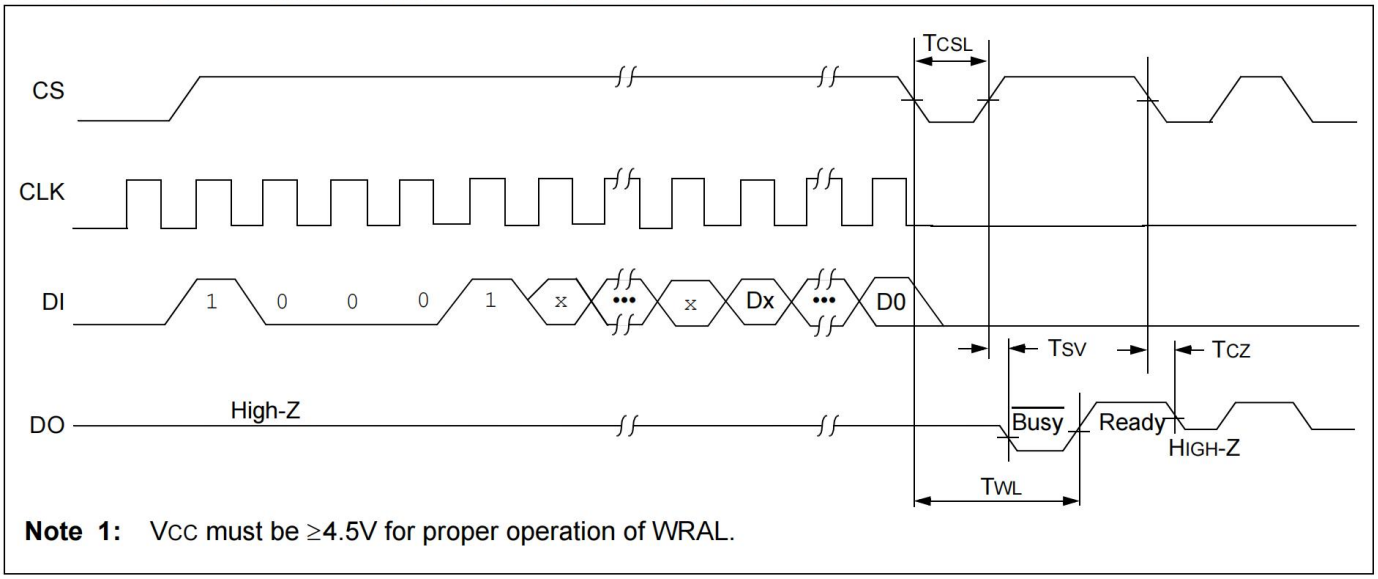
The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. For 93AA56A/B/C and 93LC56A/B/C devices, after the last data bit is clocked into DI, the falling edge of CS initiates the self-timed auto-erase and programming cycle. For 93C56A/B/C devices, the self-timed auto-erase and programming cycle is initiated by the rising edge of CLK on the last data bit. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction, but the chip must be in the EWEN status.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

Note:	After the Write All cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/$\overline{\text{Busy}}$ status from DO.

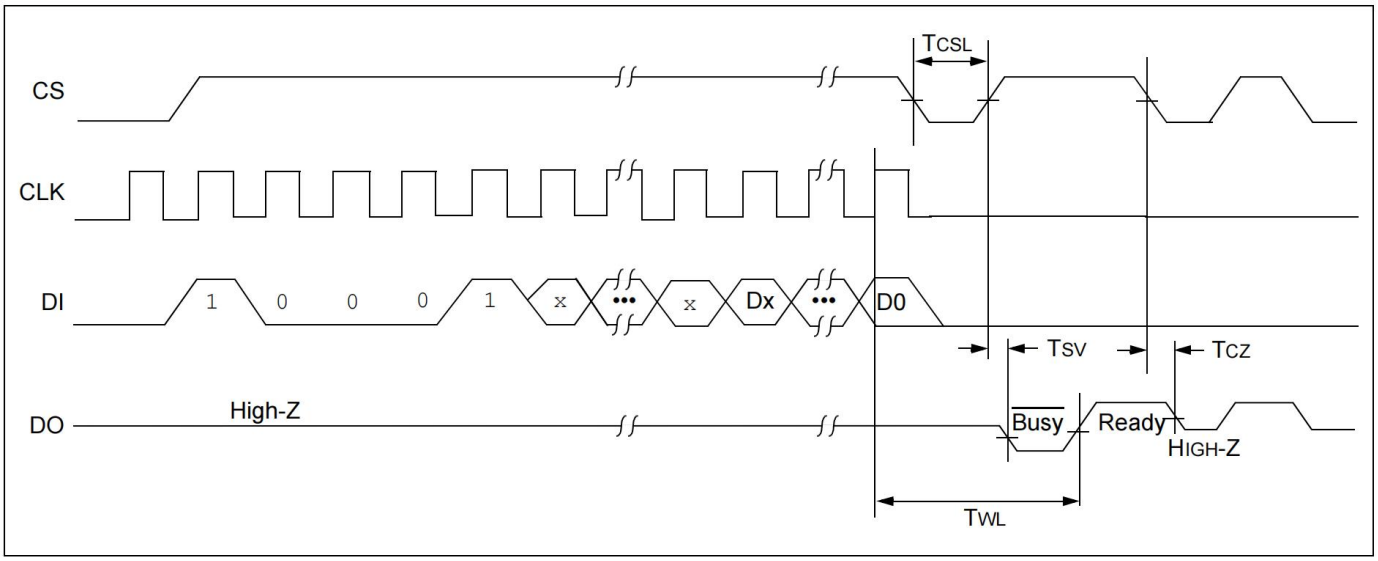
VCC must be ≥4.5V for proper operation of WRAL.

FIGURE 2-10: WRAL TIMING FOR 93AA AND 93LC DEVICES



Note 1: VCC must be ≥4.5V for proper operation of WRAL.

FIGURE 2-11: WRAL TIMING FOR 93C DEVICES



3.0 PIN DESCRIPTIONS

TABLE 3-1: PIN DESCRIPTIONS

Name	PDIP	SOIC	TSSOP	MSOP	DFN(1)	TDFN(1)	SOT-23	Rotated SOIC	Function
CS	1	1	1	1	1	1	5	3	Chip Select
CLK	2	2	2	2	2	2	4	4	Serial Clock
DI	3	3	3	3	3	3	3	5	Data In
DO	4	4	4	4	4	4	1	6	Data Out
VSS	5	5	5	5	5	5	2	7	Ground
ORG/NC	6	6	6	6	6	6	—	8	Organization/93XX56C No Internal Connection/93XX56A/B
NC	7	7	7	7	7	7	—	1	No Internal Connection
VCC	8	8	8	8	8	8	6	2	Power Supply

Note 1: The exposed pad on the DFN/TDFN packages may be connected to VSS or left floating.

3.1 Chip Select (CS)

A high level selects the device; a low level deselects the device and forces it into Standby mode. However, a programming cycle that is already in progress will be completed, regardless of the Chip Select (CS) input signal. If CS is brought low during a program cycle, the device will go into Standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (TCSL) between consecutive instructions. If CS is low, the internal control logic is held in a Reset status.

3.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a host device and the 93XX series device. Opcodes, address and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to Clock High Time (TCKH) and Clock Low Time (TCKL). This gives the controlling host freedom in preparing opcode, address and data.

CLK is a “don’t care” if CS is low (device deselected). If CS is high, but the Start condition has not been detected (DI = 0), any number of clock cycles can be received by the device without changing its status (i.e., waiting for a Start condition).

CLK cycles are not required during the self-timed write (i.e., auto erase/write) cycle.

After detection of a Start condition the specified number of clock cycles (respectively low-to-high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address and data bits before an instruction is executed. CLK and DI then become “don’t care” inputs waiting for a new Start condition to be detected.

3.3 Data In (DI)

Data In (DI) is used to clock in a Start bit, opcode, address and data synchronously with the CLK input.

3.4 Data Out (DO)

Data Out (DO) is used in the Read mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides Ready/$\overline{\text{Busy}}$ status information during erase and write cycles. Ready/$\overline{\text{Busy}}$ status information is available on the DO pin if CS is brought high after being low for minimum Chip Select low time (TCSL) and an erase or write operation has been initiated.

The Status signal is not available on DO if CS is held low during the entire erase or write cycle. In this case, DO is in the High-Z mode. If status is checked after the erase/write cycle, the data line will be high to indicate the device is ready.

Note:	After a programming cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/$\overline{\text{Busy}}$ status from DO.

3.5 Organization (ORG)

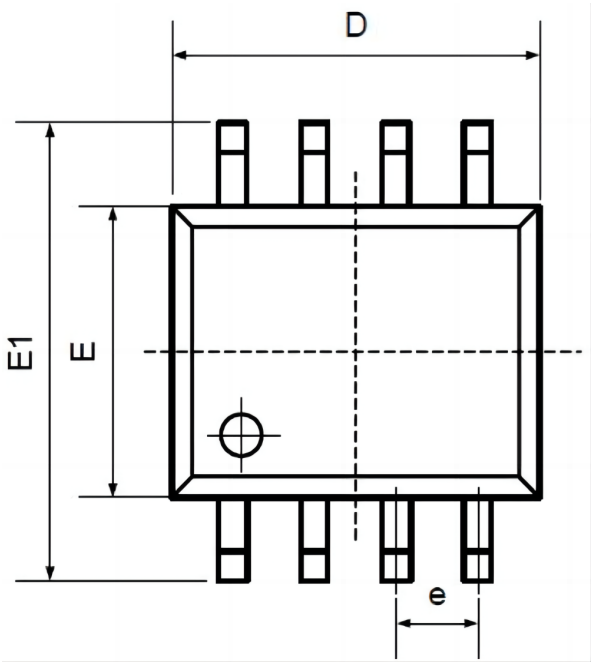
When the ORG pin is connected to VCC or Logic HI, the (x16) memory organization is selected. When the ORG pin is tied to VSS or Logic LO, the (x8) memory organization is selected. For proper operation, ORG must be tied to a valid logic level.

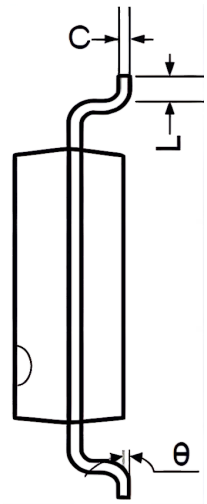
93XX56A devices are always (x8) organization and 93XX56B devices are always (x16) organization.

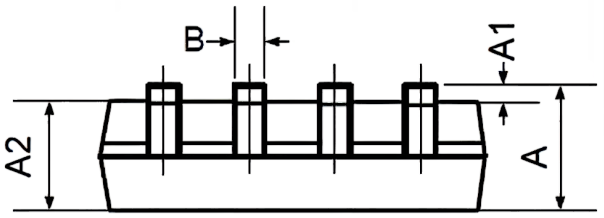
Order information

Order Number	Package	Package Quantity	Marking On The park
93AA56AT-I/SN-TUDI	SOP8	Tape,Reel,2500	93AA56AT-I/SN

Package SOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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