

H-Bridge DC Motor Driver

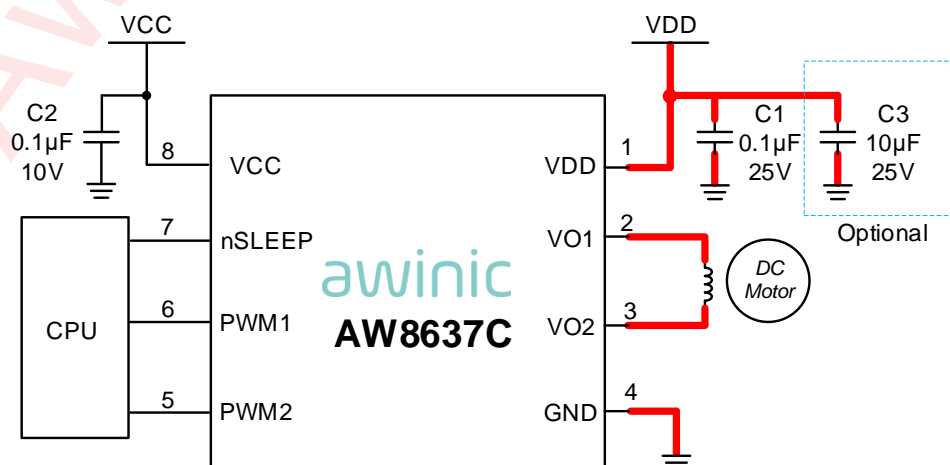
Features

- Drives a DC Motor or Other Loads
- $R_{\text{dson HS + LS}}$: 950m Ω
- 1.1-A Maximum Drive Current
- VDD: 0V to 12V Supply Voltage Range
- VCC: 1.8V to 5.5V Supply Voltage Range
- Low-Power Sleep Mode With 120-nA Maximum Sleep Current
- DFN 2mm X2mm X0.75mm-8L package
- Short-Circuit Protection
- Over-Temperature Protection
- Under-Voltage Protection

Applications

- Cameras
- DSLR Lenses
- Consumer Products
- Toys
- Robotics
- Medical Devices

Typical Application Circuit



General Description

The AW8637C provides an integrated motor driver solution for cameras, consumer products, toys, and other low-voltage or battery-powered motion control applications. The device can drive one dc motor or other devices like solenoids. The output driver block consists of N-channel power MOSFETs configured as an H-bridge to drive the motor winding. An internal charge pump generates needed gate drive voltages.

The AW8637C can supply up to 1.1A of output current. It operates on a motor power supply voltage from 0V to 12V, and a device power supply voltage of 1.8V to 5.5V.

The AW8637C has a PWM (PWM1-PWM2) input interface, which is compatible with industry standard devices.

Internal shutdown functions are provided for Over-current protection, Short-circuit protection, Under-voltage lockout, and Over-temperature protection.

Pin Configuration And Top Mark

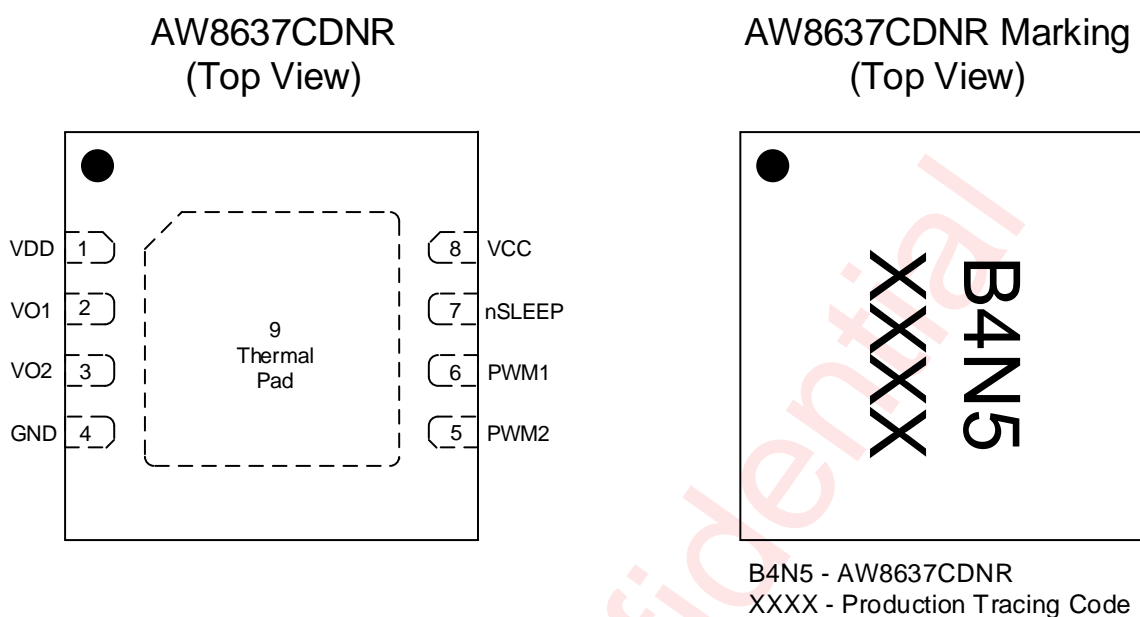


Figure 1 Pin Configuration And Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	VDD	Motor power supply. Bypass this pin to the GND pin with a 0.1- μ F ceramic capacitor rated for VDD.
2	VO1	Motor output. Connect these pins to the motor winding.
3	VO2	
4	GND	Device ground. This pin must be connected to ground.
5	PWM2	PWM2 input
6	PWM1	PWM1 input
7	nSLEEP	Sleep mode input. When this pin is in logic low, the device enters low-power sleep mode. The device operates normally when this pin is logic high. Internal pulldown
8	VCC	Logic power supply. Bypass this pin to the GND pin with a 0.1- μ F ceramic capacitor rated for VCC.
9	Thermal pad	Beneath the IC for heat dissipation. Always solder to the PCB ground for high-current power converter

Functional Block Diagram

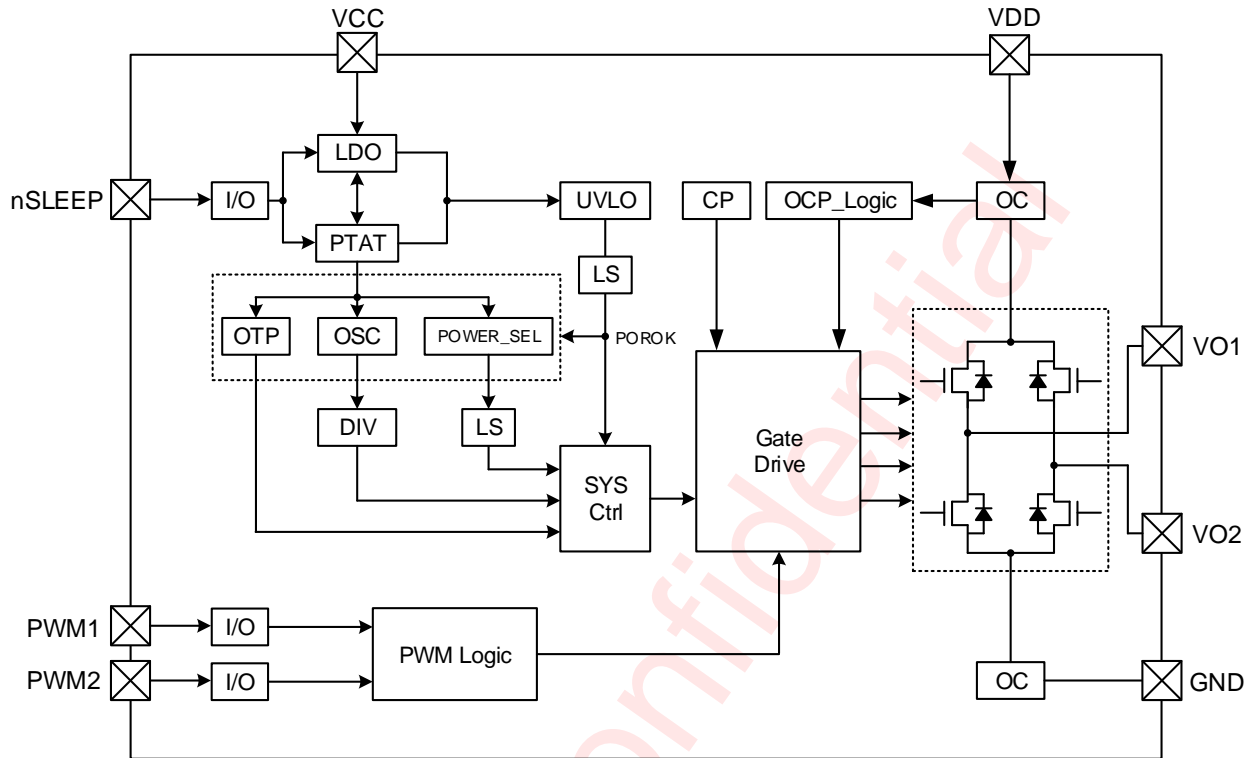


Figure 2 Functional Block Diagram

Typical Application Circuits

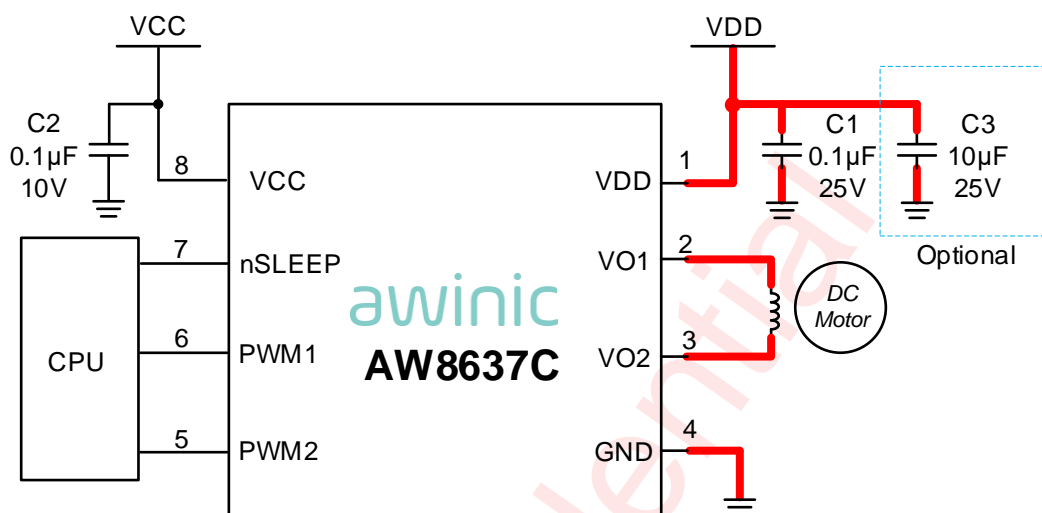


Figure 3 Typical Application Circuit of AW8637C

Notice for Typical Application Circuits:

- 1: Please place C1, C2 as close to the chip as possible. The capacitors should be placed in the same layer with the AW8637C chip.
- 2: For the sake of driving capability, the power lines and output lines should be short and wide as possible.
- 3: The power path marked in red as shown in the figures above, please traces according to 1.2A power line alignment rules.
- 4: **Table 1** lists the recommended external components for the device.

Table 1 External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C ₁	VDD	GND	25V, 0.1µF ceramic capacitor rated for VDD
C ₂	VCC	GND	10V, 0.1µF ceramic capacitor rated for VCC
C ₃	VDD	GND	25V, 10µF ceramic capacitor rated for VDD, optional according to the actual load

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW8637CDNR	-40°C~85°C	DFN 2mmX2mm-8L	B4N5	MSL1	ROHS+HF	3000 units/Tape and Reel

Absolute Maximum Ratings^(NOTE1)

PARAMETERS	RANGE
Motor power-supply voltage (VDD)	-0.3V to 13V
Logic power-supply voltage (VCC)	-0.3V to 5.5V
Control pin voltage (PWM1, PWM2, nSLEEP)	-0.5V to 5.5V
Peak drive current (VO1, VO2)	Internally limited
Junction-to-ambient thermal resistance θ_{JA}	97.7°C /W
Operating free-air temperature range	-40°C to 85°C
Maximum operating junction temperature T_{JMAX}	160°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD(Including CDM HBM) ^(NOTE 2)	
HBM(Human Body Model)	±3kV
CDM(Charge Device Model)	±1.5kV
Latch-Up	
Test Condition: JEDEC STANDARD NO.78E	+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. HBM method: ESDA/IEDEC JS-001-2017. CDM method: ESDA/JEDEC JS-002-2018. MM method: IESD22-A115C.

Electrical Characteristics

T_A=25°C for typical values (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
POWER SUPPLIES (VDD, VCC)						
VDD	VDD operating voltage	0		12	V	
I _{VDD}	VDD operating supply current	VDD=5V; VCC=3V; No PWM; No load		40	100	μA
		VDD=5V; VCC=3V; 50kHz PWM; No load		0.8	1.5	mA
I _{VDDQ}	VDD sleep mode supply current	VDD=5V; VCC=3V; nSLEEP=0		30	95	nA
VCC	VCC operating voltage	1.8		5.5	V	
I _{VCC}	VCC operating supply current	VDD=5V; VCC=3V; No PWM; No load		300	500	μA
		VDD=5V; VCC=3V; 50kHz PWM; No load		0.7	1.5	mA
I _{VCCQ}	VCC sleep mode supply current	VDD=5V; VCC=3V; nSLEEP=0		5	25	nA
CONTROL INPUTS (PWM1, PWM2, nSLEEP)						
V _{IL}	Input logic-low voltage	VCC=1.8V			0.35× VCC	V
		VCC=5V			0.19 × VCC	V
V _{IH}	Input logic-high voltage	VCC=1.8V	0.55 × VCC			V
		VCC=5V	0.48 × VCC			V
V _{HYS}	Input logic hysteresis	VCC=1.8V		0.09 × VCC		V
		VCC=5V		0.17 × VCC		V
I _{IL}	Input logic low current	V _{IN} =0V	-5		5	μA
I _{IH}	Input logic high current	V _{IN} =3.3V		33	50	μA
R _{PD}	Pulldown resistance			100		kΩ
MOTOR DRIVER OUTPUTS (VO1, VO2)						
r _{DS(on)}	HS + LS FET on-resistance	VDD=5V; VCC=3V; I _o = 800mA; T _J =25°C		950		mΩ
I _{OFF}	Off-state leakage current	V _{OUT} =0V	-200		200	nA
PROTECTION CIRCUITS						
V _{UVLO}	VCC undervoltage lockout	VCC falling			1.7	V
		VCC rising			1.8	V
I _{OC}	Overcurrent protection trip level			1.2		A
t _{DEG}	Overcurrent deglitch time			1		μs
t _{RETRY}	Overcurrent retry time			1		ms
T _{TSD}	Thermal shutdown temperature	Die temperature T _J	150	160	180	°C

Timing Requirements

$T_A=25^{\circ}\text{C}$, $V_{DD}=5\text{V}$, $V_{CC}=3\text{V}$

NO.		DESCRIPTION	TYP	UNIT
1	t_1	Output enable time	300	ns
2	t_2	Output disable time	350	ns
3	t_3	Delay time, PWMx high to VOx high	630	ns
4	t_4	Delay time, PWMx low to VOx low	200	ns
5	t_5	Output rise time	100	ns
6	t_6	Output fall time	50	ns
7	t_{wake}	Wake time, nSLEEP rising edge to part active	12	μs

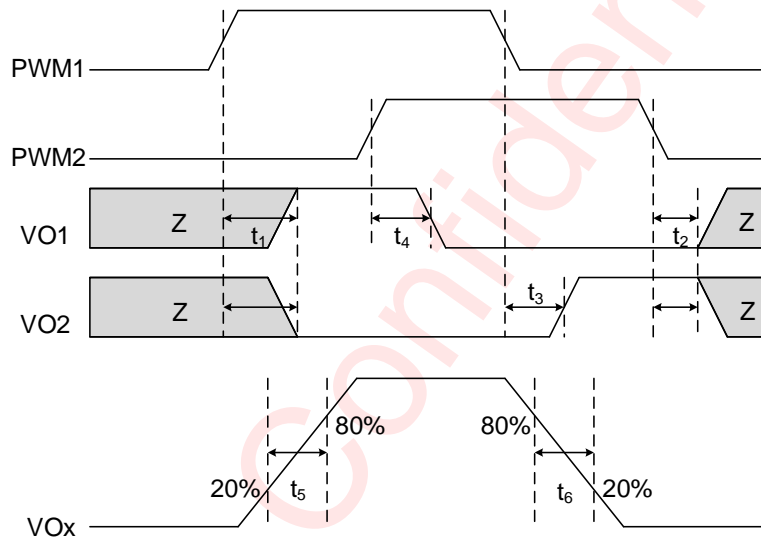


Figure 4 Input and Output Timing for AW8637C

Detailed Functional Description

OVERVIEW

The AW8637C is an H-bridge driver that can drive one dc motor or other devices like solenoids. The outputs are controlled using a PWM interface (PWM1 and PWM2) on the AW8637C device. A low-power sleep mode is included, which can be enabled using the nSLEEP pin.

The device greatly reduce the component count of motor driver systems by integrating the necessary driver FETs and FET control circuitry into a single device. In addition, the AW8637C adds protection features beyond traditional discrete implementations: under-voltage lockout, overcurrent protection, and thermal shutdown.

FEATURE DESCRIPTION

BRIDGE CONTROL

The AW8637C is controlled using a PWM input interface. Each output is controlled by a corresponding input pin. **Table 2** shows the logic for the AW8637C device.

Table 2 AW8637C Device Logic

nSLEEP	PWM1	PWM2	VO1	VO2	FUNCTION (DC MOTOR)
0	X	X	Z	Z	Coast
1	0	0	Z	Z	Coast
1	0	1	L	H	Reverse
1	1	0	H	L	Forward
1	1	1	L	L	Brake

SLEEP MODE

If the nSLEEP pin is brought to a logic-low state, the AW8637C enters a low-power sleep mode. In this state, all unnecessary internal circuitry is powered down.

POWER SUPPLIES AND INPUT PINS

The input pins can be driven within the recommended operating conditions with or without the VCC, VDD, or both power supplies present. No leakage current path will exist to the supply. Each input pin has a weak pulldown resistor (approximately 100 kΩ) to ground.

The VCC and VDD supplies can be applied and removed in any order. When the VCC supply is removed, the device enters a low-power state and draws very little current from the VDD supply. The VCC and VDD pins can be connected together if the supply voltage is between 1.8V and 5.5V.

The VDD voltage supply does not have any under-voltage lockout protection (UVLO) so as long as $VCC > 1.8V$; the internal device logic remains active, which means that the VDD pin voltage can drop to 0V. However, the load cannot be sufficiently driven at low VDD voltages.

VCC UNDERVOLTAGE LOCKOUT

If at any time the voltage on the VCC pin falls below the under-voltage lockout threshold voltage, all FETs in the H-bridge are disabled. Operation resumes when the VCC pin voltage rises above the UVLO threshold.

OVERCURRENT PROTECTION

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than t_{DEG} , all FETs in the H-bridge are disabled. Operation resumes automatically after t_{RETRY} has elapsed. Overcurrent conditions are detected on both the high-side and low side FETs. A short to the VDD pin, GND, or from the VO1 pin to the VO2 pin results in an overcurrent condition.

THERMAL SHUTDOWN

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature falls to a safe level, operation automatically resumes.

Table 3 Fault Behavior

FAULT	CONDITION	H-BRIDGE	RECOVERY
VCC under-voltage (UVLO)	$VCC < 1.7V$	Disabled	$VCC > 1.8V$
Overcurrent (OCP)	$I_{OUT} > 1.2A$ (TYPE)	Disabled	t_{RETRY} elapses
Thermal Shutdown (TSD)	$T_J > 160^{\circ}C$ (TYPE)	Disabled	$T_J < 130^{\circ}C$

DEVICE FUNCTIONAL MODES

The AW8637C is active unless the nSLEEP pin is brought logic low. In sleep mode, the H-bridge FETs are disabled Hi-Z. The AW8637C is brought out of sleep mode automatically if nSLEEP is brought logic high. The H-bridge outputs are disabled during under-voltage lockout, overcurrent, and over-temperature fault conditions.

Application Information

The AW8637C is used to drive one dc motor or other devices like solenoids. The following design procedure can be used to configure the AW8637C device.

DESIGN REQUIREMENTS

Table 4 lists the required parameters for a typical usage case.

Table 4 System Design Requirements

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	VDD	9V
Logic supply voltage	VCC	3.3V
Target rms current	I _{OUT}	0.8A
Externally applied PWM frequency	f _{PWM}	0 to 200kHz

MOTOR VOLTAGE

The appropriate motor voltage depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed dc motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

LOW-POWER OPERATION

When entering sleep mode, recommends setting all inputs as a logic low to minimize system power.

APPLICATION CURVES

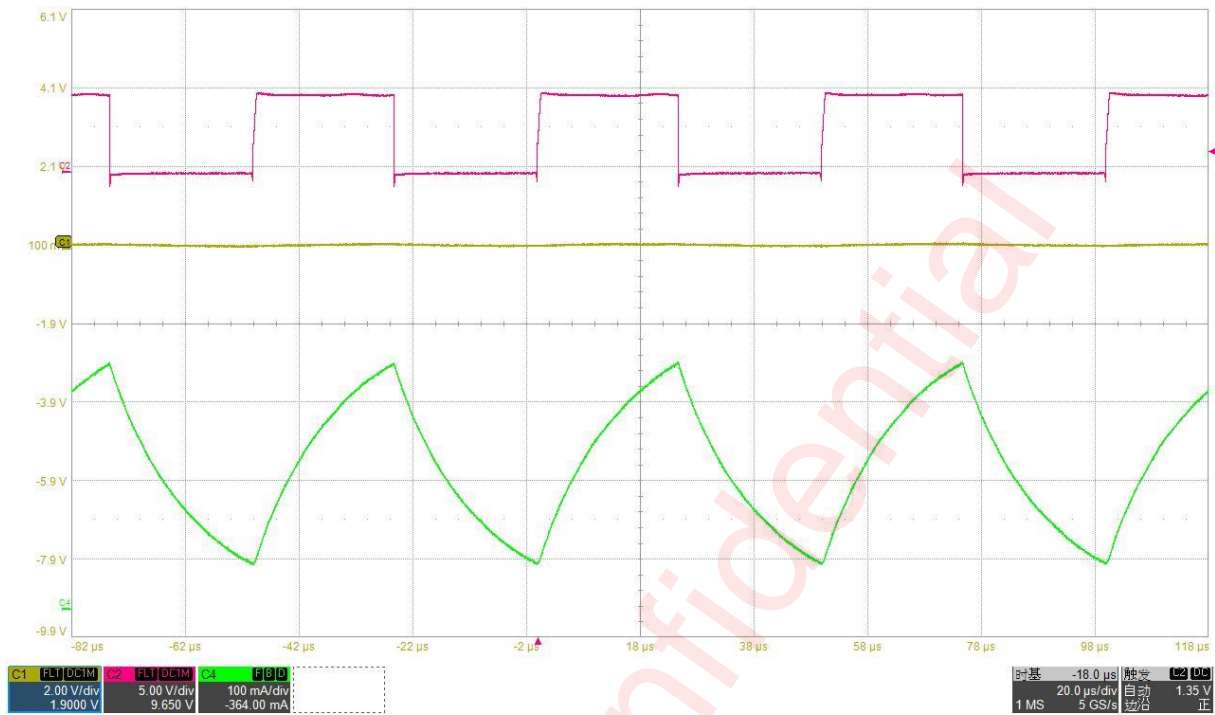


Figure 5 50% Duty Cycle Reverse Direction

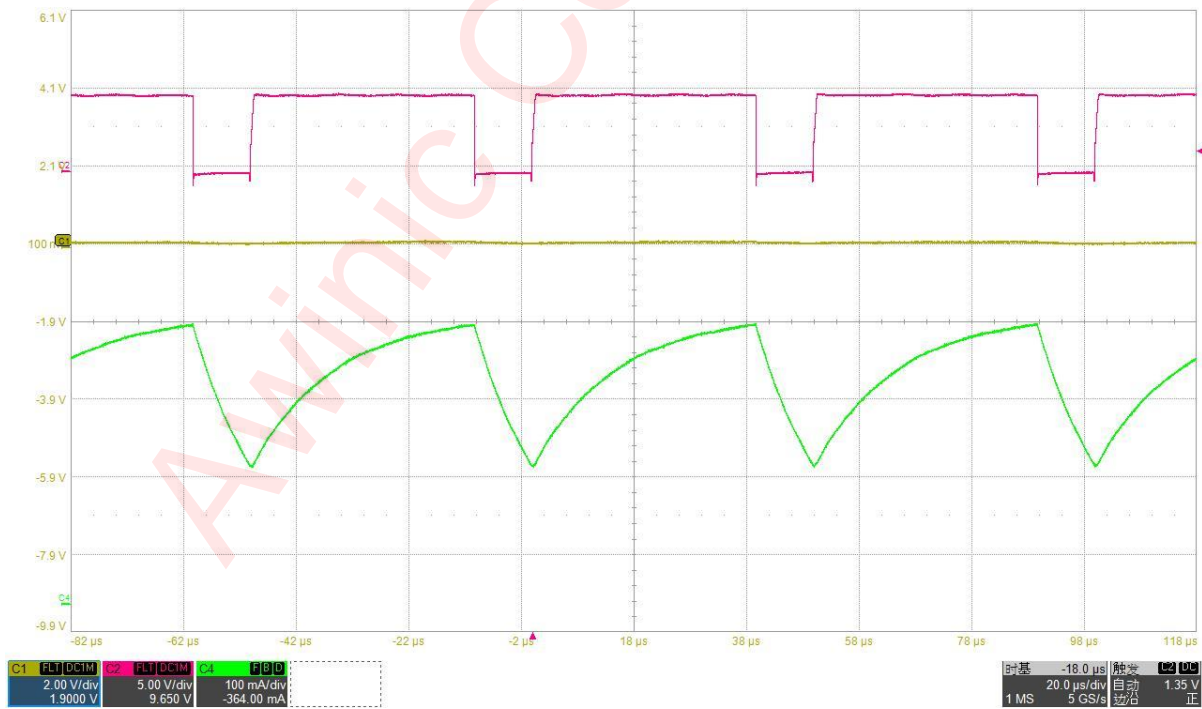


Figure 6 80% Duty Cycle Reverse Direction

POWER SUPPLY RECOMMENDATIONS

BULK CAPACITANCE

Having appropriate local bulk capacitance is an important factor in motor-drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power-supply capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless dc, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The datasheet generally provides a recommended value, but system-level testing is required to determine the appropriate size of bulk capacitor.

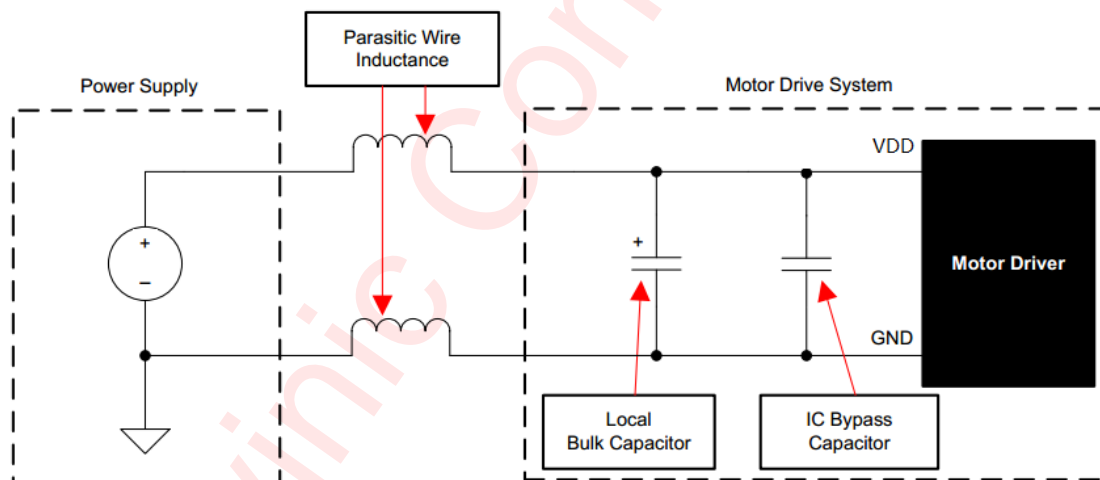


Figure 7 Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

PCB Layout Consideration

EXTERNAL COMPONENTS PLACEMENT

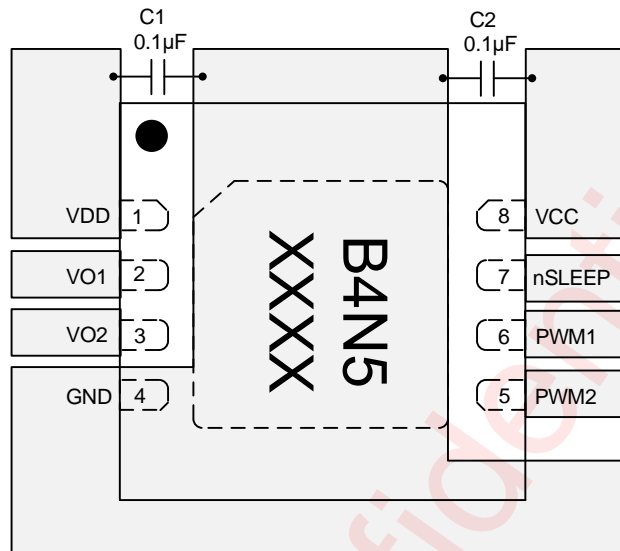


Figure 8 AW8637C External Components Placement

LAYOUT CONSIDERATIONS

This device is a high voltage driver chip. To obtain the optimal performance, PCB layout should be considered carefully. The suggested Layout is illustrated in the following diagram:

1. All of the external components close to IC in top layer PCB;
2. Create solid GND plane near and around the IC;
3. No via in traces from IC pin VDD/VCC through C1/C2 to IC pin GND, keep the trace as short as possible;
4. Try to provide a separate short and thick power line to the device, the copper width is recommended to be larger than 0.75mm. The decoupling capacitors should be placed as close as possible to boost power supply pin;
5. The output line from the device to load should be as short and thick as possible. The width is recommended to be larger than 0.5mm;

POWER DISSIPATION

Power dissipation in the AW8637C is dominated by the power dissipated in the output FET resistance, or $r_{DS(on)}$. Use Equation to estimate the average power dissipation when running a stepper motor.

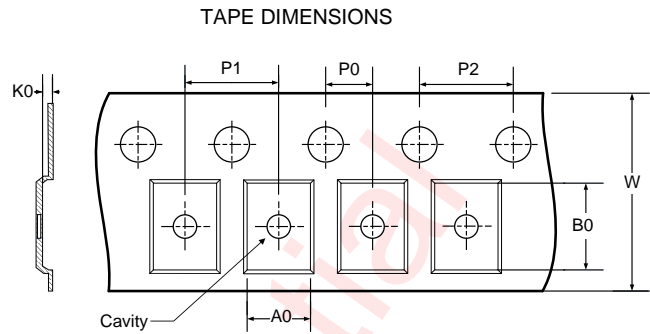
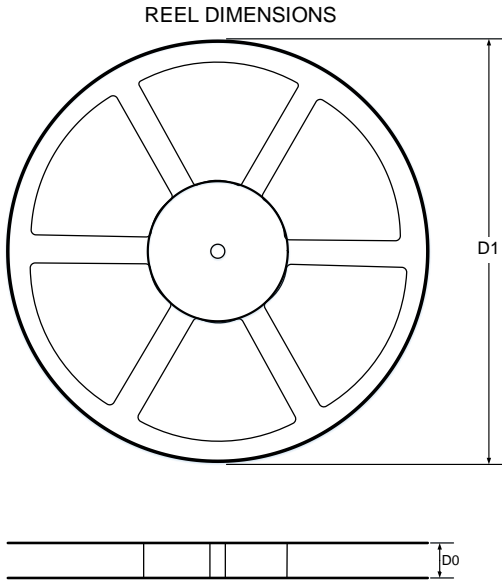
$$P_{TOT} = r_{DS(on)} \times (I_{OUT(rms)})^2$$

Where

- P_{TOT} is the total power dissipation
- $r_{DS(on)}$ is the resistance of the HS plus LS FETs
- $I_{OUT(rms)}$ is the rms or dc output current being supplied to the load

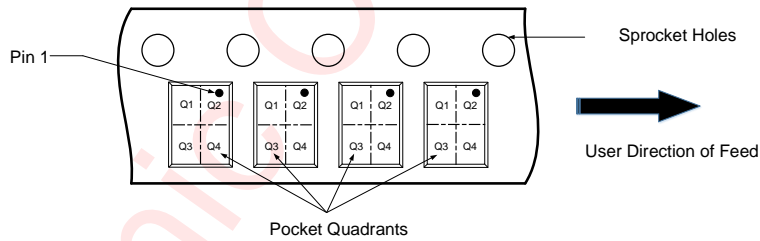
The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Tape And Reel Information



- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P0: Pitch between successive cavity centers and sprocket hole
- P1: Pitch between successive cavity centers
- P2: Pitch between sprocket hole
- D1: Reel Diameter
- D0: Reel Width

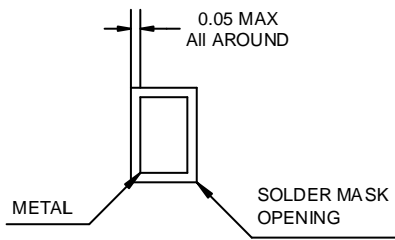
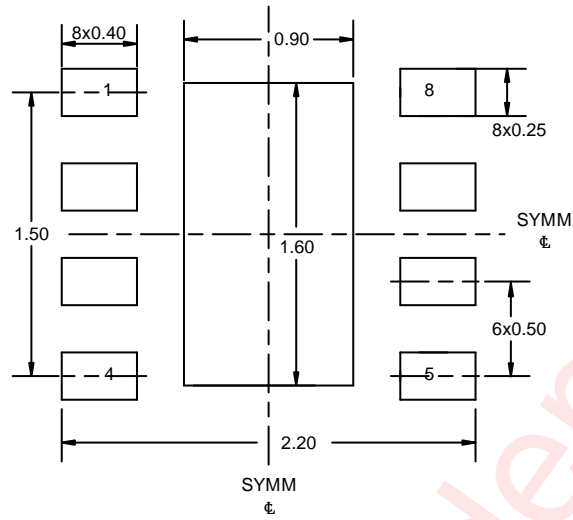
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



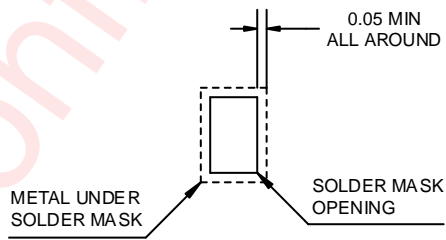
All Dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2.3	2.3	1.0	2.0	4.0	4.0	8.0	Q2

Land Pattern Data



NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	December 2019	Officially released
V1.1	December 2019	Change the R _{dson} to 950mΩ
V1.2	February 2021	Change the voltage range of VDD
V1.3	March 2022	Change the duty cycle of Figure 6
V1.4	August 2025	Change the IOCP to Type Value 1.2A Change ESD CDM to ±1kV Change Latch-Up to ±200mA Change VIL and VIH Value Change Timing Requirements Value

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