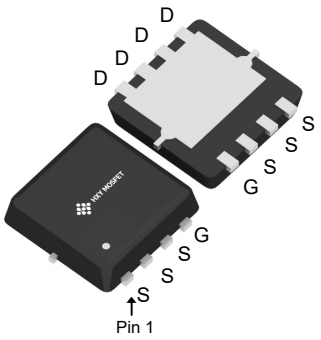
NTTFS5826NLTAG

N-Channel Enhancement Mode MOSFET

Description

The NTTFS5826NLTAG uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

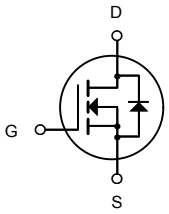


DFN3X3-8L

General Features

V_{DS} = 60V I_D = 15A

$R_{DS(ON)}$ < 40mΩ @ V_{GS}=10V



N-Channel MOSFET

Application

Battery protection

Load switch

Uninterruptible power supply

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
NTTFS5826NLTAG	DFN3X3-8L	HXY MOSFET	5000

Absolute Maximum Ratings (T_C=25°C unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_A=25°C	Continuous Drain Current, V_{GS} @ 10V[1]	15	A
I_D@T_A=70°C	Continuous Drain Current, V_{GS} @ 10V[1]	11	A
I_{DM}	Pulsed Drain Current[2]	46	A
EAS	Single Pulse Avalanche Energy[3]	25.5	mJ
I_{AS}	Avalanche Current	20	A
P_D@T_C=25°C	Total Power Dissipation[4]	34.7	W
T_{STG}	Storage Temperature Range	-55 to 175	°C
T_J	Operating Junction Temperature Range	-55 to 175	°C
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	62	°C/W

Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS} = 0V,	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	V_{DS}=0V, V_{GS} = ±20V	-	-	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.0	1.6	2.5	V
$R_{DS(on)}$	Static Drain-Source on-Resistance note3	V_{GS}=10V, I_D=5A	-	28	40	mΩ
		V_{GS}=4.5V, I_D=3A	-	36	50	
C_{iss}	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	-	1148	-	pF
C_{oss}	Output Capacitance		-	58.5	-	pF
C_{rss}	Reverse Transfer Capacitance		-	49.4	-	pF
Q_g	Total Gate Charge	V_{DS}=30V, I_D=2.5A, V_{GS}=10V	-	20.3	-	nC
Q_{gs}	Gate-Source Charge		-	3.7	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	5.3	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=30V, I_D=5A, R_G=1.8Ω, V_{GS}=10V	-	7.6	-	ns
t_r	Turn-on Rise Time		-	20	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	15	-	ns
t_f	Turn-off Fall Time		-	24	-	ns
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	5	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	15	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS}=0V, I_S=5A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	I_F=5A, dI/dt=100A/μs	-	29	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	43	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition : T_J=25°C,V_{DD}=30V,V_G=10V,L=0.5mH,Rg=25Ω,I_{AS}=8.7A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

Typical Characteristics

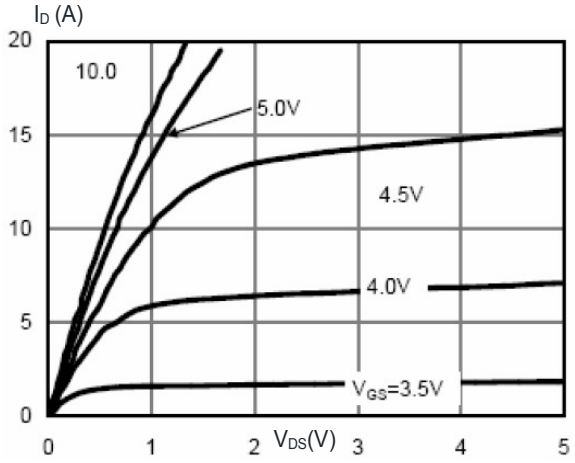


Figure1: Output Characteristics

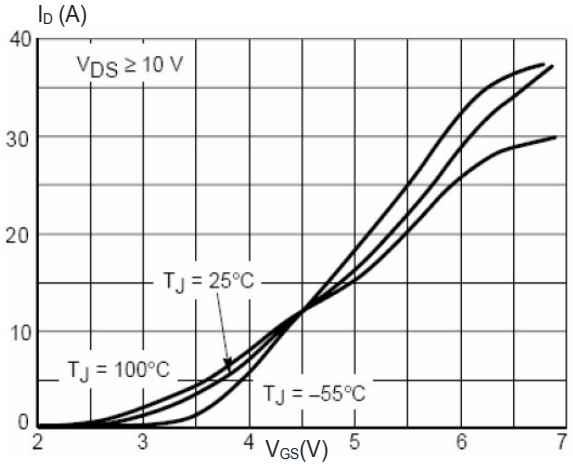


Figure 2: Typical Transfer Characteristics

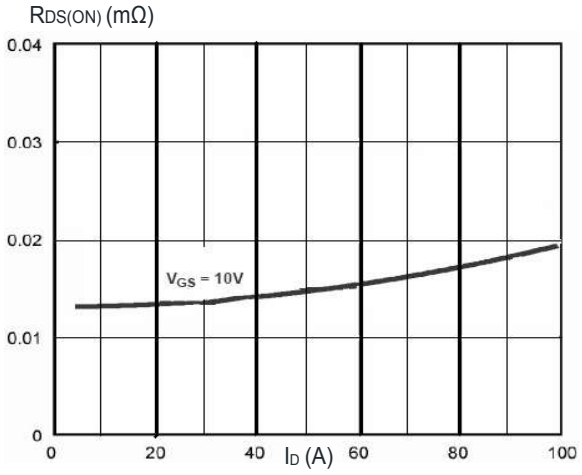


Figure 3: Rdson- Drain Current

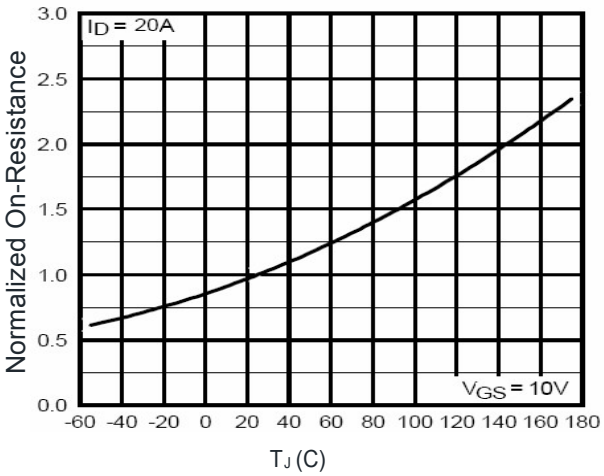


Figure 4: Rdson-Junction Temperature

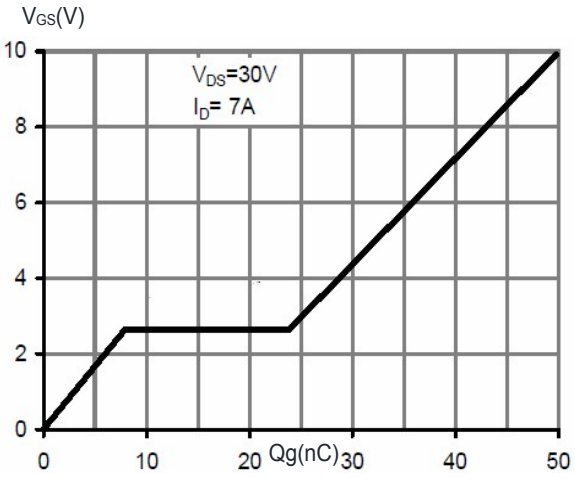


Figure 5: Gate Chare

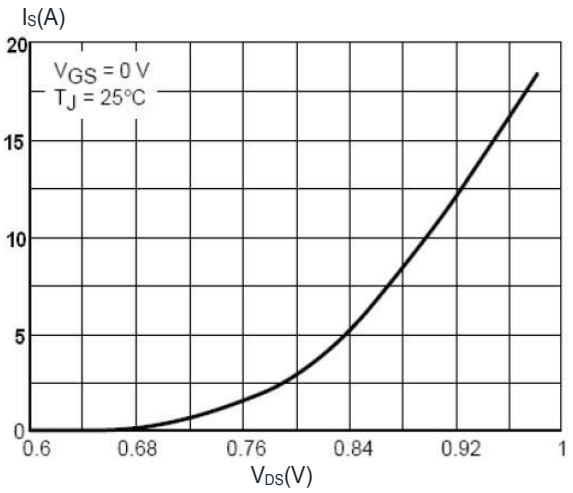


Figure 6: Source-Drain Diode Forward

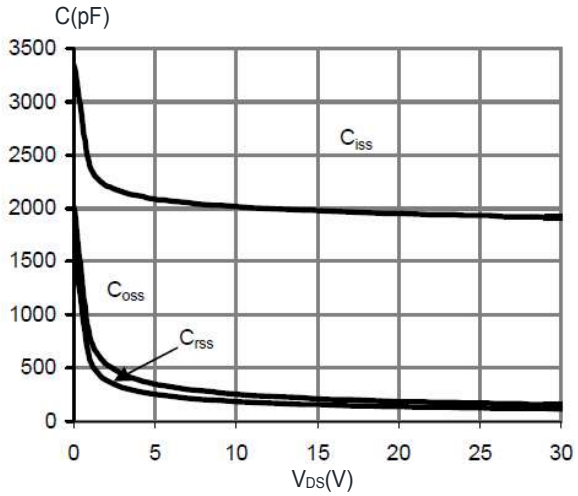


Figure 7: Capacitance vs Vds

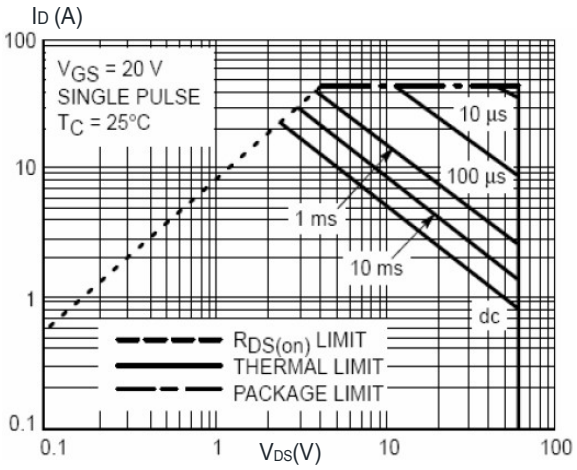


Figure 7: Safe Operation Area

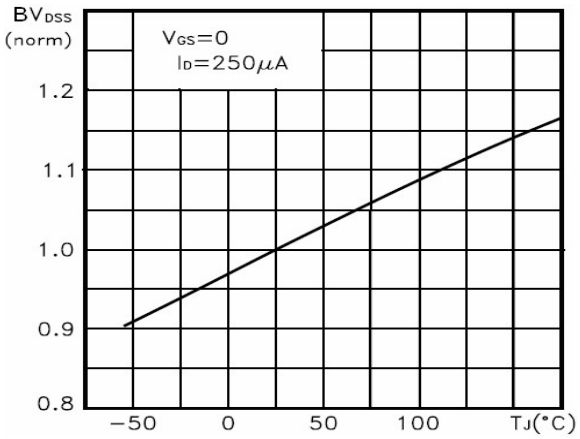


Figure 8: BVDSS vs Junction Temerature

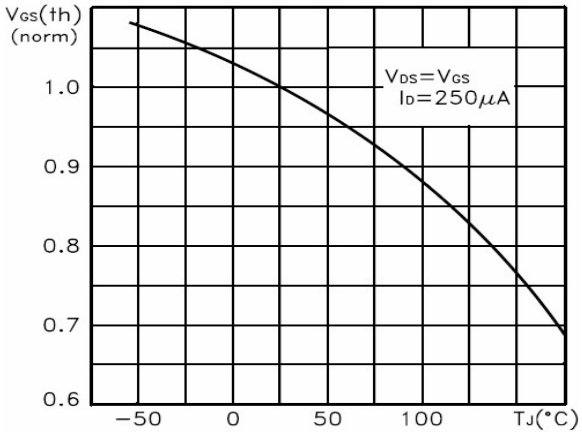


Figure 9: VGS(th) vs Junction Temperature

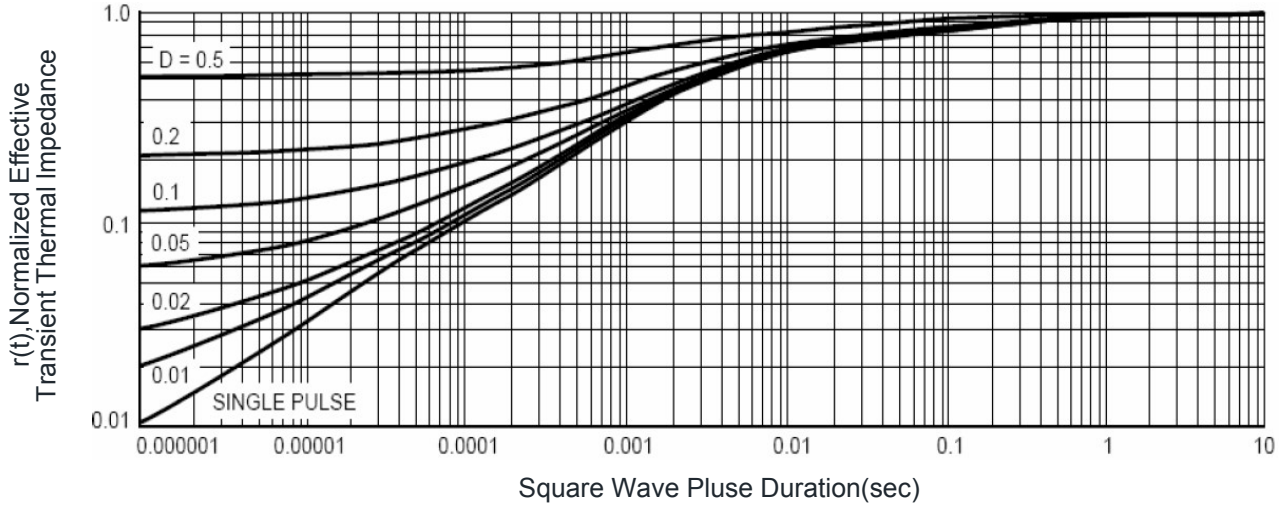


Figure 11: Normalized Maximum Transient Thermal Impedance

Test Circuit

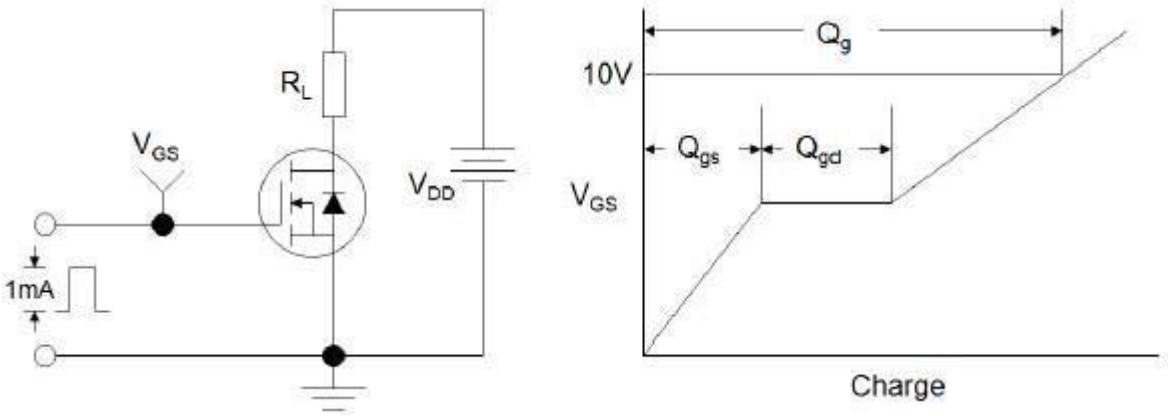


Figure1:Gate Charge Test Circuit & Waveform

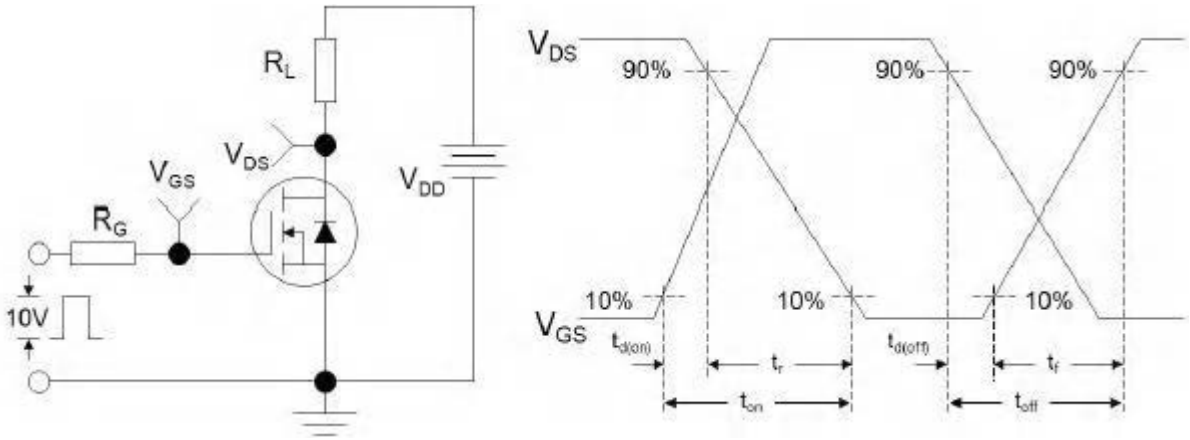


Figure 2: Resistive Switching Test Circuit & Waveforms

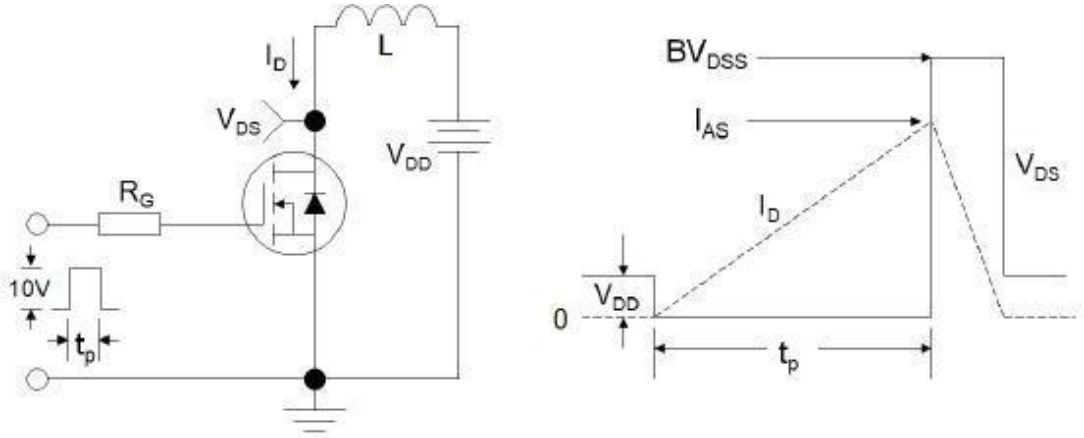
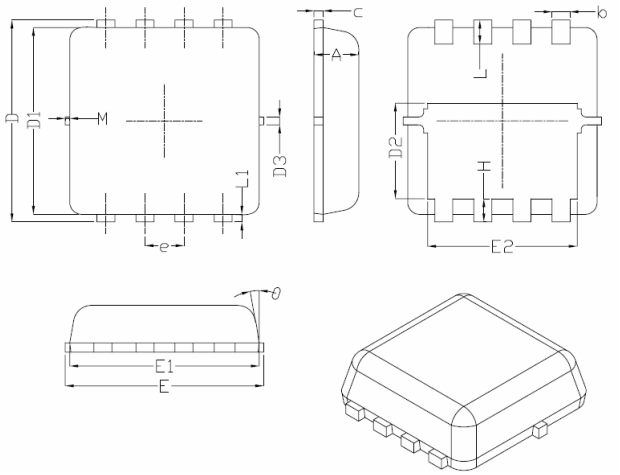


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

DFN3X3-8L Package Information



Symbol	Dimensions In Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.48	1.58	1.68
D3	-	0.13	-
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	-	0.13	-
M	*	*	0.15
θ		10°	12°

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