



钜地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65175/SN75175

四路差分线路接收器

网址 www.sztdbdt.com Q

用芯智造 · 卓越品质

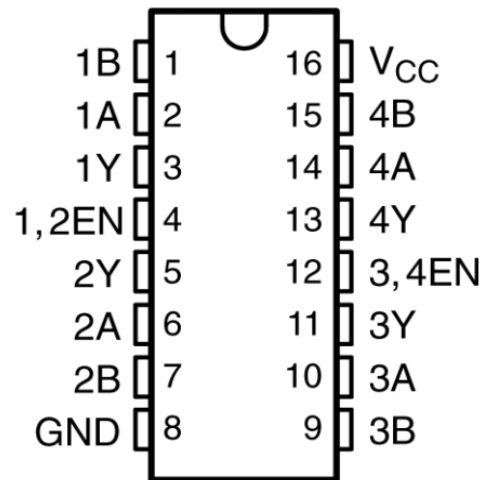
**semiconductor device
manufacturer**

- Design
- research and development
- production
- and sales



Features

- Complies with or exceeds the requirements of ANSI standards EIA/TIA-422-B, RS-423-B RS-485
- Complies with the requirements of ITU recommendations V.10, V.11, X.26 and X.27
- Suitable multi-point bus transmission on long buses in noisy environments
- Three-state output
- Common-mode input voltage range: $\pm 12V$ to $12V$
- sensitivity: $\pm 200mV$
- Input hysteresis: $50mV$ (typical)
- High input impedance: $12k\Omega$ (minimum)
- Powered by a $5V$ single supply
- Low power requirements
- Plug-in replacement for MC3486



D, N, or NS Package (Top View)

Applications

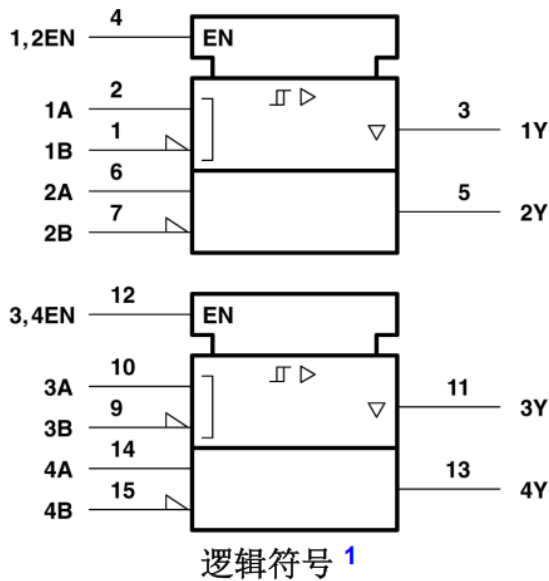
- Motor drivers
- Factory automation and

Description

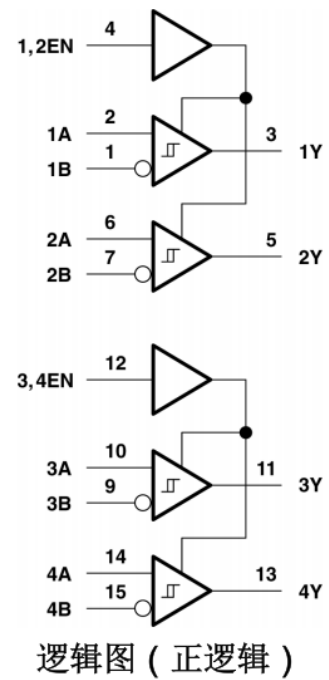
SN65175 and SN75175 are single-chip quad differential line receivers with three-state outputs. These devices with the requirements of ANSI standards EIA/TIA-422-B, RS-423-B, and RS-485, as well as several ITU. These standards are applicable to balanced multi-point bus transmissions with data rates up to 10 Mbps.

Each pair of receivers has a common active-high enable input. These receivers high input impedance, input hysteresis for improved noise immunity, and an input sensitivity of $\pm 200mV$ over a $\pm 12V$ common-mode input voltage range.

SN6175 and SN75175 achieve excellent performance when used with SN75172 or SN75174 quad differential line drivers. The rated temperature range of SN65175 is $-40^{\circ}C$ to $85^{\circ}C$. The rated operating temperature range of SN75175 is $0^{\circ}C$ to $70^{\circ}C$.



逻辑符号 1



逻辑图 (正逻辑)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 Differential Receiver Inverting Input
1A	2	I	Channel 1 Differential Receiver Non-Inverting Input
1Y	3	O	Channel 1 Single Ended Output
1,2EN	4	I	Active High Enable for Channels 1 and 2
2Y	5	O	Channel 2 Single Ended Output
2A	6	I	Channel 2 Differential Receiver Non-Inverting Input
2B	7	I	Channel 2 Differential Receiver Inverting Input
GND	8	GND	Device GND
3B	9	I	Channel 3 Differential Receiver Inverting Input
3A	10	I	Channel 3 Differential Receiver Non-Inverting Input
3Y	11	O	Channel 3 Single Ended Output
3,4EN	12	I	Active High Enable for Channels 3 and 4
4Y	13	O	Channel 4 Single Ended Output
4A	14	I	Channel 4 Differential Receiver Non-Inverting Input
4B	15	I	Channel 4 Differential Receiver Inverting Input
V _{CC}	16	PWR	Device V _{CC} (4.75 V to 5.25 V)

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIX	MAX	UNIT
V_{CC} ⁽²⁾	Supply voltage			7	V
V_I	Input voltage (A or B inputs)			± 25	V
V_{ID} ⁽³⁾	Differential input voltage			± 25	V
$V_{I(EN)}$	Enable input voltage			7	V
I_{OL}	Low-level output current			50	mA
	Continuous total dissipation	See <i>Dissipation Rating</i> table			
T_A	Operating free-air temperature range:	SN65175	-40	85	°C
		SN75175	0	70	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C
T_{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential input voltage, are with respect to network ground terminal.

(3) Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

5.2 Dissipation Rating

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}				± 12	V
Differential input voltage, V_{ID}				± 12	V
High-level enable-input voltage, V_{IH}		2			V
Low-level enable-input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}				-400	μA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A	SN65175	-40		85	°C
	SN75175	0		70	



5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		D (SOIC)	N (PDIP)	NS (SOP)	UNIT
		16-PINS			
R _{θJA}	Junction-to-ambient thermal resistance	84.6	60.6	88.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	43.5	48.1	46.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	43.2	40.6	50.7	°C/W
ψ _{JT}	Junction-to-top characterization parameter	10.4	27.5	13.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	42.8	40.3	50.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.5 Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	V _O = 2.7 V,	I _O = - 0.4 mA				0.2	V
V _{IT-}	Negative-going input threshold voltage	V _O = 0.5 V,	I _O = 16 mA				- 0.2 ⁽²⁾	V
V _{hys}	Hysteresis voltage (V _{IT+} - V _{IT-})	See 图 5-1				50		mV
V _{IK}	Enable-input clamp voltage	I _I = - 18 mA					-1.5	V
V _{OH}	High-level output voltage	V _{ID} = 200 mV,	I _{OH} = - 400 μA,	See 图 6-1		2.7		V
V _{OL}	Low-level output voltage	V _{ID} = - 200 mV,	See 图 6-1	I _{OL} = 8 mA			0.45	V
				I _{OL} = 16 mA			0.5	
I _{OZ}	High-impedance-state output current	V _O = 0.4 V to 2.4 V					±20	μA
I _I	Line input current	Other input at 0 V,	See ⁽⁴⁾	V _I = 12 V			1	mA
				V _I = - 7 V			-0.8	
I _{IH}	High-level enable-input current	V _{IH} = 2.7 V					20	μA
I _{IL}	Low-level enable-input current	V _{IL} = 0.4 V					-100	μA
r _i	Input resistance					12		k Ω
I _{OS}	Short-circuit output current ⁽³⁾					-15	-85	mA
I _{CC}	Supply current	Outputs disabled					70	mA

- (1) All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.
(2) The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.
(3) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
(4) Refer to ANSI Standards EIA/TIA-422-B, RS-423-B, and RS-485 for exact conditions.



5.6 Switching Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See 图 6-2		22	35	ns
t_{PHL}	Propagation delay time, high- to low-level output			25	35	ns
t_{PZH}	Output enable time to high level	See 图 6-3		13	30	ns
t_{PZL}	Output enable time to low level			19	30	ns
t_{PHZ}	Output disable time from high level	See 图 6-3		26	35	ns
t_{PLZ}	Output disable time from low level			25	35	ns

6 Parameter Measurement Information

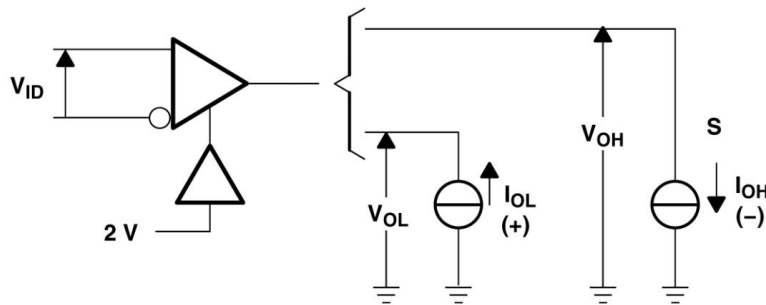
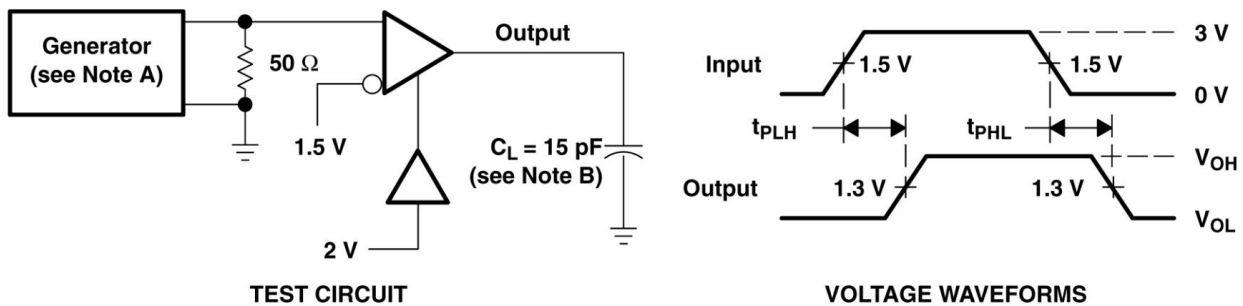
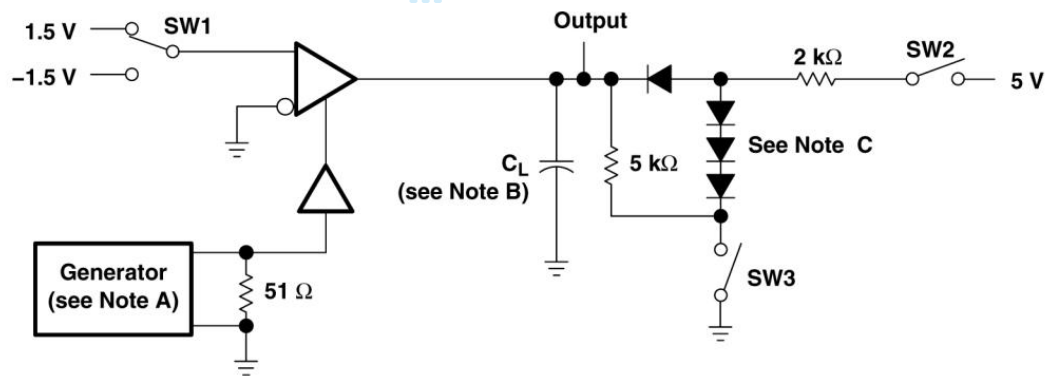


图 6-1. V_{OH} , V_{OL}

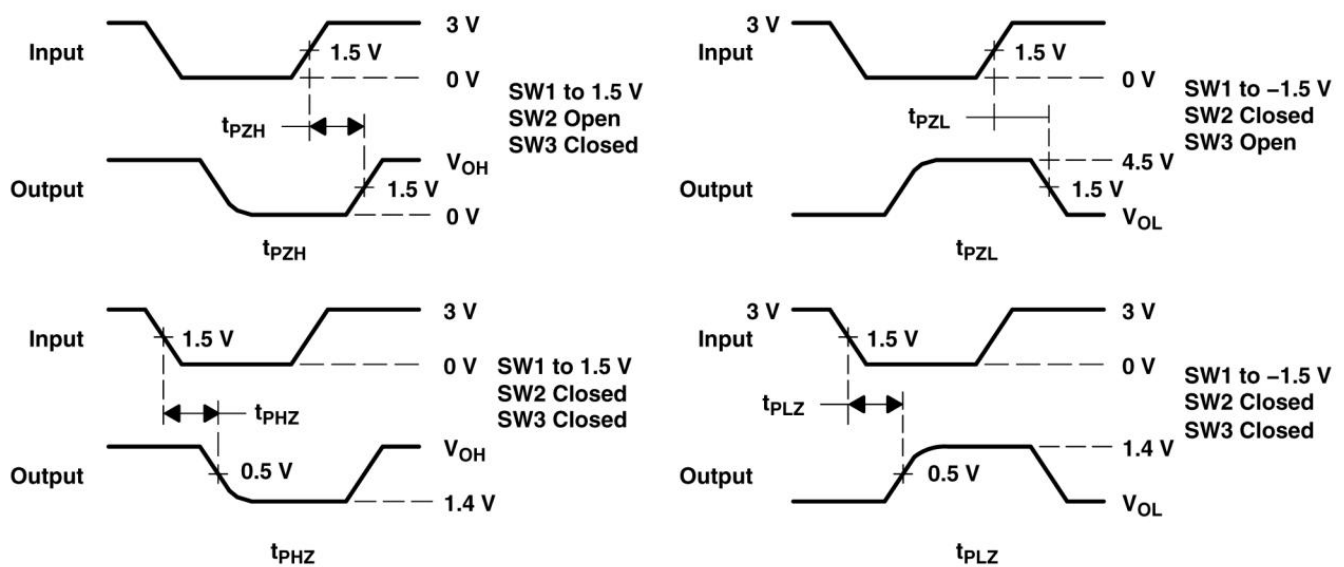


- A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1\text{ MHz}$, duty cycle = 50%, $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$, $Z_O = 50\ \Omega$.
- B. C_L includes probe and stray capacitance.

图 6-2. Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

- A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, duty cycle = 50%, $t_f \leq 6 \text{ ns}$, $t_r \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.
- B. C_L includes probe and stray capacitance.
- C. All diodes are 1N916 or equivalent.

图 6-3. Test Circuit and Voltage Waveforms



7 Detailed Description

7.1 Device Functional Modes

表 7-1. Function Table (Each Receiver)

DIFFERENTIAL A – B ⁽¹⁾	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2 \text{ V}$	H	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$	H	?
$V_{ID} \leq -0.2 \text{ V}$	H	L
X	L	Z
Open circuit	H	?

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

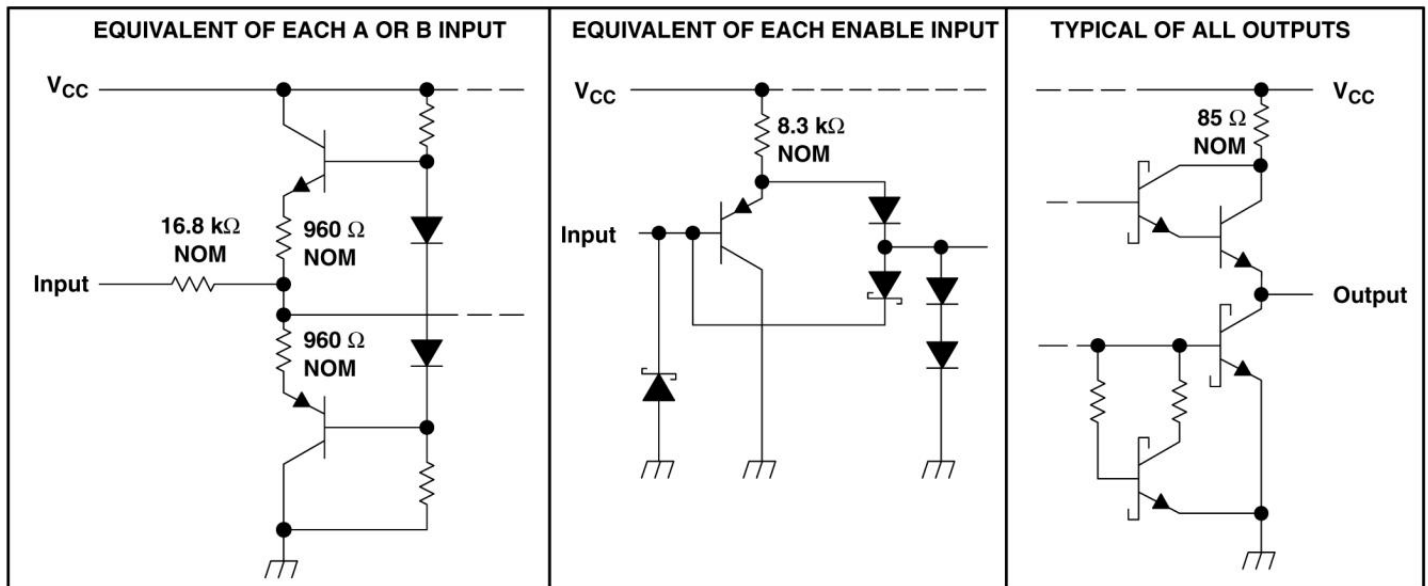
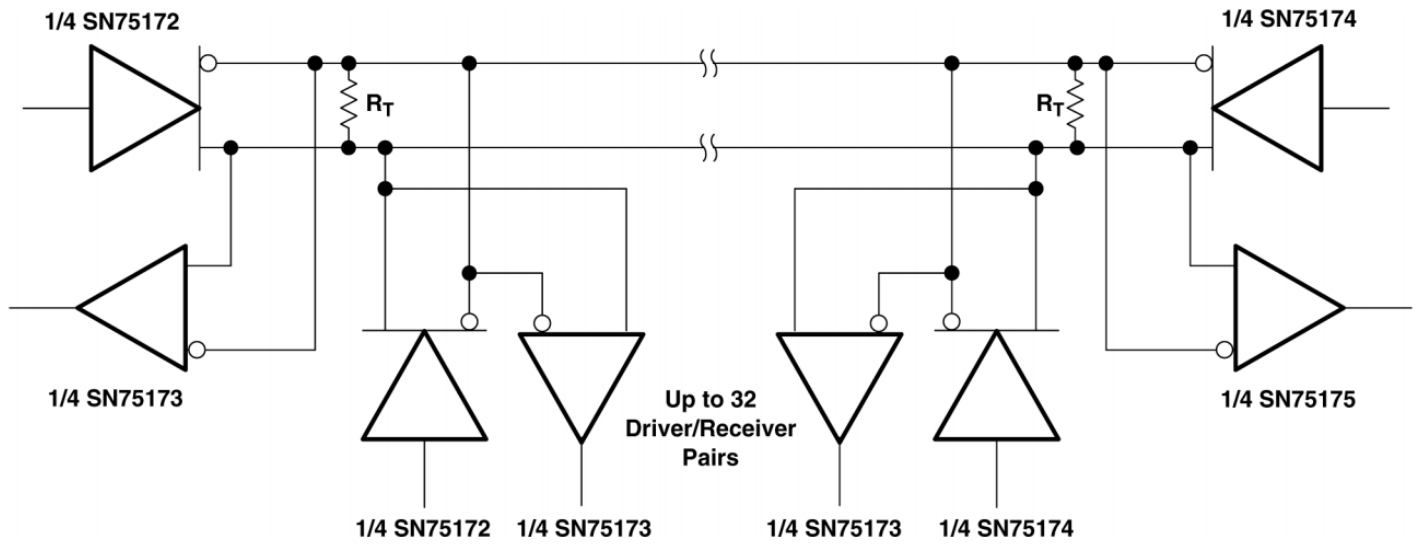


图 7-1. Schematics of Inputs and Outputs



8.1 Application Information



- A. The line should be terminated at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

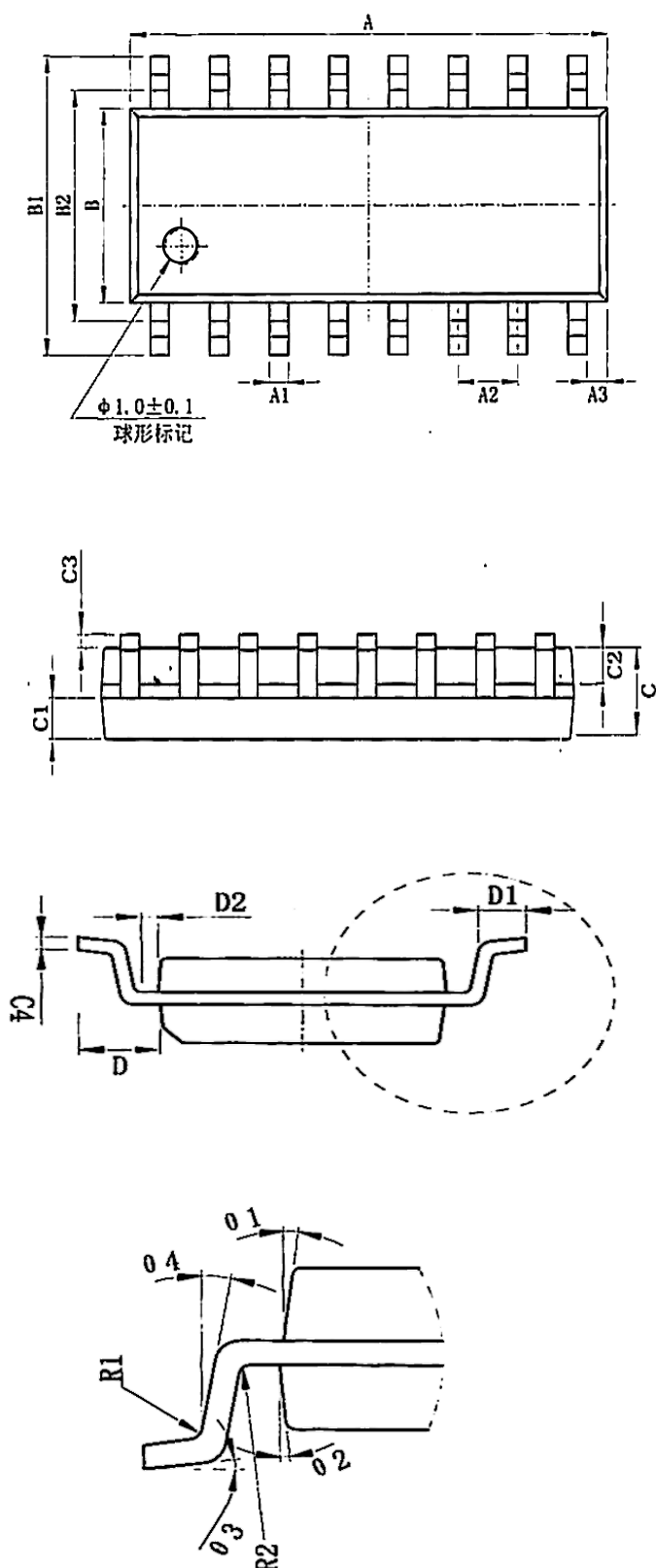
图 8-1. Typical Application Circuit



Order information

Order Number	Package	Package Quantity	Marking On The park
SN65175DR-TUDI	SOP16	Tape,Reel,2500	SN65175DR
SN65175N-TUDI	DIP16	Tube,25,A box of 1000	SN65175N
SN75175DR-TUDI	SOP16	Tape,Reel,2500	SN75175DR
SN75175N-TUDI	DIP16	Tube,25,A box of 1000	SN75175N

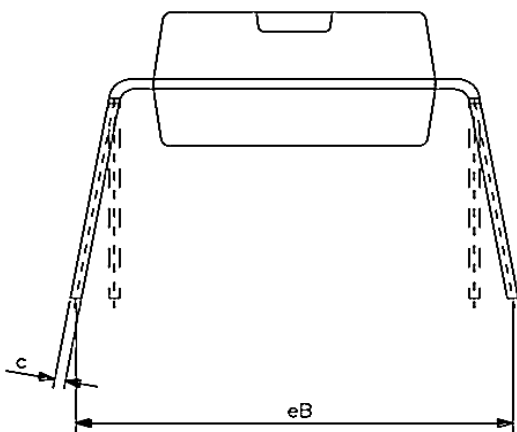
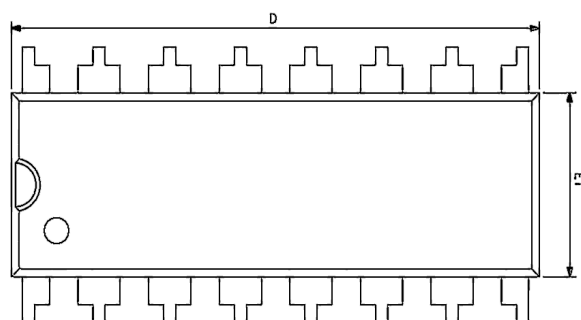
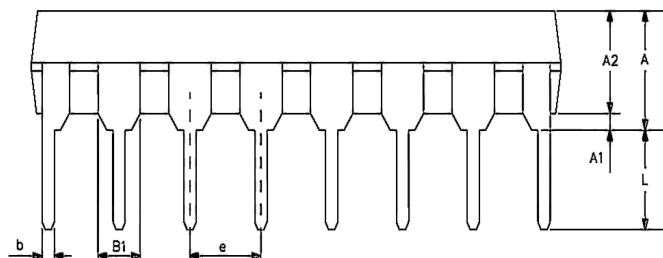
Package SOP16



SIZE SYMBOL	MIN./mm	MAX./mm
A	9.80	10.00
A1	0.356	0.456
A2	1.27TYP	
A3	0.302TYP	
B	3.85	3.95
B1	5.84	6.24
B2	5.00 TYP	
C	1.40	1.60
C1	0.61	0.71
C2	0.54	0.64
C3	0.05	0.25
C4	0.203	0.233
D	1.05 TYP	
D1	0.40	0.70
D2	0.15	0.25
R1	0.20TYP	
R2	0.20TYP	
01	8°~12°TYP4	
02	8°~12°TYP4	
03	0°~8°	
04	4°~12°	



Package DIP16



SIZE SYMBOL	MIN./mm	MAX./mm
A2	3.20	3.60
A1	0.51	—
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
C	0.20	0.36
eB	7.62	9.30
R	0.20TYP	
R1	0.30TYP	
θ	0°	8°
$\theta 1$	45°TYP	
02	12°TYP	
03	0°	8°
04	0°	10°



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