Upgraded 2W Class-K Audio Amplifier with RF-TDD Suppression and NCN

Features

- Built-In RNS Function，Excellent TDD Suppression
- NCN Function Protects the Speaker
- EEE Function , Greatly reduces EMI over the full bandwidth
- 2.0W into 8Ω at 4.2V(1% THD+N)
- 4 Selectable Gain,12dB,16dB,24dB,27.5dB
- 4 Mode selected by one-wire pulse
- Excellent Pop-Click Suppression
- Short-Circuit and Thermal Protection
- QFN 3mm x 3mm x 0.75mm - 20L Package

Applications

- Cellular Phones
- Portable Audio Devices
- Mini Speakers

General Description

AW8733B is a powerful Class-K audio amplifier that features RNS (RF-TDD Noise Suppression), NCN (Non-Crack-Noise) and EEE (Enhanced Emission Elimination).

AW8733B is a Class-K audio amplifier upgraded from AW8733A, noise, power, efficiency and other indicators have been improved.

AW8733B features the RNS function which greatly reduces RF-TDD Noise.

AW8733B features a built-in charge pump converter generates a 6.5V supply voltage. This provides a louder audio output than a stand-alone amplifier directly connected to the battery.

AW8733B features 2W output power (1% THD+N) into 8Ω load at 4.2V battery voltage.

AW8733B features the NCN function, which adjusts the system gain automatically while detecting the “Crack” distortion of output signal, protects the speaker from damage at high power levels and brings the most comfortable listening experience to the customers.

AW8733B is available in a QFN 3mm x 3mm x 0.75mm -20L Package. It is specified over the extended -40℃ to +85℃ temperature range.

Typical Application Circuit

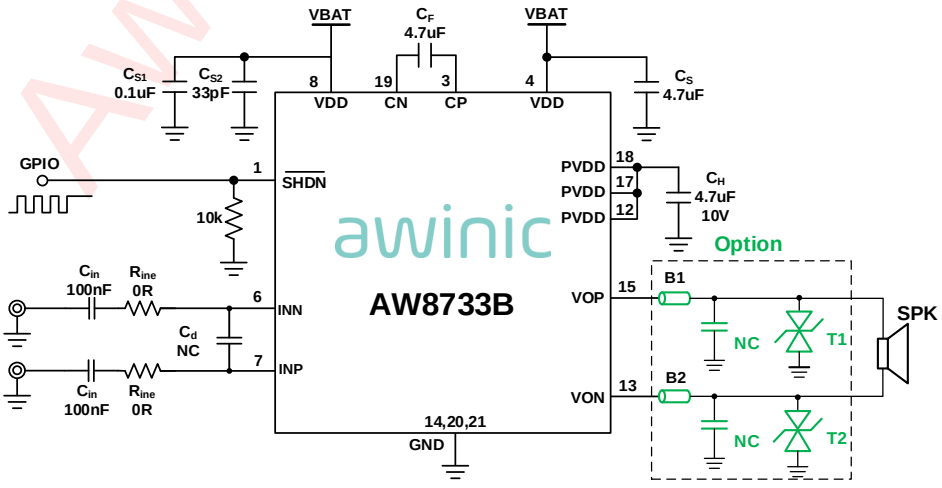
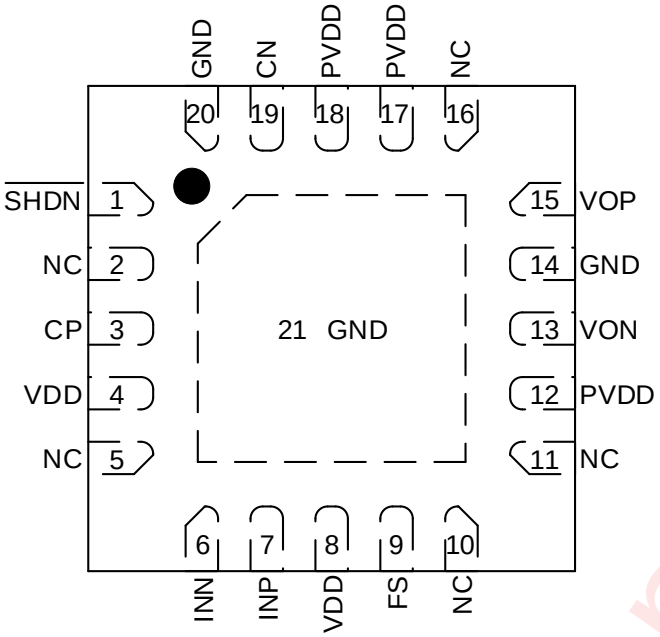


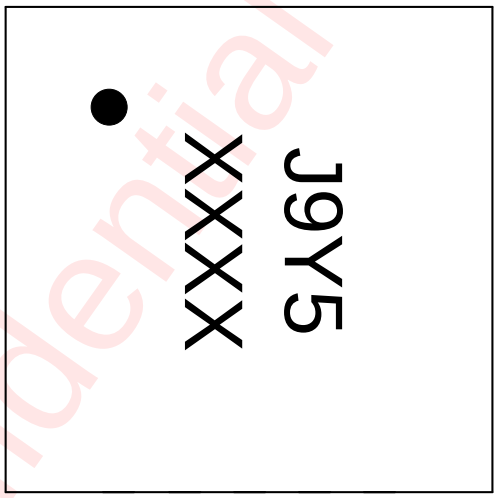
Figure 1 AW8733B Typical Application Diagram

Pin Configuration And Top Mark

AW8733BTQR
(Top view)



AW8733BTQR Marking
(Top view)



J9Y5 - AW8733BTQR
XXXX - Production Tracing Code

Figure 2 AW8733B Pin configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	$\overline{\text{SHDN}}$	Shutdown and one-wire control pin
3	CP	Positive Terminal of Flying capacitor
4,8	VDD	Supply Voltage.
6	INN	Negative Amplifier Input
7	INP	Positive Amplifier Input
9	FS	Test pin. Connect a 100k resistor to ground or No Connect
12,17,18	PVDD	Charge-Pump Output.
13	VON	Negative Amplifier output
14,20	GND	Ground
15	VOP	Positive Amplifier Output
19	CN	Negative Terminal of Flying capacitor.
21	GND	Exposed Pad. Connect to GND.
2,5,10,11,16	NC	No Connect

Functional Block Diagram

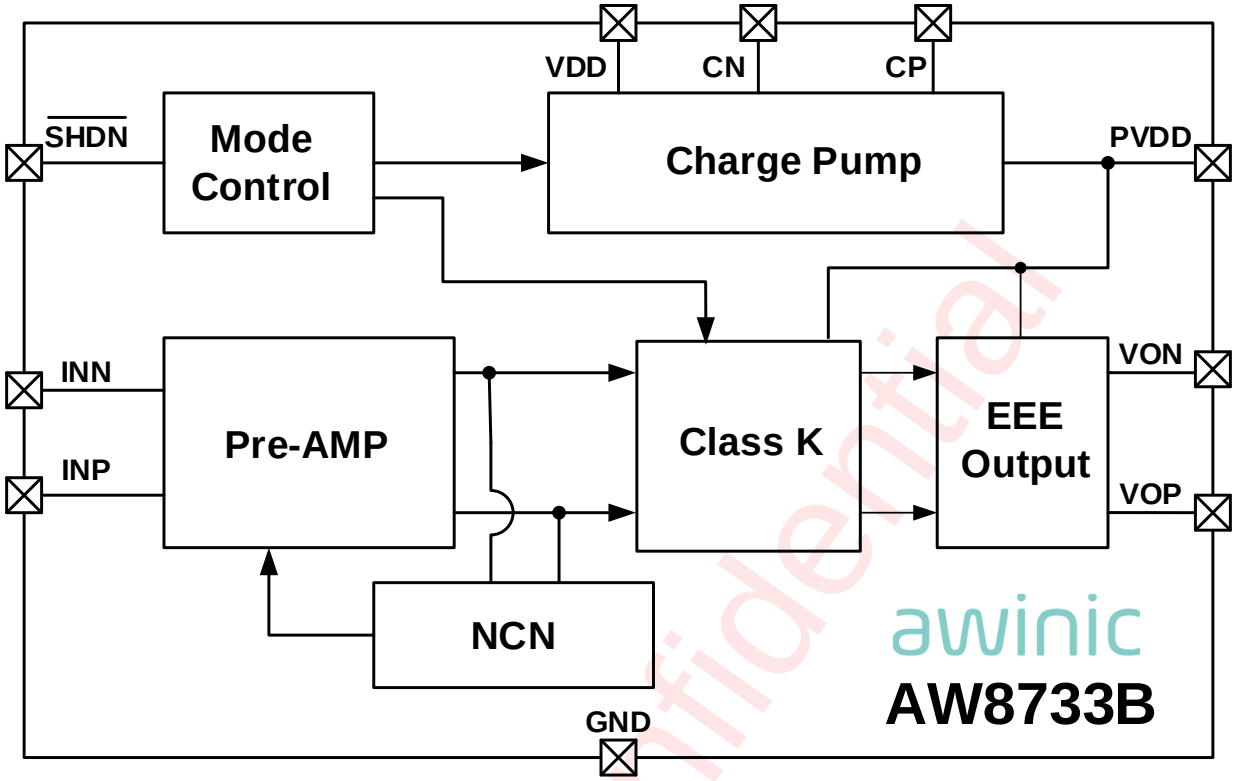


Figure 3 AW8733B Functional Diagram

Typical Application Circuits

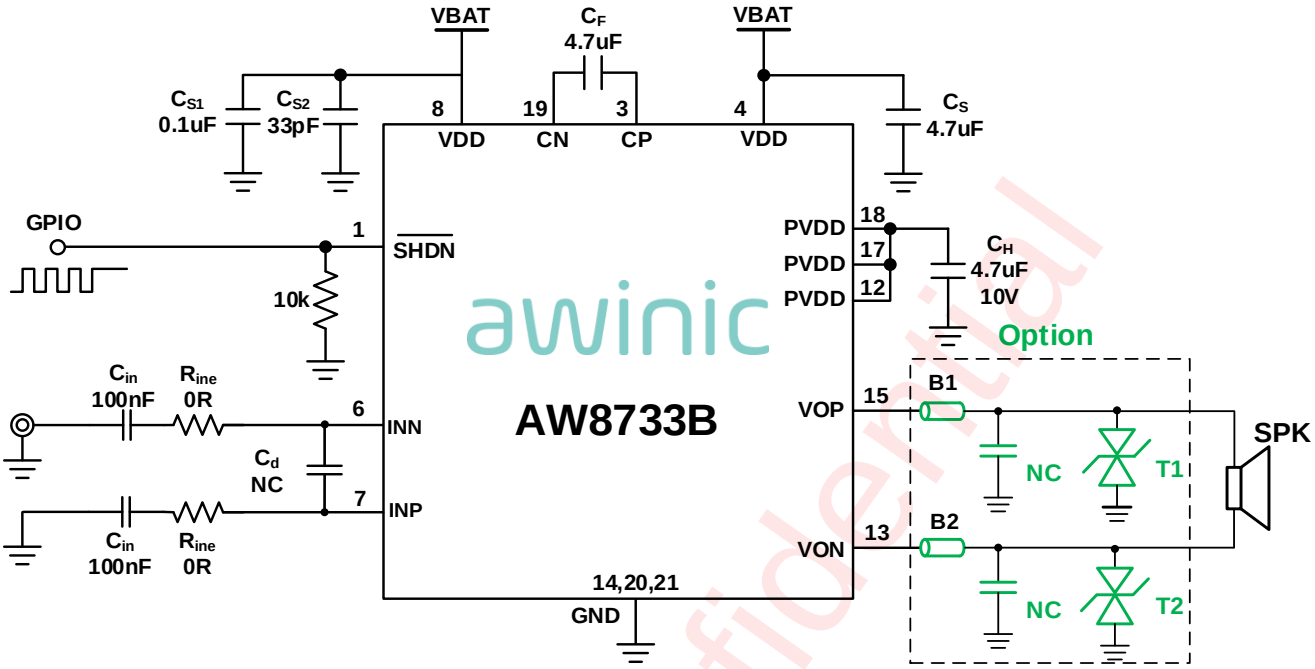


Figure 4 AW8733B Application Diagram With Single-ended Input(Note 1)

Note1:*When single-ended input, audio signal line from audio DAC (HPL or HPR) can arbitrarily connected to either of INN or INP input terminal. The other terminal must be connected to reference ground (HPREF) through input capacitor and resistor. When laying out the board, pin4/pin8 (VDD) must be connected together, and all of them must be connected to VBAT. pin12/pin17/pin18 (PVDD) plates must be connected together. Cs recommends using ceramic capacitors with X7R/X5R, and if using tantalum capacitors, they must be placed in parallel with a ceramic capacitor with a value greater than 1uF near the VDD pin to filter high-frequency interference signals.*

When applying 4Ω speaker，C_H need to be changed from 4.7μF to 22μF.

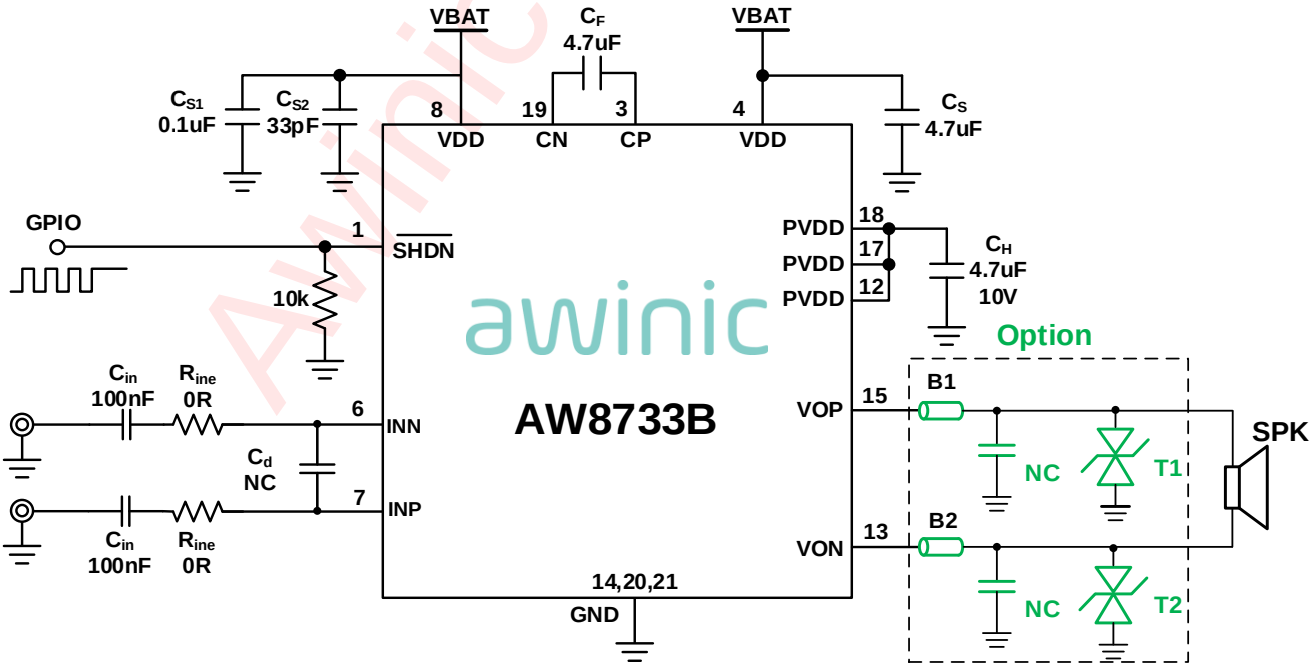


Figure 5 AW8733B Application Diagram With Differential Inputs(Note 2)

Note2: *The input signal must be differential inputs analog signal .When laying out the board, pin4/pin8 (VDD) must be connected together, and all of them must be connected to VBAT. pin12/pin17/pin18 (PVDD) plates must be connected together. Cs recommends using ceramic capacitors with X7R/X5R, and if using tantalum capacitors, they must be placed in parallel with a ceramic capacitor with a value greater than 1uF near the VDD pin to filter high-frequency interference signals.*

When applying 4Ω speaker，C_H need to be changed from 4.7μF to 22μF.

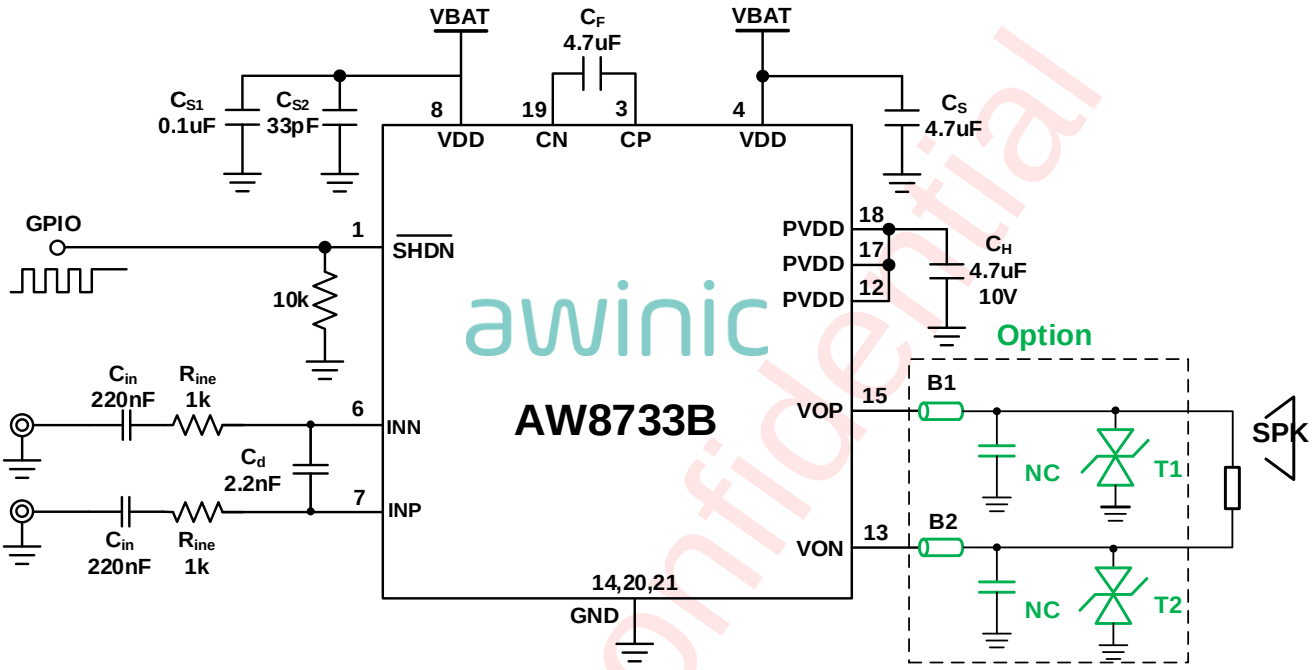


Figure 6 AW8733B Application Diagram With Differential filter capacitor(Note 3)

Note3: *The input signal could be single-ended input or differential inputs analog signal .When laying out the board, pin4/pin8 (VDD) must be connected together, and all of them must be connected to VBAT. pin12/pin17/pin18 (PVDD) plates must be connected together. Cs recommends using ceramic capacitors with X7R/X5R, and if using tantalum capacitors, they must be placed in parallel with a ceramic capacitor with a value greater than 1uF near the VDD pin to filter high-frequency interference signals.*

When the high-frequency noise background of the platform is too large, it can appropriately attenuate a part of the high-frequency input signal (adding a differential filter capacitor), so that the noise from platform is optimized. Please refer to Application Information section for specific design methods.

When applying 4Ω speaker，C_H need to be changed from 4.7μF to 22μF.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW8733BTQR	-40℃～85℃	QFN 3mm x 3mm x 0.75mm - 20L	J9Y5	MSL3	ROHS+HF	6000 units/ Tape and Reel

Absolute Maximum Ratings(Note1)

PARAMETERS	RANGE
Supply voltage V_{DD}	-0.3V to 6V
INP,INN	-0.3V to 6V
$\overline{SHDN}$ Pin Voltage	-0.3V to 6V
PVDD	-0.3V to 7V
VOP,VON	-0.3V to 7V
Package Thermal Resistance θ_{JA}	54℃/W
Operating free-air temperature	-40℃ to 85℃
Maximum Junction Temperature T_{JMAX}	125℃
Storage Temperature Range T_{STG}	-65℃ to 150℃
Lead Temperature (Soldering 10 Seconds)	260℃
ESD Rating(Note 2)	
HBM(human body model)	±2kV
CDM(charged-device model)	±1.5kV
Latch-up	
Test Condition: JESD78F	+IT：200mA -IT：-200mA

***Note1**: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

***Note2**: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2023. Test method of the charge device model: ESDA/JEDEC JS-002-2022.*

Electrical Characteristics

Test Condition : T_A=25°C for typical values (unless otherwise noted)

Parameter		Test conditions		Min	Typ	Max	Unit
V_{DD}	Power Supply			2.5		5.5	V
I_q	Quiescent current	V_{DD}=3.6V			7.5		mA
I_{SD}	Shutdown current	V_{DD}=3.6V,$\overline{SHDN}$=0V			0.1		μA
V_{IH}	$\overline{SHDN}$ high-level input			1.3		V_{DD}	V
V_{IL}	$\overline{SHDN}$ low-level input			0		0.35	V
I_{IH}	$\overline{SHDN}$ high-level input current	$\overline{SHDN}$,V_{DD}=5.5V,V_{IH}=5.8V				100	uA
I_{IL}	$\overline{SHDN}$ low-level input current	$\overline{SHDN}$,V_{DD}=5.5V,V_{IH}= -0.3V				5	uA
T_{SD}	Over temperature protection threshold				160		℃
T_{SDR}	Over temperature protection recovery threshold				120		℃
Charge Pump							
PVDD	Output Voltage	VDD =3.3V to 5.5V,no load		5.8	6.5	7	V
I_{OUT}	Maximum output current					1	A
F1	Switching Frequency	VDD=3V to 5.5V			600		kHz
T_{ST}	Soft-start time	No load,COUT=10uF			1		ms
I_L	PVDD short to GND current limit				300		mA
Class K							
$\|V_{OS}\|$	Output offset voltage	VIN=0V,no load		-30	0	30	mV
R_{ini}	Internal impedance	Mode1			18.5		kΩ
		Mode2			12.2		
		Mode3 and Mode4			5		
F_{OSC}	Modulation Frequency	VDD=2.5V to 5.5V			300		kHz
PSRR	Power supply rejection ratio	VDD=4.2V, Vp-p_sin=200mV	217Hz		80		dB
			1kHz		82		
T_{ON}	Start-up time				28		ms
V_N	Speaker output noise	VDD=4.2V,Mode1			29		μV
THD+N	Total harmonic distortion plus noise	VDD=4.2V,Po=1W,f=1kHz			0.2		%
		VDD=3.6V,Po=1W,f=1kHz			0.2		%
		VDD=4.2V,Po=0.5W,f=1kHz			0.22		%
		VDD=3.6V,Po=0.5W,f=1kHz			0.22		%
PO	Output power	THD+N=10%,f=1kHz, VDD=5V, RL=8Ω+33μH			2.7		W
		THD+N=1%,f=1kHz, VDD=5V, RL=8Ω+33μH			2.2		W
		THD+N=10%,f=1kHz, VDD=4.2V, RL=8Ω+33μH			2.4		W
		THD+N=1%,f=1kHz, VDD=4.2V, RL=8Ω+33μH			2		W
		THD+N=10%,f=1kHz, VDD=3.6V, RL=8Ω+33μH			1.85		W
		THD+N=1%,f=1kHz, VDD=3.6V, RL=8Ω+33μH			1.5		W
		THD+N=10%,f=1kHz, VDD=5V, RL=4Ω+33μH			2.8		W
		THD+N=1%,f=1kHz,			2.55		W

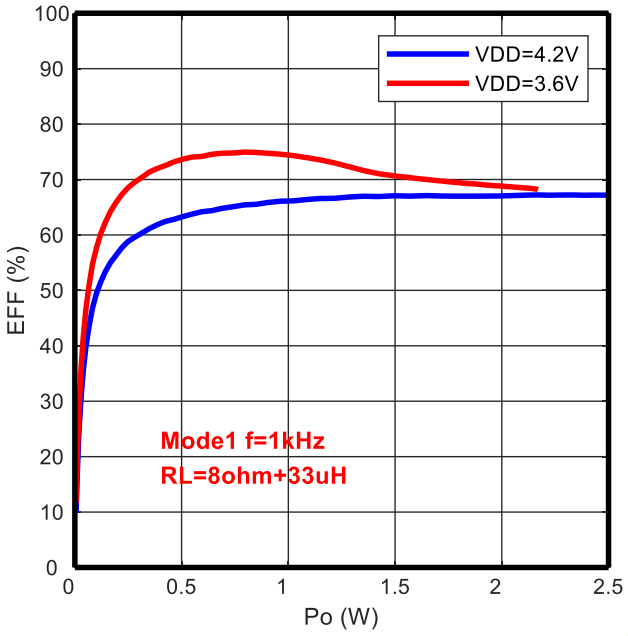
Parameter		Test conditions	Min	Typ	Max	Unit
		VDD=5V, RL=4Ω+33Mh				
		THD+N=10%,f=1kHz, VDD=4.2V, RL=4Ω+33μH		2.4		W
		THD+N=1%,f=1kHz, VDD=4.2V, RL=4Ω+33μH		2.15		W
		THD+N=10%,f=1kHz, VDD=3.6V, RL=4Ω+33μH		1.85		W
		THD+N=1%,f=1kHz, VDD=3.6V, RL=4Ω+33μH		1.6		W
One-wire Pulse Control						
T_H	$\overline{SHDN}$ high level hold time	V_{DD}=2.5V to 5.5V	0.75	2	10	us
T_L	$\overline{SHDN}$ low level hold time	V_{DD}=2.5V to 5.5V	0.75	2	10	us
T_{OFF}	$\overline{SHDN}$ delay time	V_{DD}=2.5V to 5.5V	200			us
NCN(Note1)						
T_{AT}	Attack time	fsin=1kHz		40		ms
T_{RL}	Release time			1.2		s
A_{MAX}	Maximum attenuation gain			-6		dB

Note1: *Attack time is the time when the gain decays by 6dB, and release time is the time when the gain restores by 6dB.*

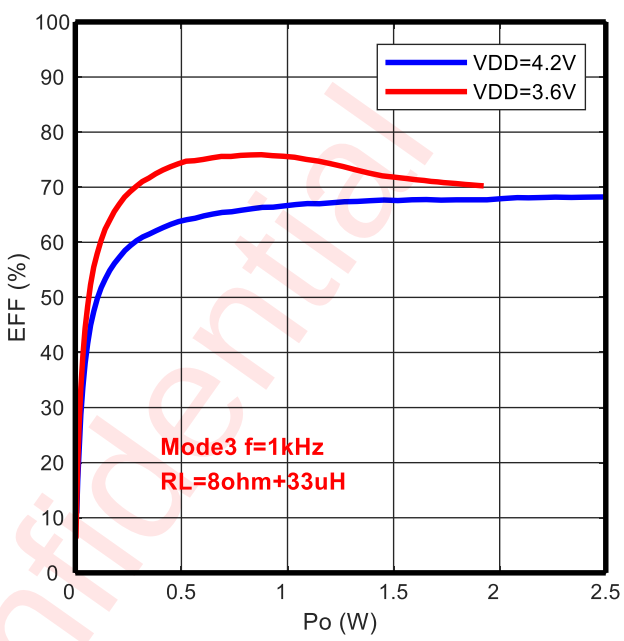
Typical Characteristics

T_A=25°C

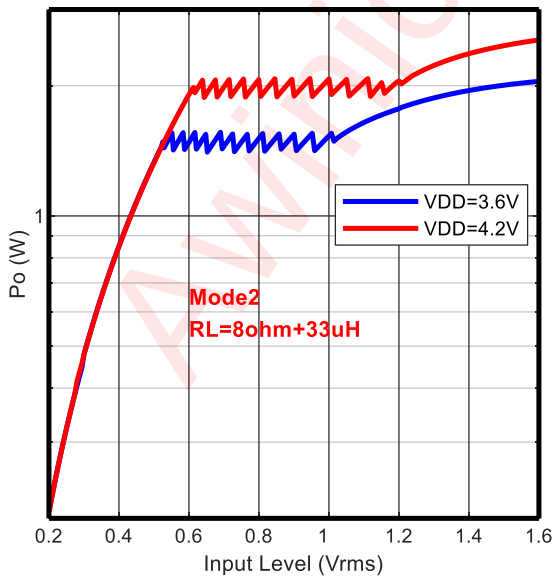
Efficiency VS. Output Power



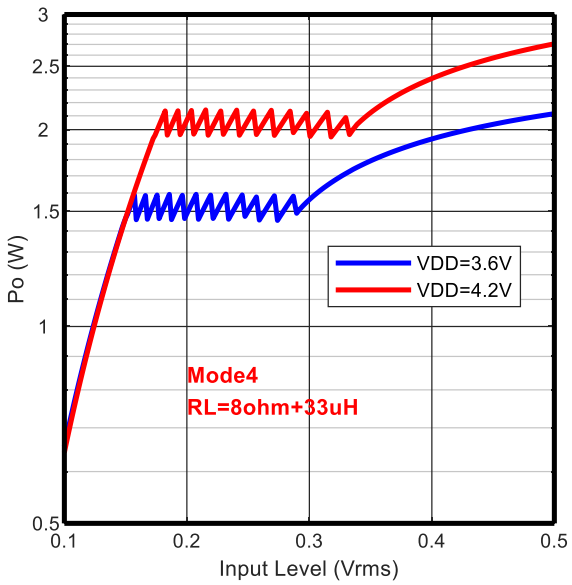
Efficiency VS. Output Power



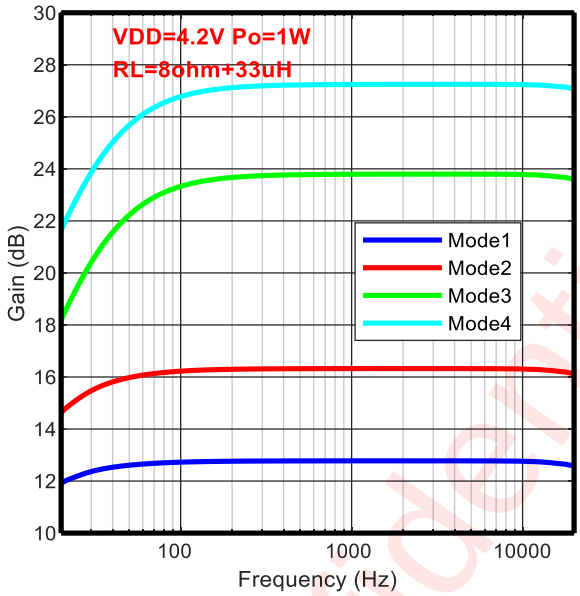
Po VS. Input



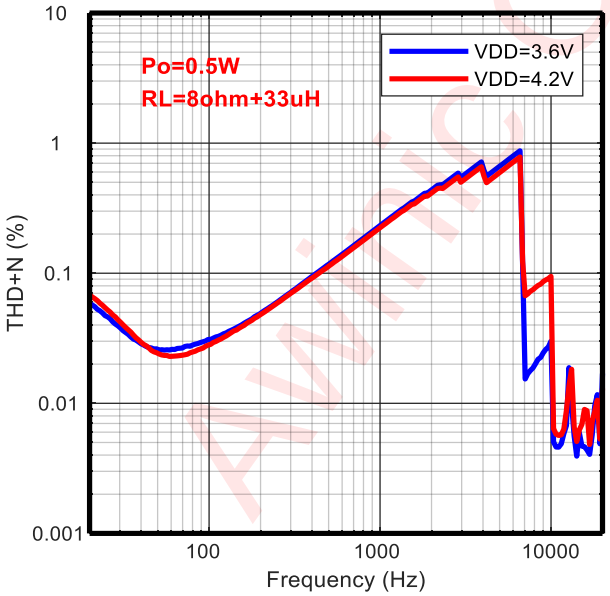
Po VS. Input



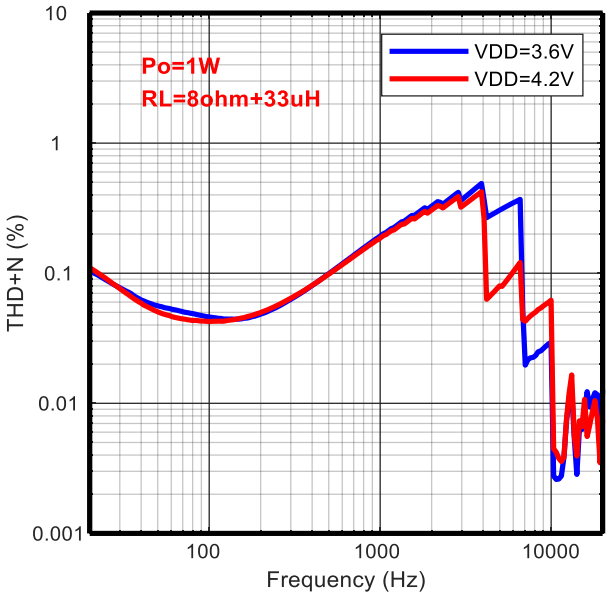
Gain VS. Frequency



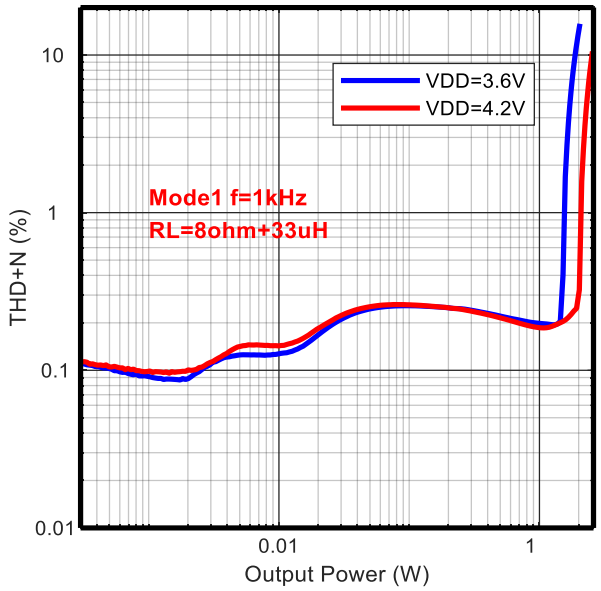
THD+N VS. Frequency



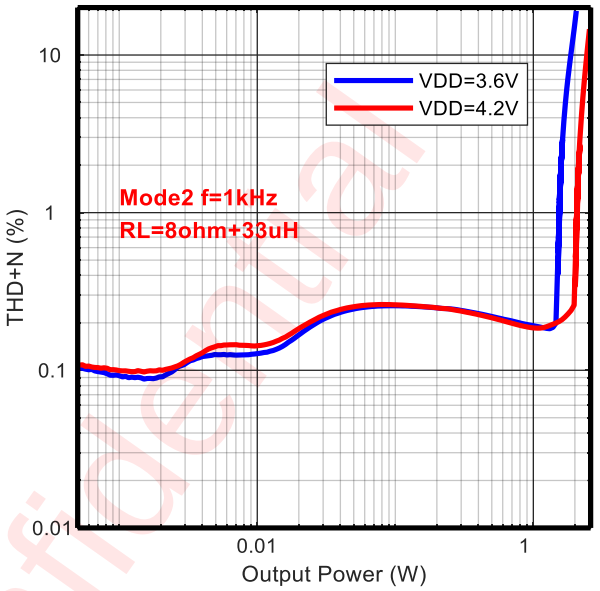
THD+N VS. Frequency



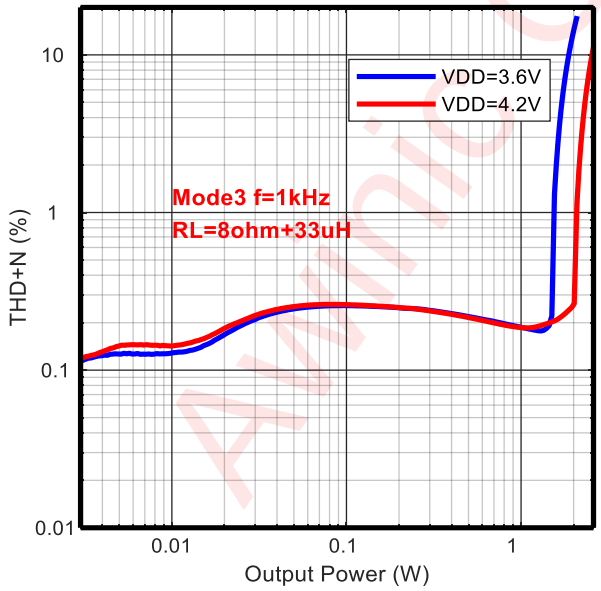
THD+N VS. Output Power



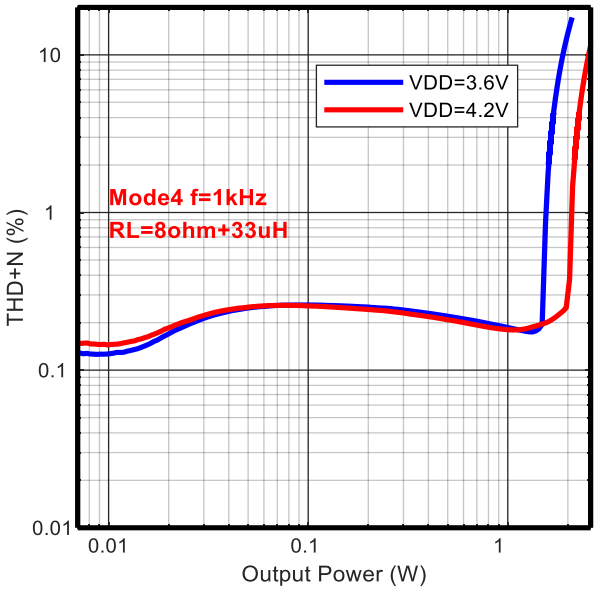
THD+N VS. Output Power



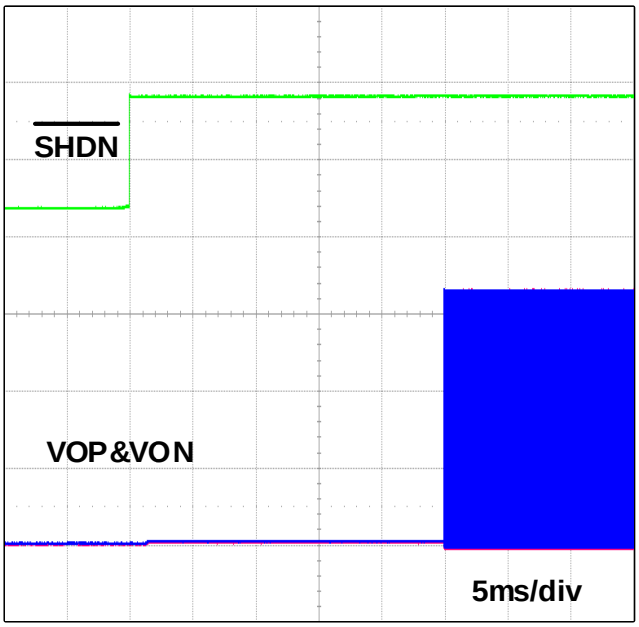
THD+N VS. Output Power



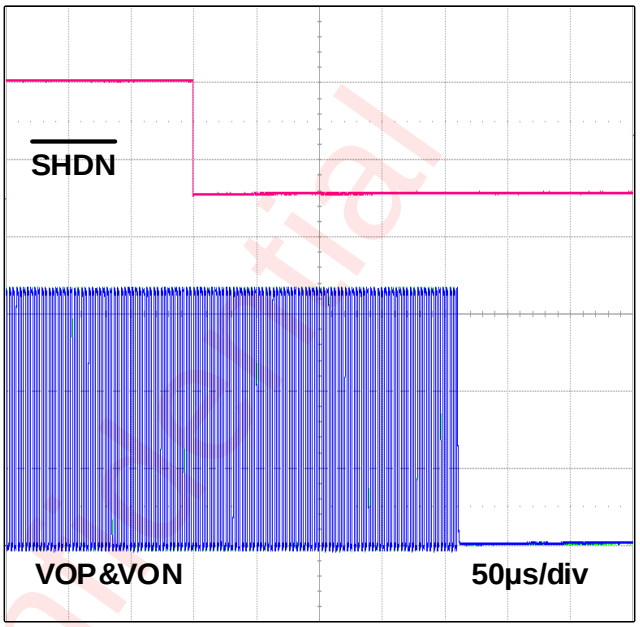
THD+N VS. Output Power



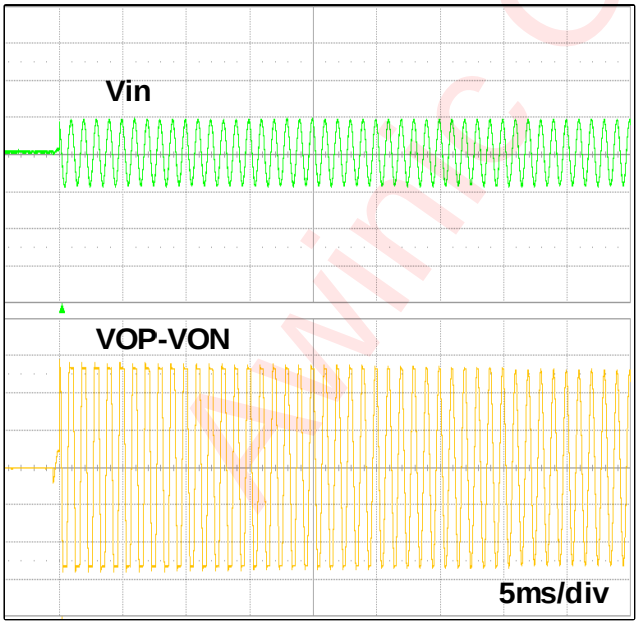
Start-up Sequence



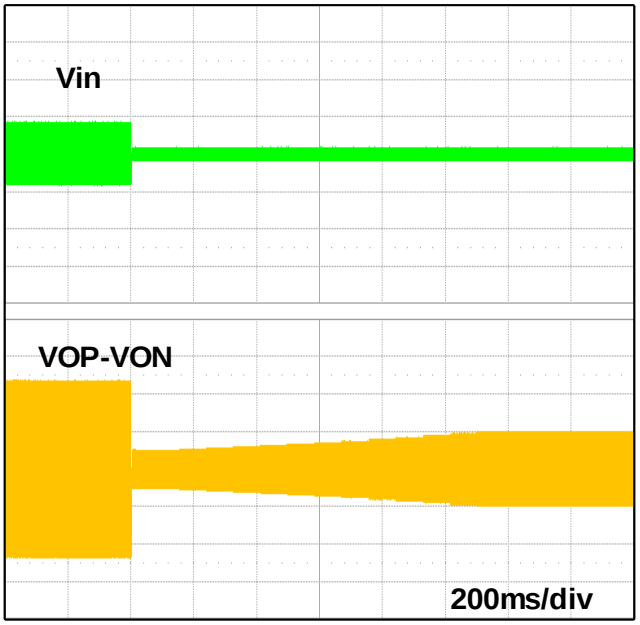
Shutdown Sequence



NCN Attack Timing



NCN Release Timing



Operation

One-wire pulse control

AW8733B select each mode by one-wire pulse control, as shown in figure 7. When $\overline{SHDN}$ pin pull high form shutdown mode, there is one rising edge, AW8733B start to work and set Gain=12dB. When high-low-high signal set to $\overline{SHDN}$ pin, there are two rising edges, AW8733B open NCN function and set Gain=16dB. When there are three rising edges, AW8733B close NCN function and set Gain=24dB. When there are four rising edges, AW8733B open NCN function and set Gain=27.5dB.

As shown in figure 7, when $\overline{SHDN}$ pull down above 500us, AW8733B will enter shutdown mode.

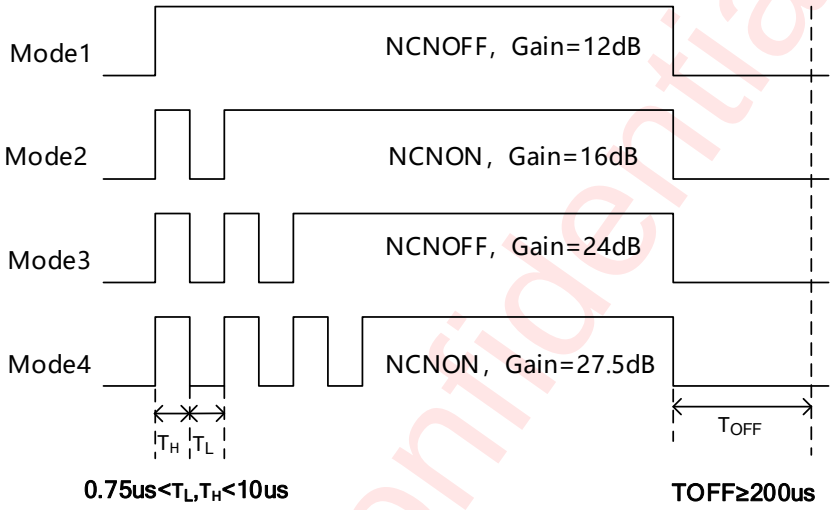


Figure 7 One-Wire Pulse Control

RNS (RF TDD Noise Suppression)

GSM radios transmit using time-division multiple access with 217Hz intervals. The result is an RF signal with strong amplitude modulation at 217Hz and its harmonics that is easily demodulated by audio amplifiers.

In RF applications, improvements to both layout and component selection decrease AW8733B's susceptibility to RF noise and prevent RF signals from being demodulated into audible noise. Minimizing the trace lengths prevents them from functioning as antennas and coupling RF signals into AW8733B. Additional RF immunity can also be obtained from relying on the self-resonant frequency of capacitors as it exhibits the frequency response similar to a notch filter. Depending on the manufacturer, 10pF to 20pF capacitors typically exhibit self resonance at RF frequencies. These capacitors, when placed at the input pins, can effectively shunt the RF noise at the inputs of AW8733B. For these capacitors to be effective, they must have a low-impedance, low-inductance path to the ground plane.

Some RF energy will couple onto audio traces regardless of the effort to prevent this phenomenon from occurring, form audible TDD Noise。AW8733B features a unique RNS technology, which effectively reduces RF energy, attenuates the RF TDD-noise, an acceptable audible level to the customer.

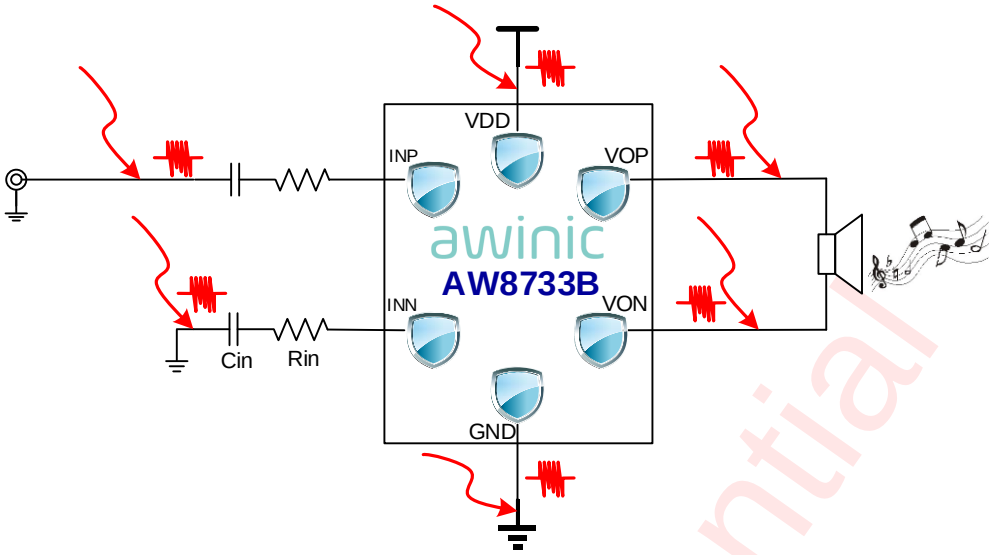


Figure 8 RF Energy Coupling Diagram

NCN

In audio application, output signal will be undesirable distortion caused by too large input and power supply voltage down with battery, and clipped output signal may cause permanent damage to the speaker. AW8733B features unique non-crack-noise (NCN) Function, which adjusts system gain automatically to generate desired output by detecting the “Crack” distortion of output signal, protects the speaker from damage at high power levels and brings the most comfortable listening experience to the customers.

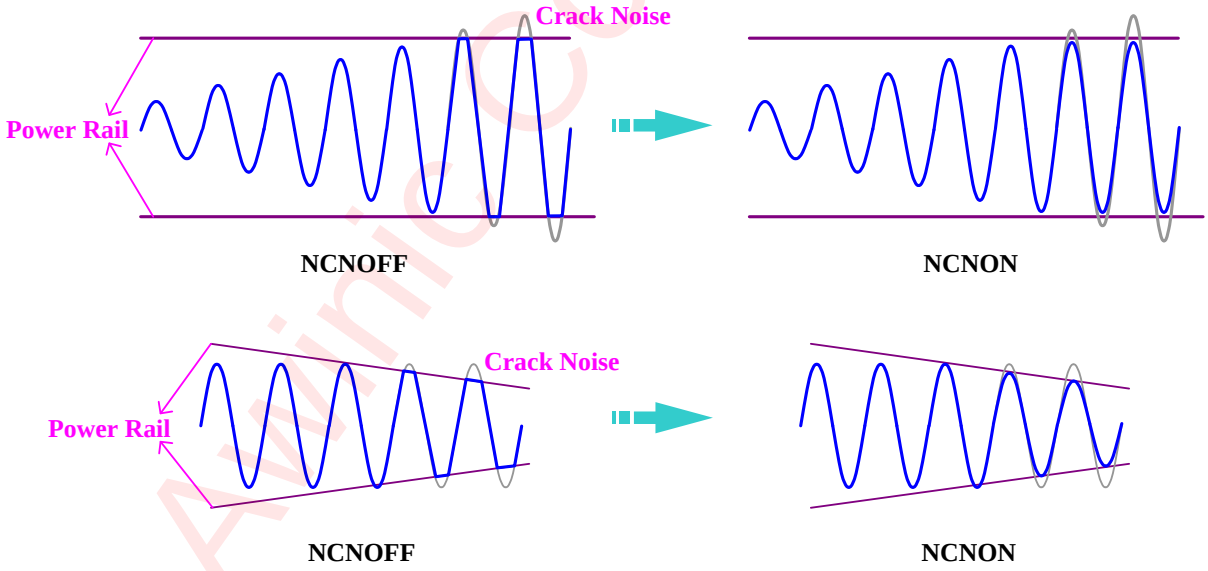


Figure 9 NCN Function Diagram

Attack Time

Attack time is the time it takes for the gain to be reduced by 6dB once the audio signal exceeds the NCN threshold. Fast attack times allow the NCN to react quickly and prevent transients such as symbol crashes from being distorted. However, fast attack times can lead to volume pumping, where the gain reduction and release becomes noticeable, as the NCN cycles quickly. Slower attack times cause the NCN to ignore the fast transients, and instead act upon longer, louder passages. Selecting an attack time that is too slow can lead to increased distortion in the case of the No Clip function. Attack time is set 40ms in AW8733B.

Release Time

Release time is the time it takes for the gain to return from 6dB to its normal level once the audio signal returns below the NCN threshold. A fast release time allows the NCN to react quickly to transients, preserving the original dynamics of the audio source. However, similar to a fast attack time, a fast release time contributes to volume pumping. A slow release time reduces the effect of volume pumping. Release time is set 1.2s in AW8733B.

Filter-Free Modulation Scheme

AW8733B features a filter-free PWM architecture that reduces the LC filter of the traditional Class-D amplifier, increasing efficiency, reducing board area consumption and system cost.

EEE

AW8733B features a unique Enhanced Emission Elimination (EEE) technology, that controls fast transition on the output, greatly reduces EMI over the full bandwidth.

Pop-Click Suppression

AW8733B features unique timing control circuit, that comprehensively suppresses pop-click noise, eliminates audible transients on shutdown, wakeup, and power-up/down.

Protection Function

When a short-circuit occurs between VOP/VON pin and VDD/GND or VOP and VON, the over-current circuit shutdown the device, preventing the device from being damaged. When the condition is removed, AW8733B reactivate itself. When the junction temperature is high, the over-temperature circuit shutdown the device. The circuit switches back to normal operation when the temperature decreases to safe levels .

Application Information

External Input Resistor-R_{ine} (Gain setting)

AW8733B is a differential audio amplifier. The IC integrates two internal input resistors, which 18.5kΩ in mode1,12.2kΩ in mode2, 5kΩ in mode3 and mode4. Take external input resistor R_{ine}=0Ω for an example, gain setting as follows:

Mode1: $A_V = 2.5 * \frac{32k\Omega}{R_{ine}+R_{ini}} = \frac{80k\Omega}{0\Omega+18.5k\Omega} = 4.3V/V$

Mode2: $A_V = 2.5 * \frac{32k\Omega}{R_{ine}+R_{ini}} = \frac{80k\Omega}{0\Omega+12.2k\Omega} = 6.56V/V$

Mode3: $A_V = 2.5 * \frac{32k\Omega}{R_{ine}+R_{ini}} = \frac{80k\Omega}{0\Omega+5k\Omega} = 16V/V$

Mode4: $A_V = 3.8 * \frac{32k\Omega}{R_{ine}+R_{ini}} = \frac{121.6k\Omega}{0\Omega+5k\Omega} = 24.32V/V$

Input Capacitor-C_{in} (Input High-Pass Cut-off Frequency)

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. The input capacitors and input resistors form a high-pass filter with the corner frequency:

$$f_H(-3dB) = \frac{1}{2 * \pi * R_{intotal} * C_{in}} (Hz)$$

Take typical application in Figure 4 as an example:

Mode1:

$$f_H(-3\text{dB}) = \frac{1}{2 * \pi * R_{\text{intotal}} * C_{\text{in}}}(\text{Hz}) = \frac{1}{2 * \pi * 18.5\text{k}\Omega * 100\text{nF}}(\text{Hz}) = 86\text{Hz}$$

Mode2:

$$f_H(-3\text{dB}) = \frac{1}{2 * \pi * R_{\text{intotal}} * C_{\text{in}}}(\text{Hz}) = \frac{1}{2 * \pi * 12.2\text{k}\Omega * 100\text{nF}}(\text{Hz}) = 130\text{Hz}$$

Mode3,Mode4:

$$f_H(-3\text{dB}) = \frac{1}{2 * \pi * R_{\text{intotal}} * C_{\text{in}}}(\text{Hz}) = \frac{1}{2 * \pi * 5\text{k}\Omega * 100\text{nF}}(\text{Hz}) = 318\text{Hz}$$

Input differential filter capacitor-C_d (Input Low-Pass Cut-off Frequency)

The input differential filter capacitor and the input resistor together form a low-pass filter, which can be used to attenuate the high-frequency component of the input signal, when the speaker plays music sound or the high-frequency noise background of the platform is too large, it can appropriately attenuate a part of the high-frequency input signal, so that the music signal is soft and comfortable, and the noise from platform is optimized. The -3dB point of the low-pass filter looks like this:

$$f_L(-3\text{dB}) = \frac{1}{2 * \pi * (R_{\text{ini}} // \text{R}_{\text{ine}}) * 2 * C_d}(\text{Hz})$$

Taking Mode1, R_{ine}=1kΩ, C_d=2.2nF as an example, the input high-pass cut-off frequency is as follows:

$$f_L(-3\text{dB}) = \frac{1}{2 * \pi * (R_{\text{ini}} // \text{R}_{\text{ine}}) * C_d}(\text{Hz}) = \frac{1}{2 * \pi * (18.5k\Omega // 1k\Omega) * 2 * 2.2nF}(\text{Hz}) = 38.1kHz$$

Taking Mode3 ,R_{ine}=1kΩ, C_d=2.2nF as an example, the input high-pass cut-off frequency is as follows:

$$f_L(-3\text{dB}) = \frac{1}{2 * \pi * (R_{\text{ini}} // \text{R}_{\text{ine}}) * C_d}(\text{Hz}) = \frac{1}{2 * \pi * (5k\Omega // 1k\Omega) * 2 * 2.2nF}(\text{Hz}) = 43.4kHz$$

Note:It is recommended to balance the capacitances(C_{in}, C_d) and resistances(R_{ine}) according to the actual application requirements, and the design value of C_{in}/C_d is recommended to be 100:1.

Supply Decoupling Capacitor（C_S）

AW8733B is a high-performance audio amplifier that requires adequate power supply decoupling. Place a low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1μF. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to AW8733B is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the 0.1μF ceramic capacitor, place a 4.7μF capacitor on the VBAT supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

Flying Capacitor（C_F）

The value of the flying capacitor (C_F) affects the load regulation and output resistance of the charge pump. A C_F value that is too small degrades the device's ability to provide sufficient current drive. Increasing the value of C_F improves load regulation and reduces the charge pump output resistance to an extent. A 4.7μF capacitor is recommended.

Hold Capacitor（C_H）

The output capacitor value and ESR directly affect the ripple at PVDD. Increasing C_H reduces output ripple. Likewise, decreasing the ESR of C_H reduces both ripple and output resistance. A 4.7μF@10V capacitor is recommended.

Optional Ferrite Bead Filter

AW8733B passed FCC and CE radiated emissions with no ferrite chip beads and capacitors. Use ferrite chip beads and capacitors if device near the EMI sensitive circuits and/or there are long leads from amplifier to speaker, placed as close as possible to the output pin. The output(VOP/VON) can reserve ESD devices, used to improve ESD protection capabilities.

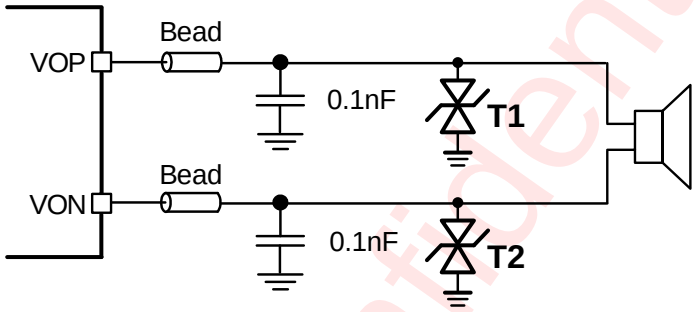
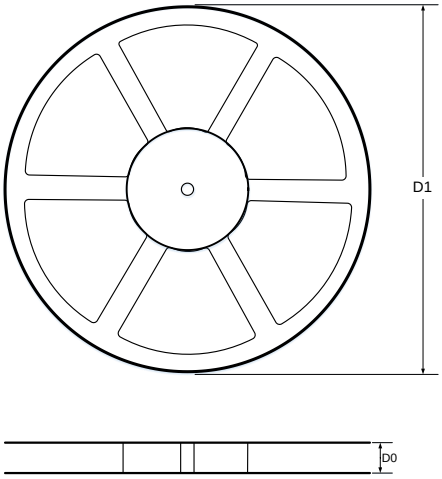


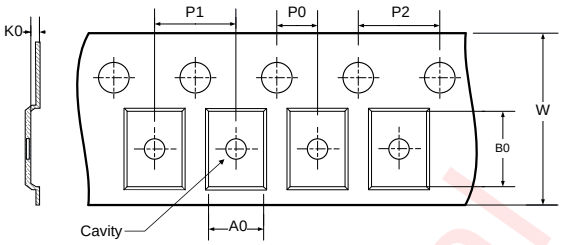
Figure 10　　Typical Output Bead and Capacitor Application

Tape And Reel Information

REEL DIMENSIONS

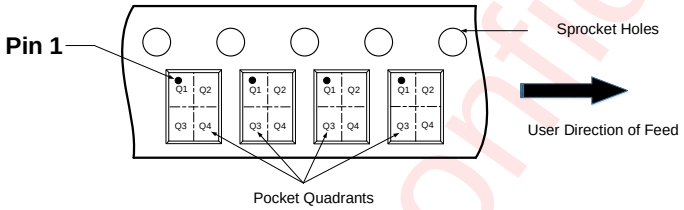


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



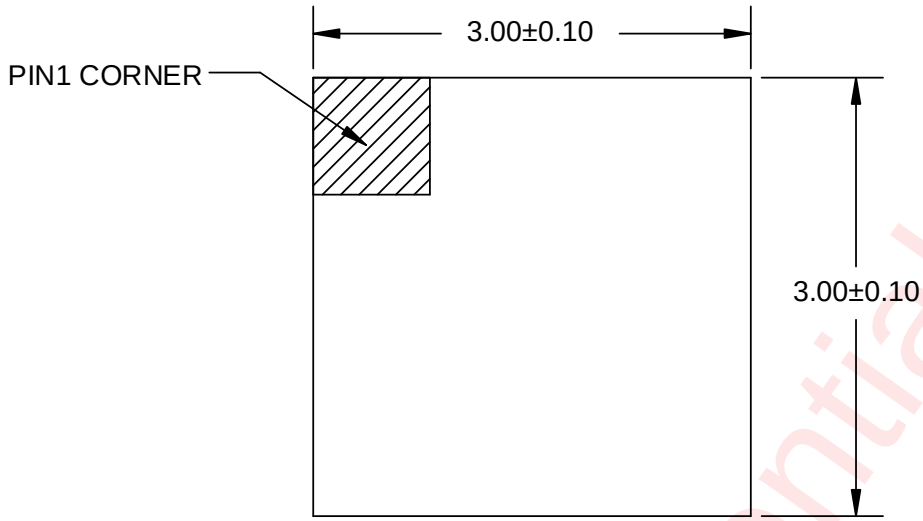
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

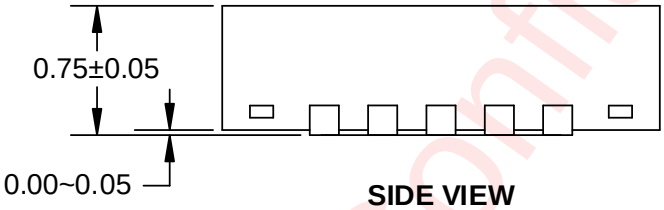
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330.0	12.50	3.30	3.30	1.10	2.00	8.00	4.00	12.00	Q1

All dimensions are nominal

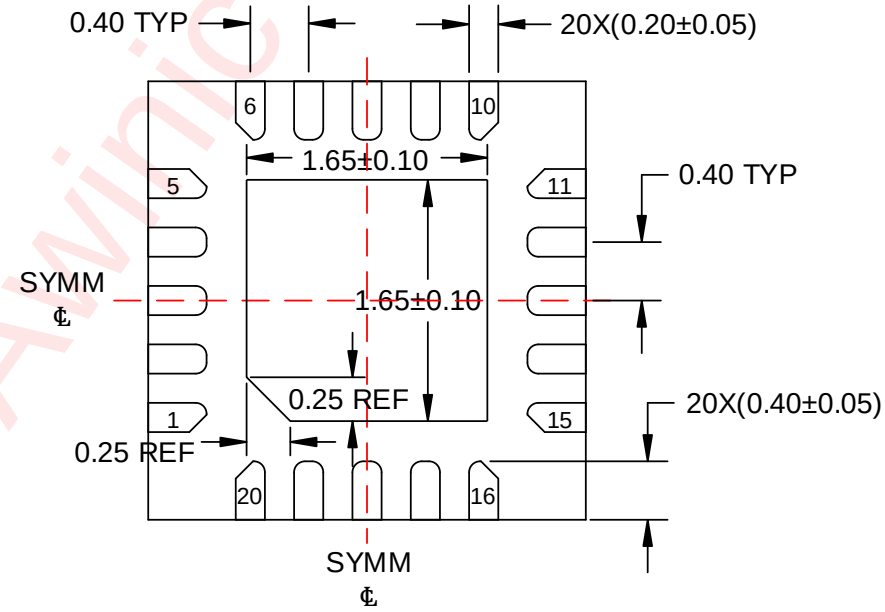
Package Description



TOP VIEW



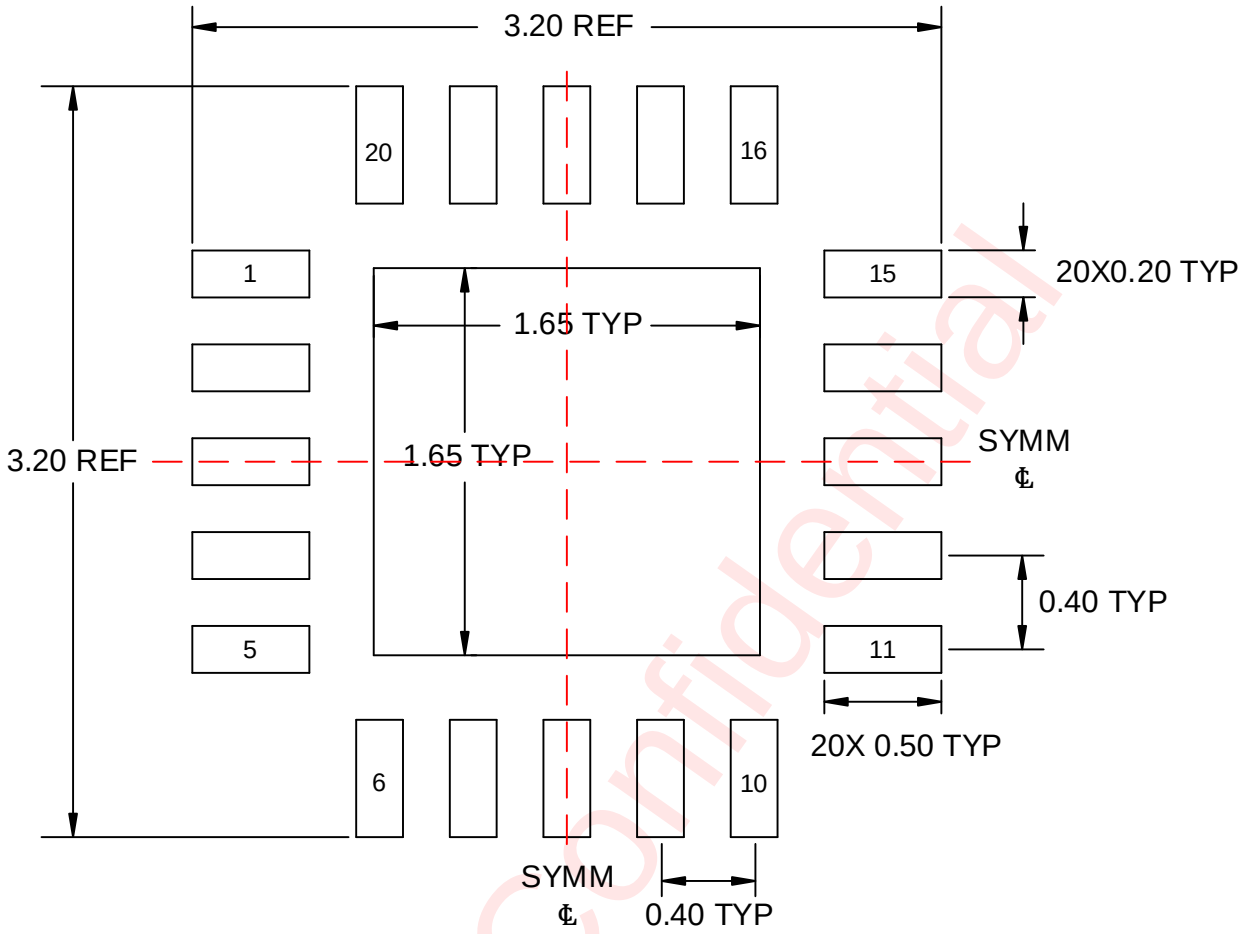
SIDE VIEW

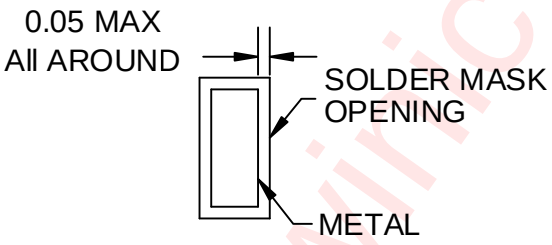


BOTTOM VIEW

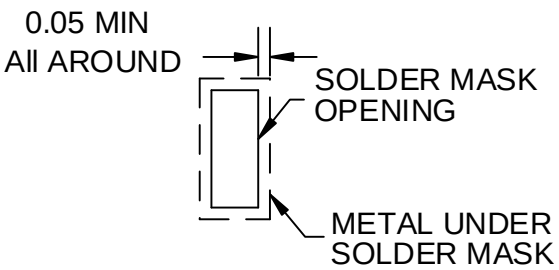
Unit：mm

Land Pattern Data





NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Jan. 2024	Officially released.
V1.1	Jul. 2024	Update electrical and typical characteristics.
V1.2	Dec. 2024	Added description of the input differential filter capacitor and application circuit.
V1.3	Oct.2025	Corrected the gain calculation formula on page 15.

Disclaimer

All trademarks are the property of their respective owners. Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.

