

1. Description

The GS6551/5552 amplifier is single/dual/quad supply, micro-power, zero-drift CMOS operational amplifiers, the amplifiers offer bandwidth of 1.8MHz, rail-to-rail inputs and outputs, and single-supply operation from 1.8V to 5.5V. GS6551/5552 uses chopper stabilized technique to provide very low offset voltage (less than 5 μ V maximum) and near zero drift over temperature. Low quiescent supply current of 220 μ A per amplifier and very low input bias current of 20pA make the devices an ideal choice for low offset, low power consumption and high impedance applications. The GS655X offers excellent CMRR without the crossover associated with traditional complementary input stages. This design results in superior performance for driving analog-to-digital converters (ADCs) without degradation of differential linearity.

3. Applications

- Transducer Application
- Temperature Measurements
- Electronics Scales

2. Features

- Single-Supply Operation from +1.8V ~ +5.5V
- Rail-to-Rail Input / Output
- Gain-Bandwidth Product: 1.8MHz (Typ@25°C)
- Low Input Bias Current: 20pA (Typ@25°C)
- Low Offset Voltage: 5 μ V (Max @25°C)
- Quiescent Current: 220 μ A per Amplifier (Typ)
- Operating Temperature: -45°C ~ +125°C
- Zero Drift: 0.005 μ V/ oC (Typ)

- Handheld Test Equipment
- Battery-Powered Instrumentation



4. Pinning Information

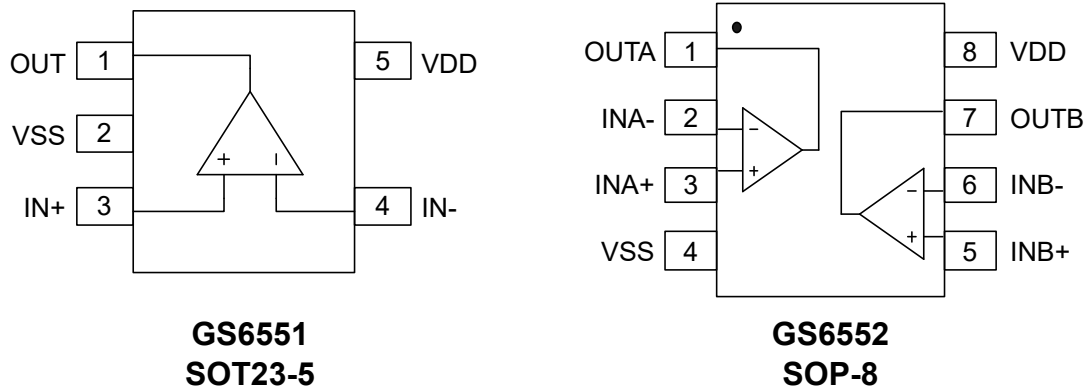


Figure 1. Pin Assignment Diagram



5. Absolute Maximum Ratings

Condition	Min	Max
Power Supply Voltage (V_{DD} to V_{SS})	-0.5V	+7.5V
Analog Input Voltage (IN+ or IN-)	$V_{SS}-0.5V$	$V_{DD}+0.5V$
PDB Input Voltage	$V_{SS}-0.5V$	+7V
Operating Temperature Range	-45°C	+125°C
Junction Temperature	+160°C	
Storage Temperature Range	-55°C	+150°C
Lead Temperature (soldering, 10sec)	+260°C	

6. Package Thermal Resistance ($T_A=+25^\circ\text{C}$)

Condition	Ratings
SOP-8, θ_{JA}	125°C/W
MSOP-8, θ_{JA}	216°C/W
SOT23-5, θ_{JA}	190°C/W

7. ESD Susceptibility

Condition	Ratings
HBM	6KV
MM	400V



8. Electrical characteristics

$V_S=+5V$, $V_{CM}=+2.5V$, $V_O=+2.5V$, $T_A=+25^\circ C$, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Offset Voltage	V_{OS}			1	5	μV
Input Bias Current	I_B			20		pA
Input Offset Current	I_{OS}			10		pA
Common-Mode Rejection Ratio	CMRR	$V_{CM}=0V$ to $5V$		110		dB
Large Signal Voltage Gain	A_{VO}	$R_L=10k\Omega$, $V_O=0.3V$ to $4.7V$		145		dB
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			5	50	nV/ $^\circ C$
Output Voltage High	V_{OH}	$R_L=100k\Omega$ to $-V_S$		4.998		V
		$R_L=10k\Omega$ to $-V_S$		4.994		V
Output Voltage Low	V_{OL}	$R_L=100k\Omega$ to $+V_S$		2		mV
		$R_L=10k\Omega$ to $+V_S$		5		mV
Short Circuit Limit	I_{SC}	$R_L=10k\Omega$ to $-V_S$		60		mA
Output Current	I_O			65		mA
Power Supply Rejection Ratio	PSRR	$V_S=2.5V$ to $5.5V$		115		dB
Quiescent Current	I_Q	$V_O=0V$, $R_L=0\Omega$		220		μA
Gain-Bandwidth Product	GBP	$G=+100$		1.8		MHz
Slew Rate	SR	$R_L=10k\Omega$		0.95		V/ μs
Overload Recovery Time				0.1		ms
Voltage Noise	e_n p-p	0Hz to 10Hz		0.3		μV_{P-P}
Voltage Noise Density	e_n	$f=1kHz$		38		nV/ \sqrt{Hz}

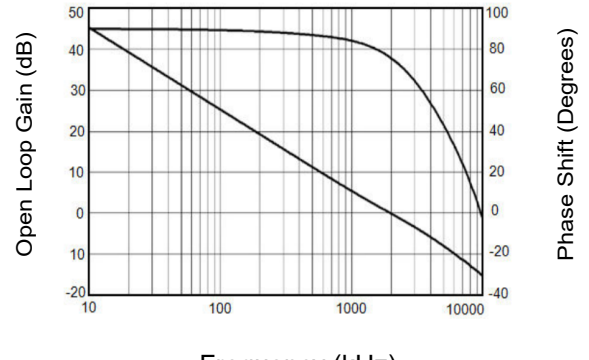
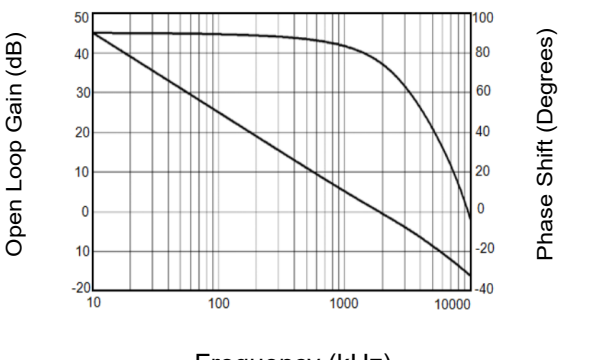
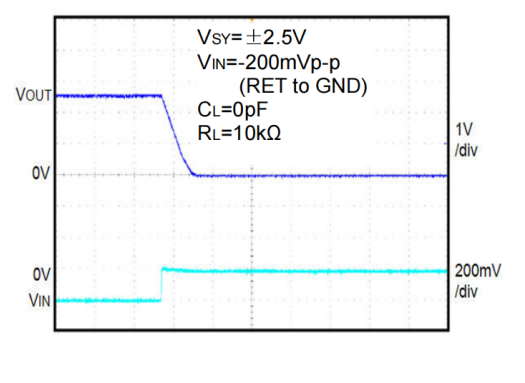
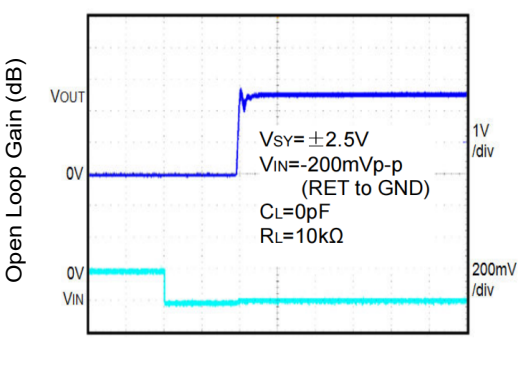
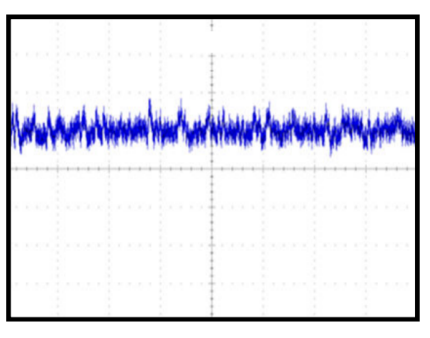
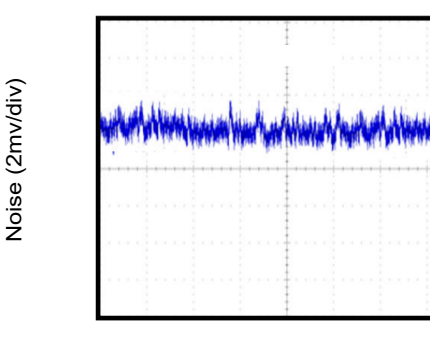


9.1 Typical characteristic

<p>Figure 1: Large Signal Transient Response at +5V</p>	<p>Figure 2: Large Signal Transient Response at +2.5V</p>
<p>Figure 3: Small Signal Transient Response at +5V</p>	<p>Figure 4: Small Signal Transient Response at +2.5V</p>
<p>Figure 5: Closed Loop Gain vs. Frequency at +5V</p>	<p>Figure 6: Closed Loop Gain vs. Frequency at +2.5V</p>

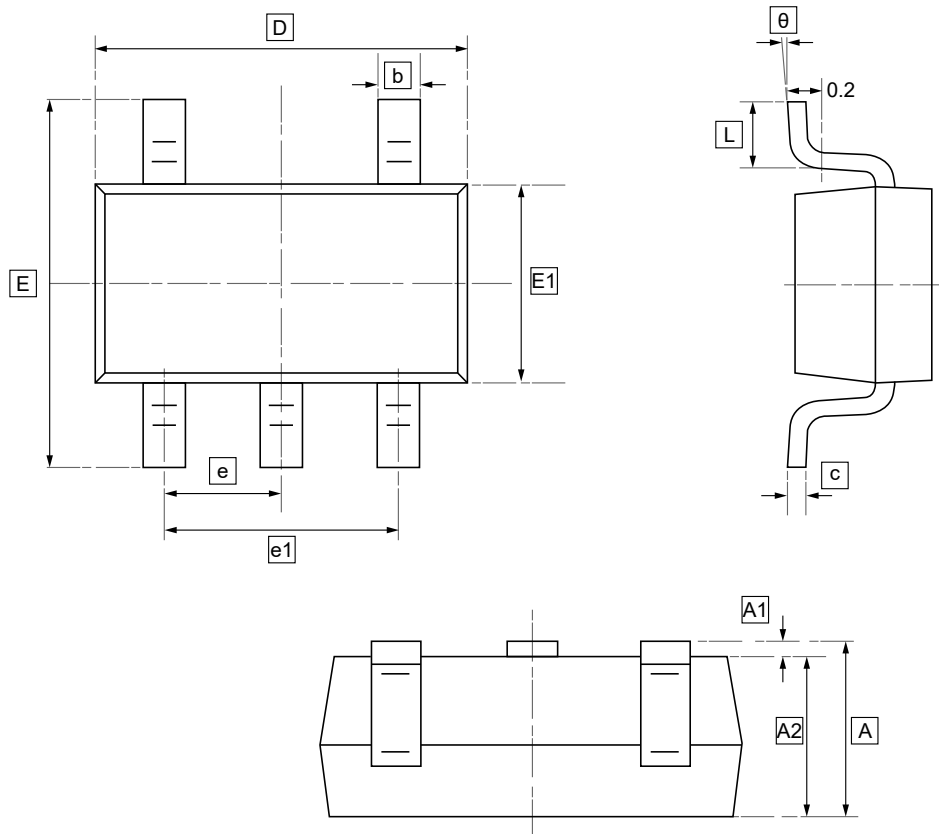


9.2 Typical characteristic

	
<p>Figure 7: Open Loop Gain, Phase Shift vs. Frequency at +5V</p>	<p>Figure 8: Open Loop Gain, Phase Shift vs. Frequency at +2.5V</p>
	
<p>Figure 9: Positive Overvoltage Recovery</p>	<p>Figure 10: Negative Overvoltage Recovery</p>
	
<p>Figure 11: 0.1Hz to 10Hz Noise at +5V</p>	<p>Figure 12: 0.1Hz to 10Hz Noise at +2.5V</p>



10.1 SOT-23-5 Package Outline Dimensions

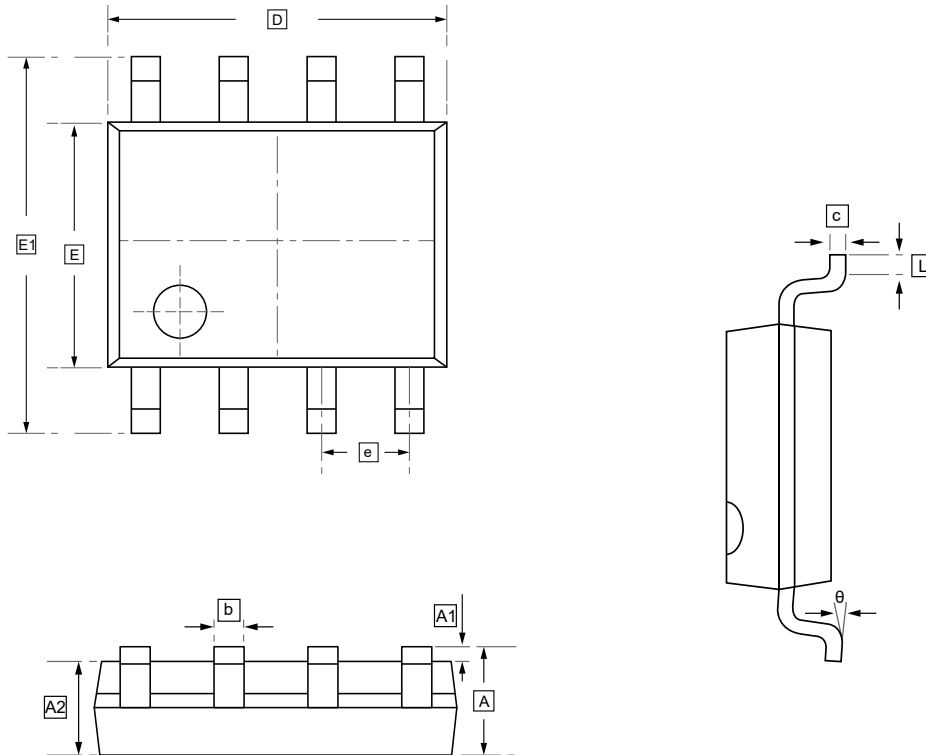


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E1	E	e	e1	L	θ
Min	1.050	0.000	1.050	0.300	0.100	2.820	1.500	2.650	0.950	1.800	0.300	0°
Max	1.250	0.100	1.150	0.500	0.200	3.020	1.700	2.950	BSC	2.000	0.600	8°



10.2 SOP-8 Package Outline Dimensions

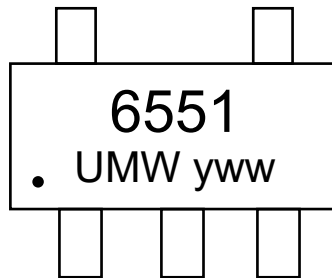


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°



11. Ordering Information



yww: Batch Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW GS6551-TR	6551	SOT23-5	3000	Tape and reel
UMW GS6552-SR	6552	SOP-8	3000	Tape and reel



12.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.