SiHB12N65E-VB Datasheet

N-Channel 650V (D-S) Super Junction Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	650	
$R_{DS(on)}$ at 25 °C (Ω)	V_{GS} = 10 V	0.330

FEATURES

- Low figure-of-merit (FOM) R_{on} x Q_g
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)

RoHS

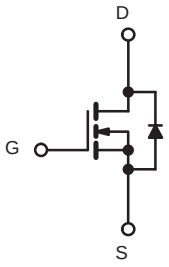
APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting

TO-263



Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage			V_{DS}	650	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	13	A
		T_C = 100 °C		8	
Pulsed Drain Current [a]			I_{DM}	39	
Linear Derating Factor				1.67	W/°C
Single Pulse Avalanche Energy [b]			E_{AS}	900	mJ
Maximum Power Dissipation			P_D	150	W
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	T_J = 125 °C		dV/dt	50	V/ns
Reverse Diode dV/dt [d]				4.5	
Soldering Recommendations (Peak Temperature) [c]	for 10 s			260	°C

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature.
b. V_{DD} = 100 V, starting T_J = 25 °C, L = 30 mH, R_g = 25 Ω, I_{AS} = 6A
c. 1.6 mm from case.
d. $I_{SD} \leq I_D$, dI/dt = 100 A/μs, starting T_J = 25 °C.

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.7	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	650	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.75	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	3	-	5	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
		V_{GS} = ± 30 V	-	-	± 1	µA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 650V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 520 V, V_{GS} = 0 V, T_J = 125 °C	-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 4.5 A	-	0.330	-	Ω
Forward Transconductance	g_{fs}	V_{DS} = 30 V, I_D = 8 A	-	5.6	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	1900	-	pF
Output Capacitance	C_{oss}		-	80	-	
Reverse Transfer Capacitance	C_{rss}		-	4	-	
Effective Output Capacitance, Energy Related [a]	$C_{o(er)}$	V_{DS} = 0 V to 520 V, V_{GS} = 0 V	-	63	-	
Effective Output Capacitance, Time Related [b]	$C_{o(tr)}$		-	213	-	
Total Gate Charge	Q_g	V_{GS} = 10 V; I_D = 8 A, V_{DS} = 520 V	-	49	7 0	nC
Gate-Source Charge	Q_{gs}		-	15	-	
Gate-Drain Charge	Q_{gd}		-	1 9	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 520 V, I_D = 8 A, V_{GS} = 10 V, R_g = 9.1 Ω	-	18	25	ns
Rise Time	t_r		-	24	55	
Turn-Off Delay Time	$t_{d(off)}$		-	48	70	
Fall Time	t_f		-	25	40	
Gate Input Resistance	R_g	f = 1 MHz, open drain	-	0.8	-	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	13	A
Pulsed Diode Forward Current	I_{SM}		-	-	39	
Diode Forward Voltage	V_{SD}	T_J = 25 °C, I_S = 8 A, V_{GS} = 0 V	-	-	1.5	V
Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = I_S = 8 A, dI/dt = 100 A/µs, V_R = 400 V	-	475	-	ns
Reverse Recovery Charge	Q_{rr}		-	5.8	-	µC
Reverse Recovery Current	I_{RRM}		-	35	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

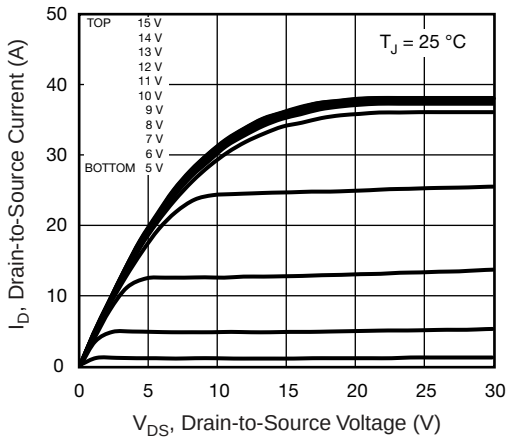


Fig. 1 - Typical Output Characteristics

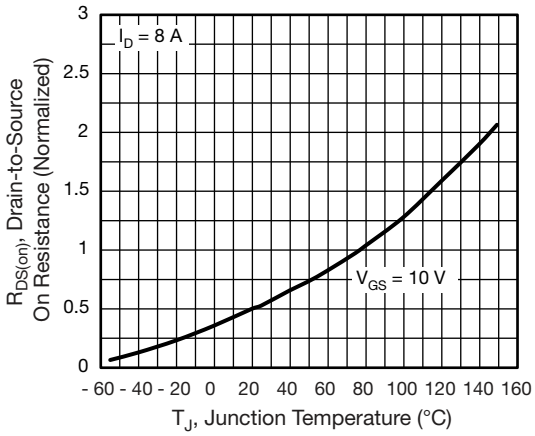


Fig. 4 - Normalized On-Resistance vs. Temperature

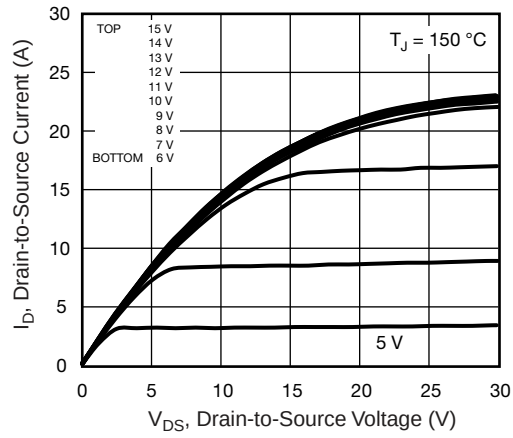


Fig. 2 - Typical Output Characteristics

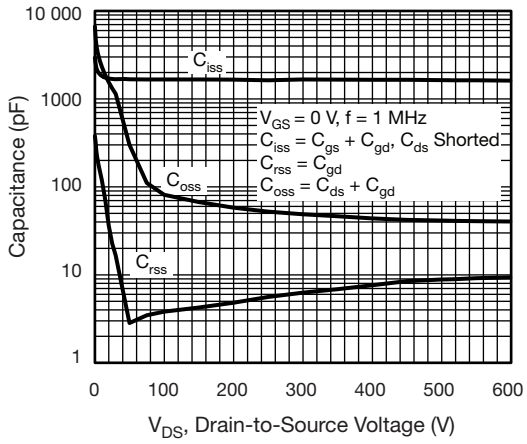


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

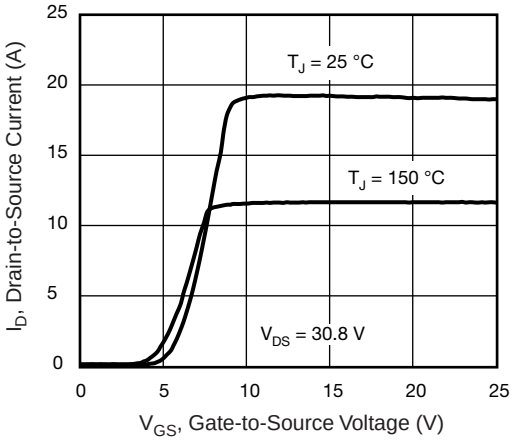


Fig. 3 - Typical Transfer Characteristics

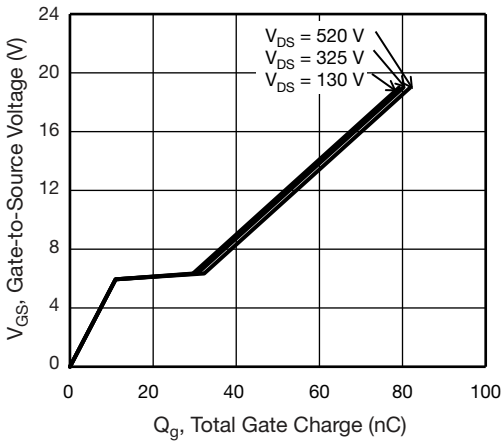


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

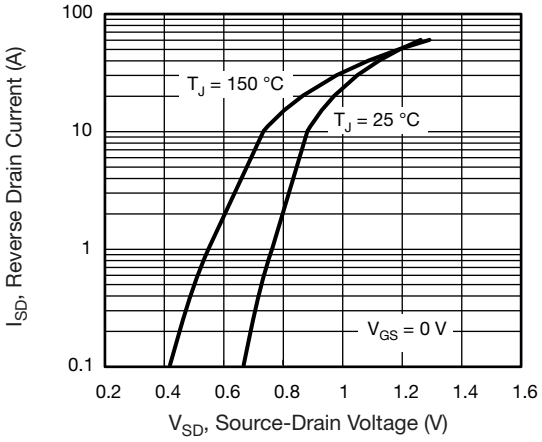


Fig. 7 - Typical Source-Drain Diode Forward Voltage

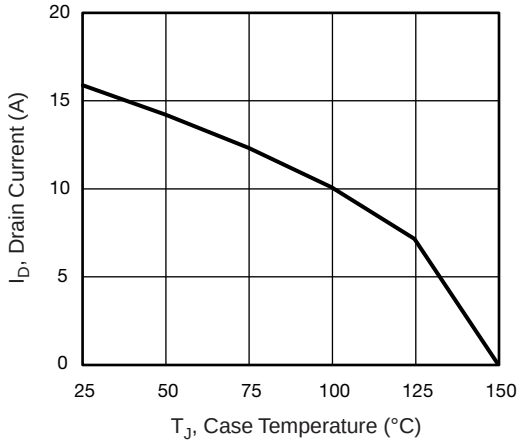


Fig. 9 - Maximum Drain Current vs. Case Temperature

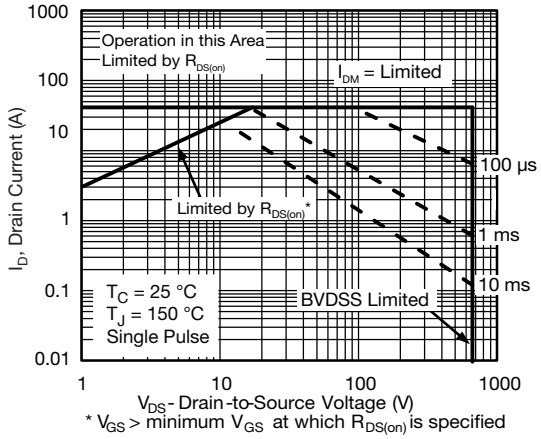


Fig. 8 - Maximum Safe Operating Area

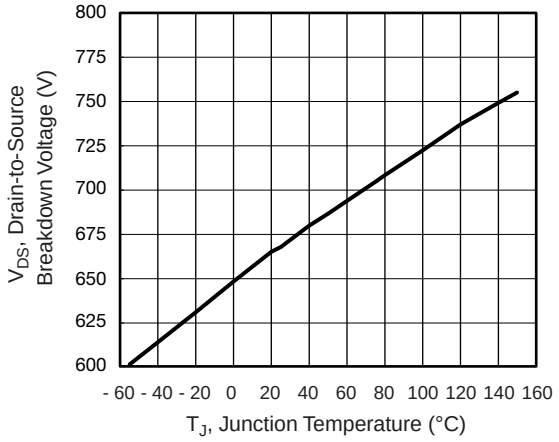


Fig. 10 - Temperature vs. Drain-to-Source Voltage

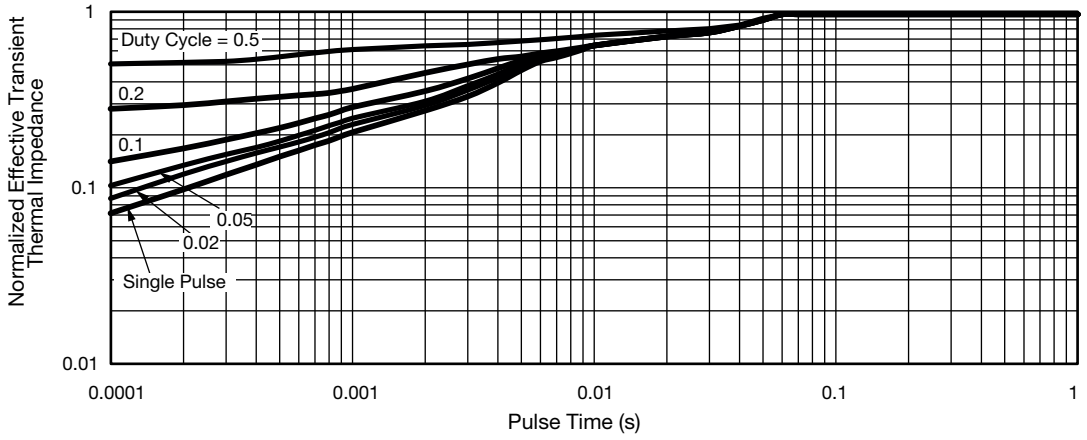


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

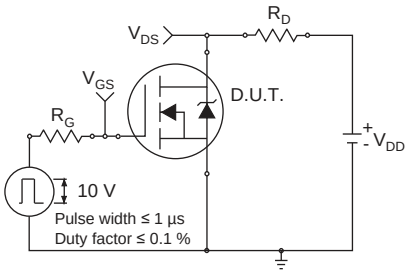


Fig. 12 - Switching Time Test Circuit

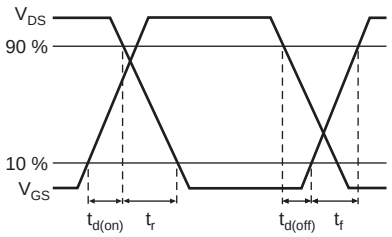


Fig. 13 - Switching Time Waveforms

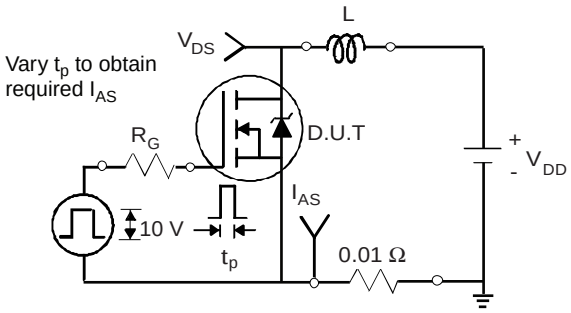


Fig. 14 - Unclamped Inductive Test Circuit

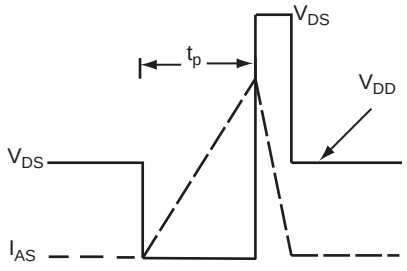


Fig. 15 - Unclamped Inductive Waveforms

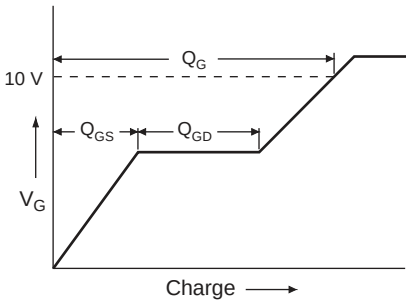


Fig. 16 - Basic Gate Charge Waveform

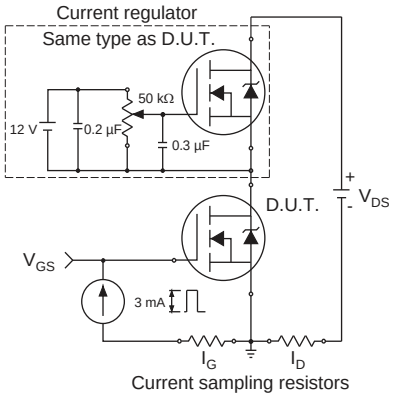
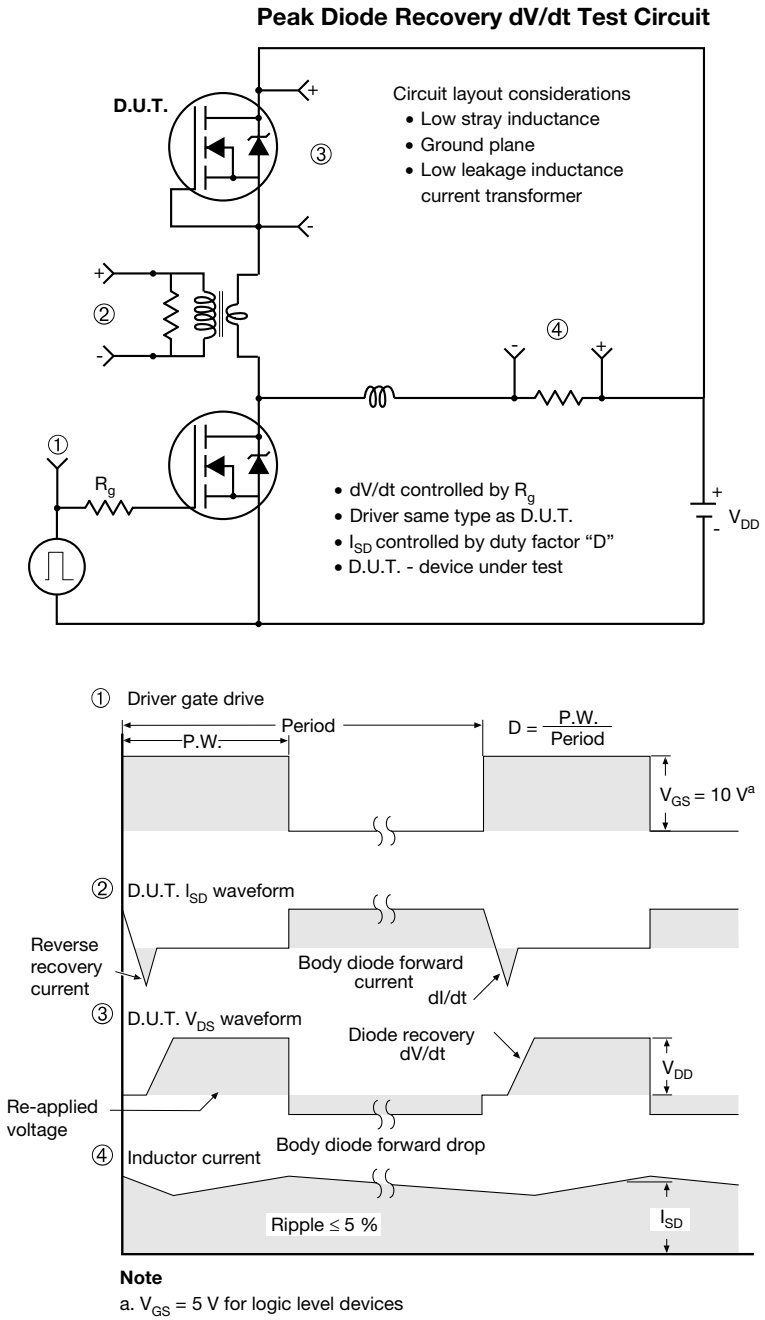


Fig. 17 - Gate Charge Test Circuit

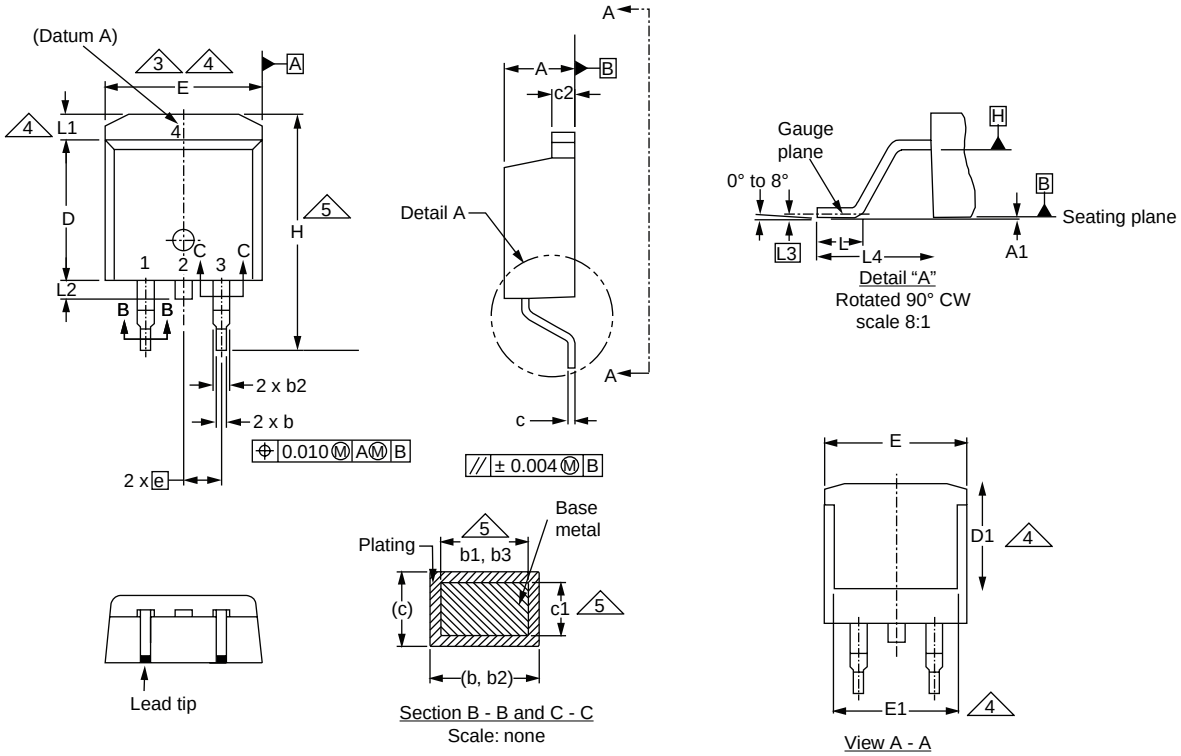


Note

a. V_{GS} = 5 V for logic level devices

Fig. 18 - For N-Channel

TO-263AB (HIGH VOLTAGE)



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

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