MC12G MC12T

Very High Frequency, Dual-Channel, Single-Grounded Digital Capacitive Sensor

1. Overview

The MC12G and MC12T are high-integration dual-channel capacitive sensor that measure single-ended grounded-capacitance. These sensors are directly connected to the capacitance plates under test, detecting minute capacitance variations through very-high-frequency (VHF) resonant excitation and signal processing. The excitation frequency ranges from 10MHz to 100MHz, with a 16-bit digital output for capacitance measurement, achieving a maximum resolution of 0.5fF. Featuring a fully digital design, the sensors support up to 1MHz I2C communication rates for configuration and data transfer. With an internal regulator (LDO), the sensor can operate across a wide input voltage range. Additionally, the sensor incorporates temperature sensing circuits for thermal compensation and other temperature monitoring applications.

Capacitive sensing achieves dielectric detection of various substances through electrode coordination, representing a non-contact detection technology with low power consumption, cost-effectiveness, and high resolution. Unlike traditional RC oscillator-based capacitive sensing structures for touch sensing, MC12G and MC12T employ VHF LC-resonance method that enhances electric field penetration. The sensor's frequency calculation is fully digitized through its internal digital signal processing unit, enabling flexible configuration of multiple operating modes. The MC12T features a simplified SOP8 package for cost-effective dual-channel capacitance detection, while the MC12G adopts a compact QFN16 package with comprehensive internal control mechanisms.

Compared with similar domestic and international products, MC12G and MC12T demonstrate superior performance in capacitance excitation frequency, extended non-contact measurement range, expanded operating voltage range, and flexible configuration of reference frequency and operational modes. The sensor integrates temperature sensing signals for thermal compensation, featuring independent dual-channel measurement circuits that enable mutual reference compensation, along with configurable automatic alarm algorithm and logic. This compact, cost-effective solution is widely applicable in smart home devices for level detection, proximity sensing, and touch control applications, while also serving industrial inspection scenarios including automotive fluid monitoring, water immersion detection, food safety testing, and soil moisture measurement.

2. Features

- Capacitance measurement range: 0 to 150 pF
- Temperature range: -55℃ to +125℃
- Frequency range: 10MHz to 100MHz
- Frequency resolution: up to 15-bit
- Power supply voltage range: 2.0V to 5.5V
- Conversion time: 1ms to 100ms (configurable)
- Peak measurement current: 1.3mA to 8.3mA (configurable)
- Sleep mode current: 50nA
- Shut-down mode current: 40nA
- Average power consumption: 7.5μA@1Hz
- QFN16/SOP8 package is optional

3. Applications

- Smart home liquid level measurement
- Industrial tank level measurement
- Engine oil level measurement
- Food moisture content analysis
- Soil moisture content analysis
- Proximity sensing
- Touch Perception

Product Information

Part Number	Package	Dimensions
MC12G	QFN16	3.0*3.0*0.75mm
MC12T	SOP8	4.9*3.9*1.6mm

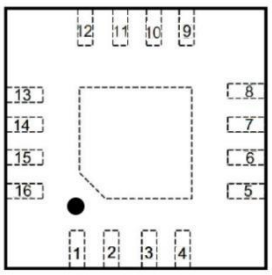
Table of Contents

1. Overview 1
2. Features 1
3. Applications 1
4. Package Pin Description 4
4.1. MC12G package Pinout Diagram (QFN16) 4
4.2. MC12T package Pinout Diagram (SOP8) 5
5. Electrical Specifications 5
5.1. Maximum Absolute Ratings 5
5.2. ESD Rating 5
5.3. Electrical Characteristics 6
5.4. I2C Interface Timing 7
6. Detailed description 8
6.1. Overview 8
6.2. System Block Diagram 8
6.3. Functional Description 9
6.3.1. Clock System 9
6.3.2. Channel Conversion 10
6.3.2.1 Conversion Mode 10
6.3.2.2 Data Format and Reading 11
6.3.2.3 Conversion Time 12
6.3.3. Capacitance Calculation 14
6.3.4. Drive Current 15
6.3.5. Alarm Function and INTB 15
6.3.6. Reference Voltage 17
6.3.7. Status Register 17
6.3.8. Temperature Measurement 17
6.4. Function Mode 18
6.4.1. Power On 18
6.4.2. Conversion Mode 18
6.4.3. Sleep Mode 18
6.4.4. Shutdown Mode 18
6.4.5. Software Reset 18
6.5. I2C programming 18
6.5.1. I2C Address Selection 19

6.5.2. I2C Interface Data Format 19
6.6. Register Description 21
6.6.1. Register List 21
6.6.2. DATA_CH0_MSB、DATA_CH0_LSB 22
6.6.3. DATA_CH1_MSB、DATA_CH1_LSB 22
6.6.4. RCNT_CH0_MSB、RCNT_CH0_LSB 22
6.6.5. RCNT_CH1_MSB、RCNT_CH1_LSB 23
6.6.6. SCNT_CH0 23
6.6.7. SCNT_CH1 23
6.6.8. FIN_DIV_CH0 24
6.6.9. FREF_DIV_CH0 24
6.6.10. FIN_DIV_CH1 24
6.6.11. FREF_DIV_CH1 25
6.6.12. STATUS 25
6.6.13. TH_MSB、TH_LSB 26
6.6.14. TL_MSB、TL_LSB 26
6.6.15. CFG 26
6.6.16. CH_EN 27
6.6.17. RESET 27
6.6.18. DRIVE_I_CH0 28
6.6.19. DRIVE_I_CH1 28
6.6.20. VC_SEL 29
6.6.21. GLITCH_FILTER_EN 29
6.6.22. DEVICE_ID_MSB、DEVICE_ID_LSB 30
7. Application and Implementation 30
7.1 Typical Application Circuits 30
7.2 Typical Application Examples 32
7.3 Inductance self-resonant Frequency 33
8. Package 34
8.1 MC12G QFN16 3.0*3.0*0.75mm Product Dimensions and Specifications Diagram 34
8.2 MC12T SOP8 4.9*3.9*1.6mm Product Dimensions and Specifications Diagram 35
9. Ordering Information 36

4. Package Pin Description

4.1. MC12G package Pinout Diagram (QFN16)

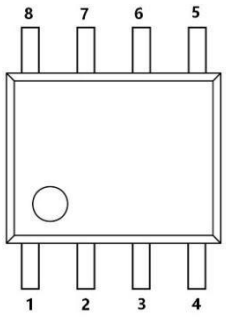


Front View

Pin Number	Pin Name	Type	Description
1	SCL	I	I2C clock line
2	SDA	I/O	I2C data line
3	CLKIN	I	External Counting Clock (GND is required when selecting internal clock counting)
4	ADDR	I	I2C address line
5	INTB	O	Interrupt signal output, low level valid
6	SD	I	Shut down mode enable signal
7	VDD	P	Power supply
8	GND	G	Ground
9	C0A	A	Channel 0 capacitor input port
10	C0B	A	Channel 0 capacitor input port
11	C1A	A	Channel 1 capacitor input port
12	C1B	A	Channel 1 capacitor input port
13	VC	A	Internal reference voltage
14	VT	A	Negative temperature coefficient voltage
15	NC	-	Floating
16	NC	-	Floating

Note 1: I denotes input, O denotes output, P denotes power supply, G denotes ground, and A denotes analog signal.
Note 2: When designing the circuit, it is recommended that the thermal pad is floating or grounded.

4.2. MC12T package Pinout Diagram (SOP8)



Front View

Pin Number	Pin Name	Type	Description
1	VT	A	Negative temperature coefficient voltage
2	SCL	I	I2C clock line
3	SDA	I/O	I2C data line
4	VDD	P	Power supply
5	GND	G	Ground
6	C0	A	Channel 0 capacitor input port
7	C1	A	Channel 1 capacitor input port
8	VC	A	Internal reference voltage

Note: I denotes input, O denotes output, P denotes power supply, G denotes ground, and A denotes analog signal.

5. Electrical Specifications

5.1. Maximum Absolute Ratings

		Minimum	Maximum	Unit
VDD	Power supply voltage range	-0.3	6.0	V
Vi	Pin voltage	-0.3	VDD	V
T_J	junction temperature	-55	125	℃
Tstg	Storage temperature	-55	125	℃

Note: The above are the limit parameters. This specification does not apply to the functional operation of the device in the environment beyond this limit condition. Long-term exposure to this limit environment will affect the reliability of the device.

5.2. ESD Rating

		Value	Unit
VESTD Static Discharge	Human-body model（HBM）	±8000	V
	Charged-device model（CDM）	±750	V

5.3. Electrical Characteristics

Unless otherwise specified, the table data assumes T=25℃ and VDD=5V.

Parameter		Test Condition	Minimum	Typical Value	Maximum	Unit
Power						
V_{DD}	Supply voltage	T = -55℃ to 125℃	2.0		5.5	V
I_{DD}	Measurement peak current (1)		1.3	3.7	8.3	mA
I_{DDCST}	Constant standby current (2)			75		uA
I_{DDSL}	Sleep mode murrent (3)			0.05		uA
I_{SD}	Shut-down mode current (3)			0.04		uA
I_{DDAVG}	Average current	1Hz, IDRIVE=3mA, TCV=2ms		7.5		uA
Sensor						
$C_{SENSORMAX}$	Maximum capacitance under test	L=150nH, f_{SENSOR}=30MHz		150		pF
$C_{C0A/C1A}$	Pin parasitic capacitance			2		pF
ENOB	Effective resolution				15	Bit
f_{cs}	Channel sampling rate		0.01		1	kSPS
f_{SENSOR}	Sensor frequency range	T = -55℃ to 125℃	10		100	MHz
$I_{SENSORMAX}$	Sensor driving current	One channel	0.5	3.0	8.0	mA
Internal clock						
f_{INTCLK}	Internal clock frequency		2.3	2.4	2.5	MHz
$T_{CF\_INT\_U}$	Internal clock temperature drift coefficient	T = 20℃ to 125℃		-700		ppm/℃
		T = -55℃ to 20℃		800		ppm/℃
External clock						
f_{CLKIN}	External clock frequency	T = -55℃ to 125℃	0.1		50	MHz
CLKIN_DUTY	External clock duty cycle		40%		60%	
V_{CLKIN_HI}	External clock input voltage high		0.7*VDD			V
V_{CLKIN_LO}	External clock input				0.3*VDD	V

	voltage low					

Note 1: Measurement peak current, representing the current during conversion when configured in single conversion and continuous conversion modes.

Note 2: The standby current for continuous conversion refers to the current during non-conversion periods when configured in continuous conversion mode.

Note 3: Current flowing into SDA and SCL pins during I2C read/write operations is excluded.

5.4. I2C Interface Timing

Table 5.4 I2C Bus Timing Characteristics (1)

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min Value	Max Value	Min Value	Max Value	
SCL frequency	f_{SCL}	0	400	0	1000	kHz
SCL low level time	t_{LOW}	1300	—	620	—	ns
SCL high level time	t_{HIGH}	600	—	220	—	ns
The duration of SCL's high level following SDA's low pull during startup (restart)	$t_{HD;STA}$	400	—	260	—	ns
The time span from SCL's downward pull to SDA data change	$t_{HD;DAT}$	0	0.9	0	—	μs
The time span between the stabilization of SDA data and the subsequent SCL surge	$t_{SU;DAT}$	100	—	150	—	ns
The SDA's low-pull-out duration before the SCL's high-level hold time during restart	$t_{SU;STA}$	400	—	260	—	ns
The time interval between SCL rising to SDA rising during a stop	$t_{SU;STO}$	400	—	260	—	ns
The interval between start and stop	t_{BUF}	1300	—	500	—	ns
Time required for the rising edge of SCL/SDA	t_{RC}	20+ 0.1Cb(2)	1000	20+ 0.1Cb(2)	120	ns
Time required for the SCL/SDA falling edge	t_{FC}	20+ 0.1Cb(2)	300	20+ 0.1Cb(2)	120	ns

Note 1: All values are referenced to VIHmin and VILmax.

Note 2: Cb denotes the total capacitance of the I2C bus.

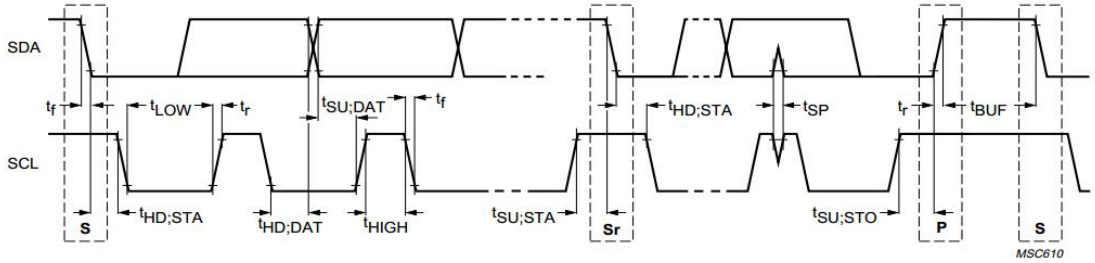


Figure 5.4 I2C timing parameters

6. Detailed description

6.1. Overview

The MC12G and MC12T are high-precision, dual-channel capacitive sensors designed for diverse capacitive sensing applications. Unlike conventional switch-capacitor architectures, these sensors employ LC-resonant method for capacitance measurement. The narrowband characteristics of LC oscillators enable them to achieve lower noise level and demonstrate enhanced immunity to external interference.

When the capacitance of the LC resonant circuit changes, the resonant frequency of the circuit also changes accordingly. Based on this principle, MC12G and MC12T measure the oscillation frequency and output a data proportional to the frequency. This data can be used to calculate the capacitance value.

6.2. System Block Diagram

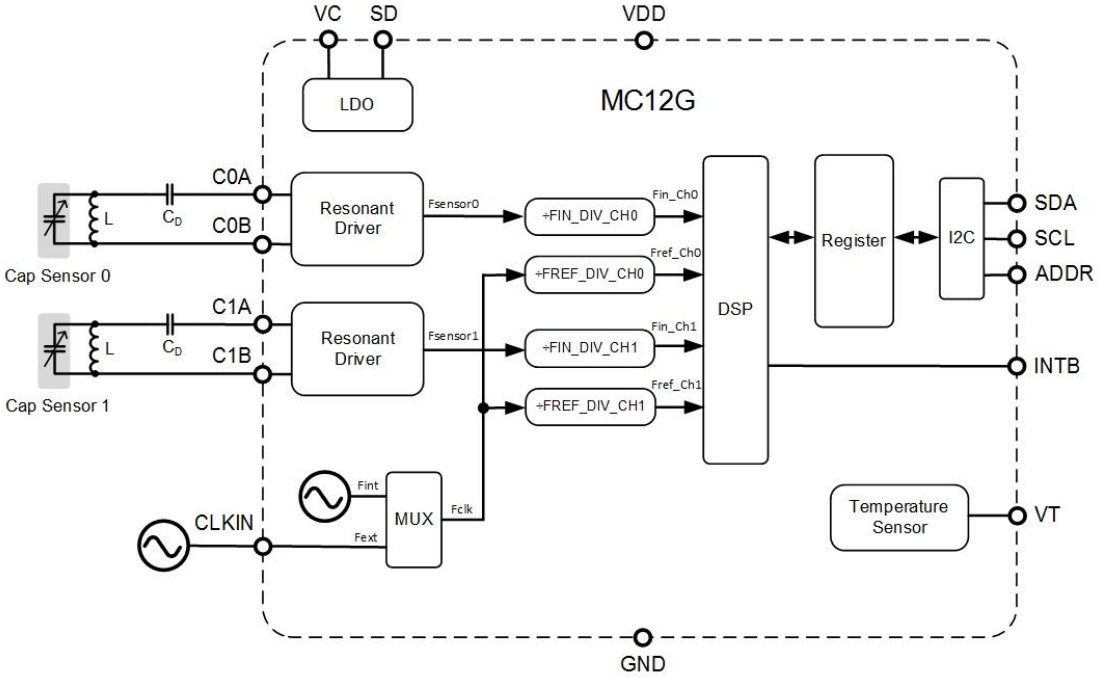


Figure 6.2-1 Block Diagram of the MC12G System

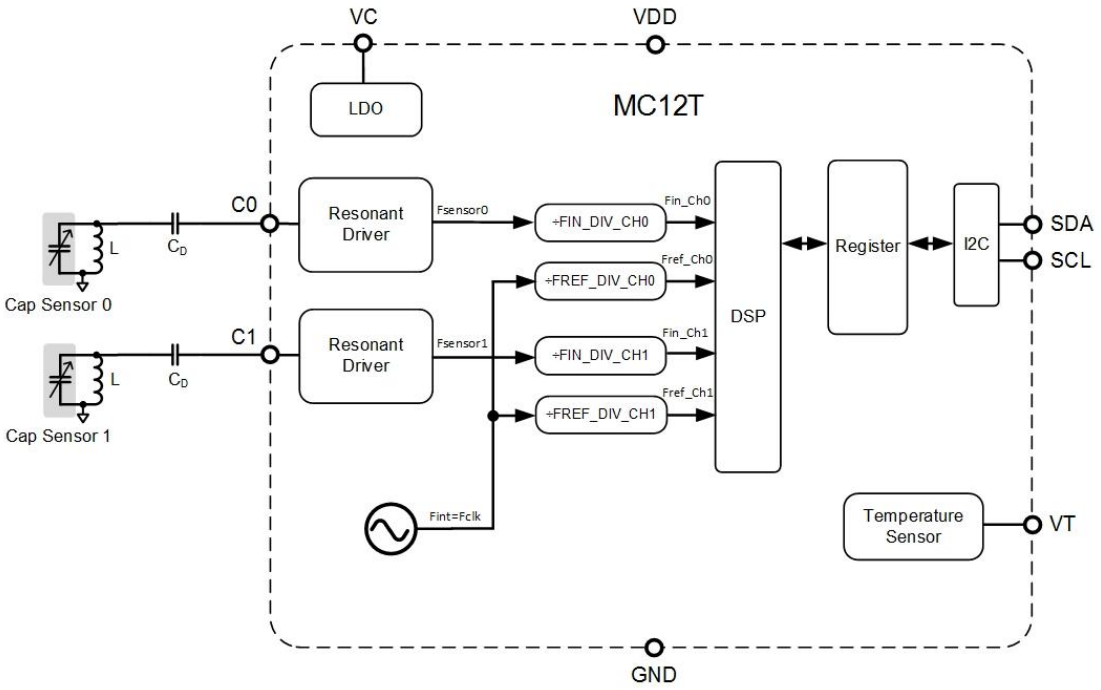


Figure 6.2-2 Block Diagram of the MC12T System

The system block diagrams for MC12G and MC12T include functional modules such as power management (LDO), resonant driver, divider, internal clock (Fint), digital frequency calculation (DSP), registers, temperature sensor, and I2C interface. The resonant driver and external LC of MC12G and MC12T form an active oscillator, which sends the output signal to the digital logic circuit to measure and digitize the sensor's signal frequency (f_{SENSOR}). For MC12G, the C0B/C1B pins are internally connected to GND through the sensor. The digital logic uses the reference frequency (f_{CLK}) to measure the sensor's signal frequency f_{SENSOR}, where f_{CLK} comes from either the sensor clock or external clock. The I2C interface enables communication between the sensor and MCU. By measuring the voltage at the VT pin on the MCU side, ambient temperature can be indirectly measured for temperature compensation. For MC12G, controlling the SD pin allows the sensor to be powered down to reduce system power consumption. Meanwhile, the INTB pin can output alarm status bits or conversion completion flags according to configuration.

6.3. Functional Description

6.3.1. Clock System

According to the block diagrams of the MC12G and MC12T systems, f_{CLK}, f_{IN}, and f_{REF} are three critical clock signals. Based on register configurations, F_{CLK} can be set to either an internal or external clock (MC12T exclusively supports internal clock). The reference clock f_{REF} is derived by dividing F_{CLK}. For high-precision applications, external clocks with high accuracy and stability are recommended, while internal clocks are more suitable for low-cost applications requiring moderate precision. When using external clocks, their voltage must range from 0V to VDD. The measured signal clock F_{IN} is obtained by dividing the sensor's resonant signal f_{SENSOR}. To ensure accurate measurement results, the clock frequencies of f_{REF} and f_{IN} must meet the following conditions:

$$f_{INx} < \frac{f_{REFx}}{2.5}$$

In practical applications, the closer the f_{REFx}/f_{INx} ratio is to 2.5, the higher the measured effective resolution, with a maximum effective bit depth of 15 bits. The table below defines the clock configuration registers.

Table 6.3.1 Clock Configuration Register Definitions

Channel	Clock	Register and Address	Position	Description
0,1	F_{CLK}	CFG, 0x1F	REF_CLK_SEL	b0: Select internal clock b1: Select external clock
0	F_{REF0}	FREF_DIV_CH0, 0x12	CH0_FREF_DIV[7:0]	b00000000-b11111111: The corresponding value ranges from 0 to 255 $f_{REF0} = f_{CLK} / (CH0\_FREF\_DIV+1)$
1	F_{REF1}	FREF_DIV_CH1, 0x14	CH1_FREF_DIV[7:0]	b00000000-b11111111: The corresponding value ranges from 0 to 255 $f_{REF1} = f_{CLK} / (CH1\_FREF\_DIV+1)$
0	F_{IN0}	FIN_DIV_CH0, 0x11	CH0_FIN_DIV[3:0]	b0000-b0111: Corresponding to values from 0 to 7 b1000-b1111: Corresponding to value 8 $f_{IN0} = f_{SENSOR0} / 2^{CH0\_FIN\_DIV}$
1	F_{IN1}	FIN_DIV_CH1, 0x13	CH1_FIN_DIV[3:0]	b0000-b0111: Corresponding to values from 0 to 7 b1000-b1111: Corresponding to value 8 $f_{IN1} = f_{SENSOR1} / 2^{CH1\_FIN\_DIV}$

6.3.2. Channel Conversion

6.3.2.1 Conversion Mode

By setting the channel enable bits, you can choose to enable single-channel or multi-channel conversion. When selecting multi-channel conversion, channel 0 is activated first, followed by channel 1, with a switching time between the two channels ≤10us. The table below defines the configuration registers for channels.

Table 6.3.2-1 Channel Configuration Register Definitions

Channel	Register and Address	Position	Description
0	CH_EN, 0x20	CH0_EN	b0: Close channel 0 b1: Enable channel 0
1	CH_EN, 0x20	CH1_EN	b0: Close channel 1 b1: Enable channel 1

The CFG register enables configuration of the sensor's operating modes, including single conversion, continuous conversion, and stop conversion. The table below defines the registers for these modes.

Table 6.3.2-2 Work Mode Configuration Register Definitions

pattern	register and address	position	explain
Conversion mode	CFG, 0x1F	OS,SD	b00: Continuous conversion mode, with the time interval determined by the value of CR[2:0]. To change the continuous conversion mode, you must stop the conversion first. b01: Stop conversion. b10: Same as b00. b11: Single conversion mode. After setting the flag, the sensor performs one-time conversion and automatically stops. Upon completion, OS and SD automatically switch to b01.
Samples per second (MPS)	CFG, 0x1F	CR[2:0]	b000: Convert every 60 seconds b001: Convert every 30 seconds b010: Convert every 10 seconds b011: Convert every 5s b100: Convert every 2s b101: Convert every 1 second b110:0.5s Convert once b111:0.25s Change once

Note that to ensure the accuracy of converted data, the following two points must be followed when modifying the register configuration:

i. To switch from continuous to single conversion mode, you must first send a stop conversion command, followed by a single conversion command.

ii. Do not modify any register configurations related to the conversion process during measurement. If configuration parameters need to be modified, stop the conversion first, ensure the conversion stops, then modify the parameters and restart the conversion.

6.3.2.2 Data Format and Reading

The sensor measures the ratio of the frequency of each channel signal divided by the frequency of the reference clock divided by the divider, expressed in a 16-bit data format:

$$DATA_X = \frac{f_{INx}}{f_{REFx}} * 2^{16} = \frac{f_{SENSORx}}{f_{CLK}} * \frac{CHx\_FREF\_DIV + 1}{2^{CHx\_FIN\_DIV}} * 2^{16}$$

The converted data results are stored in the following corresponding registers:

Table 6.3.2-3 Convert Data Register Definitions

Channel	Register and Address	Position	Description
0	DATA_CH0_MSB, 0x00	DATA0[15:8]	Channel 0 converts the high 8-bit data
	DATA_CH0_LSB, 0x01	DATA0[7:0]	Channel 0 converts the lower 8 bits of data
1	DATA_CH1_MSB, 0x02	DATA1[15:8]	Channel 1 converts data high 8 bits
	DATA_CH1_LSB, 0x03	DATA1[7:0]	Channel 1 converts the lower 8 bits of data

Note that to ensure accurate data conversion, the I2C read operation on DATAx must be performed during the sensor's non-conversion period. The specific method is as follows:

i. Single-transaction mode: I2C must read DATAx after the conversion completes.

ii. For continuous conversion mode, first halt the conversion, then perform an I2C read on DATAx, and restart the continuous conversion.

6.3.2.3 Conversion Time

The figure below shows the timing diagram for single-channel and dual-channel selection in single-conversion mode. T_{CV} is the total single-channel single-conversion time, T_{SC} is the channel switching time (<10us), and T_{SVT} is the VT voltage establishment time.

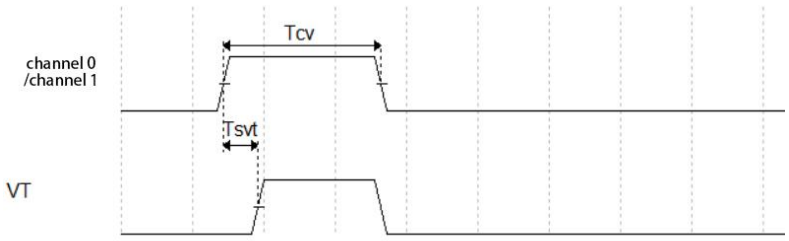


Figure 6.3.2-1 Single-channel single-convert mode timing diagram

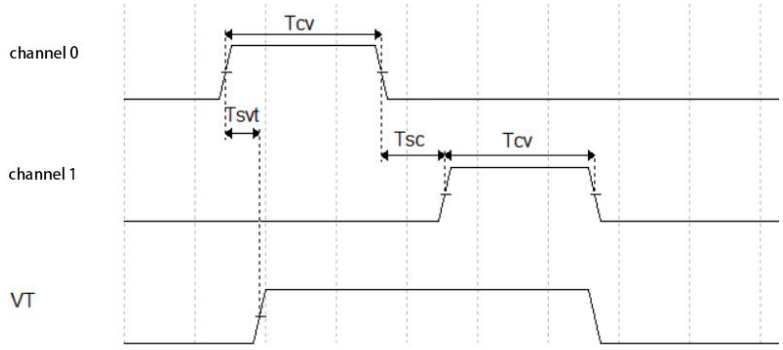


Figure 6.3.2-2 Timing diagram of dual-channel single conversion mode

The figure below shows the timing diagrams for single-channel and dual-channel configurations in continuous conversion mode. T_{PER} denotes the measurement period of continuous conversion

mode, T_{CV} represents the total single-channel conversion time, T_{SC} indicates the channel switching time (<10us), and T_{SVT} stands for the voltage establishment time of VT.

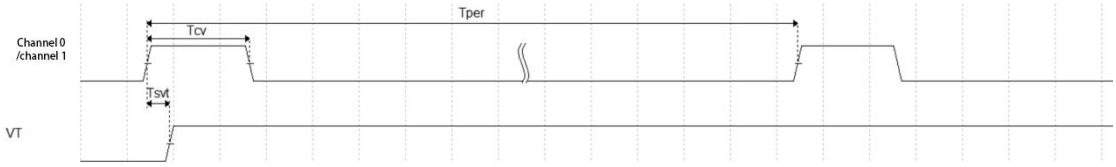


Figure 6.3.2-3 Single-channel continuous conversion mode timing diagram

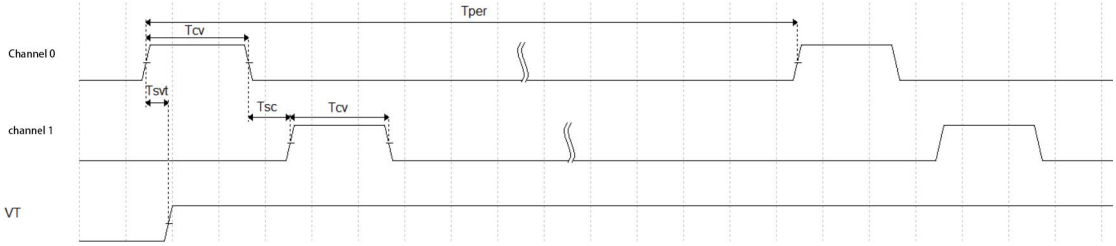


Figure 6.3.2-4 Dual-channel continuous conversion mode timing diagram

To ensure the continuous conversion mode operates properly, T_{PER} and T_{CV} must satisfy the following constraints:

$$i.\ Single\ channel\ measurement, T_{PER} > T_{CV}$$
$$ii.\ Dual\ ch\ annel\ measurement, T_{PER} > 2 * T_{CV} + 10us$$

T_{CV} comprises four components: T_{START} (startup time), T_{SET} (setup time), T_{CNT} (counting time), and T_{DELAY} (delay time).

$$T_{CV} = T_{START} + T_{SET} + T_{CNT} + T_{DELAY}$$

The channel's start time T_{START} indicates the stabilization period of the internal reference voltage, fixed at 200us.

The channel setup time T_{SET} indicates the initial stabilization period for the oscillation signal, defined by the following registers:

Table 6.3.2-4 Establish Time Configuration Register Definition

Channel	Register and Address	Position	Description
0	SCNT_CH0, 0x0E	SCNT0[7:0]	Channel 0 settling time
1	SCNT_CH1, 0x0F	SCNT1[7:0]	Channel 1 settling time

Note: Unless otherwise specified, all variables in the following formulas use international units.

The T_{SET} calculation formula is:

$$T_{SET} = SCNTx * 16 / f_{REFx}$$

To ensure sufficient channel signal setup time, configure T_{SET} to ≥100us. Specifically, when using the internal clock as F_{CLK}, SCNT_CHx=0x0F corresponds to T_{SET}=100us, while SCNT_CHx=0xFF corresponds to T_{SET}=1.7ms.

The channel count time (T_{CNT}) indicates the duration during which F_{REFx} counts pulses from F_{Inx}, as defined by the following registers:

Table 6.3.2-5 Count Time Configuration Register Definitions

Channel	Register and Address	Position	Description
0	RCNT_CH0_MSB, 0x08	RCNT0[15:8]	Channel 0 conversion time, high 8 bits
	RCNT_CH0_LSB, 0x09	RCNT0[7:0]	Channel 0 conversion time, low 8 bits
1	RCNT_CH1_MSB, 0x0A	RCNT1[15:8]	Channel 1 conversion time, high 8 bits
	RCNT_CH1_LSB, 0x0B	RCNT1[7:0]	Channel 1 conversion time, low 8 bits

The TNCNT calculation formula is:

$$T_{CNT} = RCNTx \,/\, f_{REFx}$$

The configuration of RCNTx determines the sensor's effective resolution (ENOB). When ENOB> n, it requires RCNTx> 2^n+1. For example, achieving 14-bit resolution requires RCNTx> 2^{15} = 32768, corresponding to RCNTx[15:0]> 0x8000. In this case, if the internal clock is used as Fclk and CHx_FREF_DIV=0, the counting time:

$$T_{CNT} = 32768/2400 = 13.65\text{ms}$$

RCNTx can be configured up to 65535, which corresponds to a maximum 15-bit effective resolution and the longest count time.

The channel delay time TDELAY is:

$$T_{DELAY} = 4 \,/\, f_{REFx}$$

Therefore, the calculation formula for conversion time (TCV) is:

$$T_{CV} = 200us + (SCNTx * 16 + RCNTx + 4) \,/\, f_{REFx}$$

To ensure accurate VT voltage detection, T_{CV} and T_{SVT} must satisfy the following constraints:

$$T_{CV} > T_{SVT} + T_{ADC}$$

The capacitance value of T_{SVT} and VT pins relative to ground is determined by the capacitance. For a 1nF capacitor, T_{SVT} equals 1ms. The external ADC samples the VT pin after the VT voltage stabilizes, with T_{ADC} representing the measurement time for the external ADC.

6.3.3. Capacitance Calculation

The formula for calculating LC resonant frequency is (unless otherwise specified, all variables in the formula use international units):

$$f_{SENSOR} = \frac{1}{2\pi * \sqrt{L * (C_{SENSOR} + C_F)}}$$

Therefore, the measured capacitance C_{SENSOR} can be calculated as follows:

$$C_{SENSOR} = \frac{1}{L * (2\pi \cdot f_{SENSOR})^2} - C_F$$

C_F denotes the total capacitance to ground in parallel with C_{SENSOR}, which can be expressed as:

$$C_F = \frac{C_D * C_P}{C_D + C_P}$$

In the above equation, each capacitor represents:

The C_D acts as an external DC-blocking capacitor, positioned between the resonant point and the C0A/C1A pins (see Figures 6.2-1 and 6.2-2).

The capacitance (C_P) is the sum of the sensor's internal C0A/C1A pin-to-ground capacitance and parasitic capacitance, typically 66pF.

Using the data DATAx, the value of $f_{SENSORx}$ can be calculated as follows:

$$f_{SENSORx} = f_{CLK} * \frac{2^{CHx\_FIN\_DIV}}{CHx\_FREF\_DIV + 1} * \frac{DATA_X}{2^{16}}$$

6.3.4. Drive Current

The drive current I_{DRIVE} of the two-channel oscillator can be configured to different values, defined by the following registers.

Table 6.3.4 Drive Current Configuration Register Definitions

Channel	Register and Address	Position	Description
0	DRIVE_I_CH0, 0x23	I0[3:0]	Set the single-channel drive current value b0000-b1111:0.5mA to 8mA, LSB=0.5mA
1	DRIVE_I_CH1, 0x24	I1[3:0]	

To ensure successful oscillator startup, the drive current I_{DRIVE} must exceed a specific threshold. This threshold depends on the capacitor network formed by C_{SENSOR}, C_D, and C_P, as well as the Q factor of inductor L. Generally, higher drive currents enhance channel oscillation capability and amplify oscillation amplitude. For larger C_{SENSOR} capacitance and inductors with low Q factors, increasing the drive current is essential to achieve reliable channel oscillation.

6.3.5. Alarm Function and INTB

The MC12G and MC12T models feature alarm functionality, with alarm thresholds (TH and TL) defined by the following registers. Both TH and TL are 16-bit registers, matching the bit width of DATA_CHx.

Table 6.3.5-1 Alarm Threshold Configuration Register Definitions

Threshold	Register and Address	Position	Description
Alarm triggered	TH_MSB, 0x19	TH[15:8]	When DATA_CHx exceeds the threshold, the ALERT_CHx bit in the STATUS register is set to 1.
	TH_LSB, 0x1A	TH[7:0]	
Alarm triggered remove	TL_MSB, 0x1B	TL[15:8]	When DATA_CHx<TL, the ALERT_CHx bit in the STATUS register is set to 0
	TL_LSB, 0x1C	TL[7:0]	

The alarm status is triggered when the conversion is complete and the following conditions are met:

$$DATA\_CHx > TH$$

When the alarm status is triggered, the ALERT_CHx in the status register is set to 1, and the INTB pin output level drops from high to low (applicable only to MC12G). To ensure the alarm function is enabled, the TH and TL threshold parameters must meet the following conditions:

$$TH \geq TL$$

When the alarm status is triggered, there are four ways to clear the alarm status:

i. Read channel conversion data $DATA_CHx$via I2C. This method is limited to single conversion mode and stop mode.

ii. Perform a channel conversion and $DATA_CHx < TL$satisfy the condition.

iii. Enable the software reset function.

iv. Pull up the SD pin.

For the MC12G, the INTB pin can output the alarm status bit from channel 0 or channel 1, with low level being valid. After the alarm status is cleared, the INTB pin returns to high level. Additionally, the INTB pin can be configured to output the conversion complete flag for channel 0 or channel 1. The INTB functionality is defined by the following registers.

Table 6.3.5-2 INTB Function Register Definitions

Channel	Register and Address	Position	Description
0,1	CFG, 0x1F	INTB_EN	b0: INTB pin output is disabled. b1: INTB pin output enable.
0,1	CFG, 0x1F	INTB_MODE	b0: INTB pin output alarm status bit, low level valid. b1: INTB pin output conversion completion flag, active low.
0,1	CH_EN, 0x20	INTB_CH	b0: The alarm status or conversion completion flag for INTB pin output channel 0. b1: The alarm status or completion flag for the INTB pin output channel 1.

6.3.6. Reference Voltage

Both MC12G and MC12T sensors support multiple VDD voltage levels. By adjusting the VC_SEL register, the internal reference voltage (VC pin voltage) is modified to optimize sensor performance under different VDD conditions.

Table 6.3.6 VC_SEL Register Definition

Channel	Register and Address	Position	Description
0,1	VC_SEL, 0x23	VC	b00: Reference voltage is 2.5V b01: Reference voltage is 3.0V b10: Reference voltage is 1.8V b11: Reference voltage is 2.0V

For practical use, configure according to the following two points:
i. When 2.5V<VDD<5.5V is set to 0, the reference voltage is configured to 2.5V (default).
ii. When 2V<VDD<2.5V, the reference voltage is set to 2.0V.

6.3.7. Status Register

The status register indicates whether the measurement data of MC12G and MC12T has overflowed, whether the conversion is complete, and the alarm status.

Table 6.3.7 Status Register Definitions

Channel	Register and Address	Position	Description
0	STATUS, 0x17	OF_CH0	b0: Channel 0 data not overflowed b1: Channel 0 data overflow
1	STATUS, 0x17	OF_CH1	b0: Channel 1 data not overflowing b1: Channel 1 data overflow
0	STATUS, 0x17	DRDY_CH0	b0: Channel 0 conversion is not complete b1: Channel 0 conversion completed
1	STATUS, 0x17	DRDY_CH1	b0: Channel 1 conversion not completed b1: Channel 1 conversion completed
0	STATUS, 0x17	ALERT_CH0	b0: Channel 0 did not trigger alarm b1: Channel 0 triggers alarm
1	STATUS, 0x17	ALERT_CH1	b0: Channel 1 did not trigger alarm b1: Channel 1 triggers alarm

6.3.8. Temperature Measurement

The MC12G and MC12T devices provide a voltage VT with a negative temperature coefficient, which is output to the VT pin for approximate temperature estimation. The startup sequence for the VT pin voltage is detailed in Section 6.3.2.3. To measure the VT voltage, an external ADC is required for sampling, though the standard 10-bit precision ADC integrated in the MCU is sufficient. The temperature value T is calculated by the MCU using the following formula:

$$T = K \cdot V_{\mathrm{T}} + T_C$$

Where VT is the voltage measured by the ADC, in volts (V); K is the temperature coefficient, with a default value of-507.8℃/V; TC is the temperature correction value, with a default of 339.8℃. Users can also calibrate K and TC.

6.4. Function Mode

6.4.1. Power On

After power-on, MC12G and MC12T automatically enter continuous conversion mode. Users can send a stop conversion command via I2C to put the sensor into sleep mode, then perform operations such as parameter modification, single conversion, or continuous conversion.

6.4.2. Conversion Mode

The MC12G and MC12T devices feature two conversion modes: single-cycle and continuous, which are configured via the CFG register as detailed in Section 6.3.2.

6.4.3. Sleep Mode

After completing each I2C command operation, the MC12G and MC12T automatically enter sleep mode (low-power mode). When the host sends a valid I2C command, the MC12G and MC12T will automatically wake up and execute the corresponding operation. Note that in continuous conversion mode, the MC12G and MC12T will not enter sleep mode after each conversion.

6.4.4. Shutdown Mode

The external SD pin on the MC12G is used for hardware shutdown. When the SD pin is pulled high, the sensor's functions are completely disabled, and I2C access is blocked. The sensor recovers within 20us when the SD pin transitions from high to low.

6.4.5. Software Reset

The MC12G and MC12T sensors feature a software reset (Softreset) function. By writing 0x7A to the reset register, the software reset activates, restoring the sensor to its power-on state with all registers returning to default values, achieving a sensor recovery time of <20us.

Table 6.4.5 Reset register definition

Channel	Register and Address	Position	Description
0,1	RESET, 0x22	RESET[7:0]	b01111010： Initiate software reset. The sensor returns to its power-on initial state, and all registers revert to default values.

6.5. I2C programming

The MCU accesses the control and data registers of MC12G and MC12T via the I2C interface. The SDA and SCL pins incorporate spike suppression circuits to reduce bus noise. Both MC12G and MC12T support 400KHz I2C communication rates. The I2C data SDA and clock SCL are

connected to the corresponding ports of the host processor, with each linked to VDD through pull-up resistors (R_P). The host software manages read/write operations for each node sensor. In practical applications, the device address is configured using the ADDR pin value.

6.5.1. I2C Address Selection

The MC12G supports multiple I2C addresses through different ADDR pin connections, with the specific mapping as follows:

Table 6.5-1 MC12G I2C Address Truth Table

ADDR Connection	I2C Address
connect to GND	0x68
connect to VDD	0x69
connect to SDA	0x6A
connect to SCL	0x6B

The I2C address of the MC12T is fixed at 0x69.

6.5.2. I2C Interface Data Format

The typical I2C bus operation is defined as follows:

Bus idle: Both SDA and SCL maintain high levels.

Start data transfer: When SCL is high, the change of SDA status (from high to low) indicates the start condition. Each data transfer starts with a start condition.

Stop data transmission: When SCL is high, the change of SDA status (from low to high) indicates the stop state. Each data transmission is terminated by repeating start or stop conditions.

Data transfer: The number of data bytes transmitted between start and stop conditions is not limited and is determined by the master device. The receiver confirms the data transfer.

Response: Each receiving slave device must generate a response signal when addressed. The slave must stabilize the SDA line at a low level during the high phase of the acknowledgment clock pulse. The master device terminates data transfer by not responding after receiving the last byte from the slave.

In I2C bus communication, the host first transmits the slave address and write flag (Slave Address + W), followed immediately by the register address (Register Address). For read sequences, the host then sends the slave address and read flag (Slave Address + R), after which the slave transmits data (Data from Register) to the host. When the host responds with ACK, the next byte of data can be read consecutively; if the host replies with NACK, the slave stops sending data. For write sequences, the host directly transmits data (Data to Register) to the slave. Note that the slave address width is 7 bits, with the write flag W=0 and read flag R=1. The detailed read/write sequence diagram is shown below:

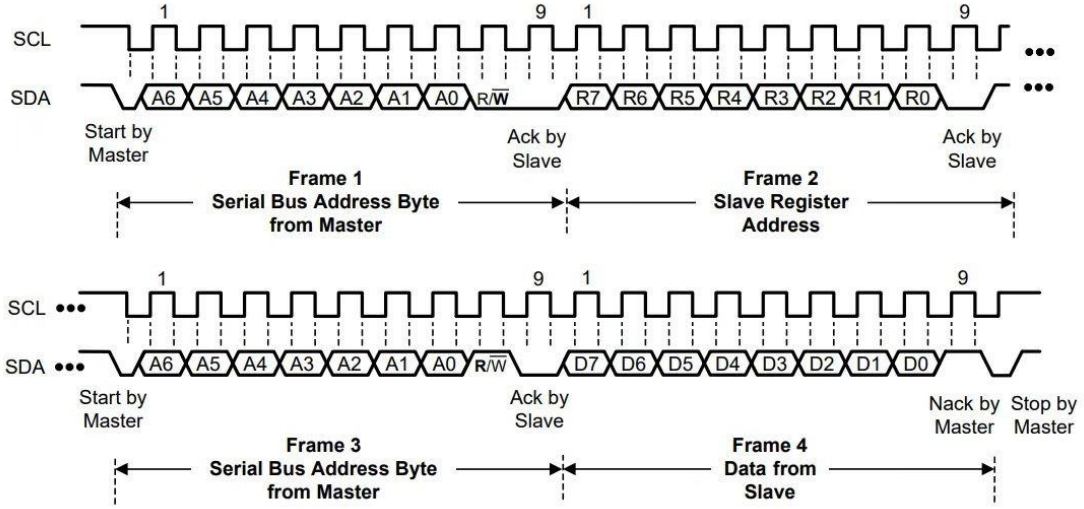


Figure 6.5.2-1 I2C Single-byte Read Timing

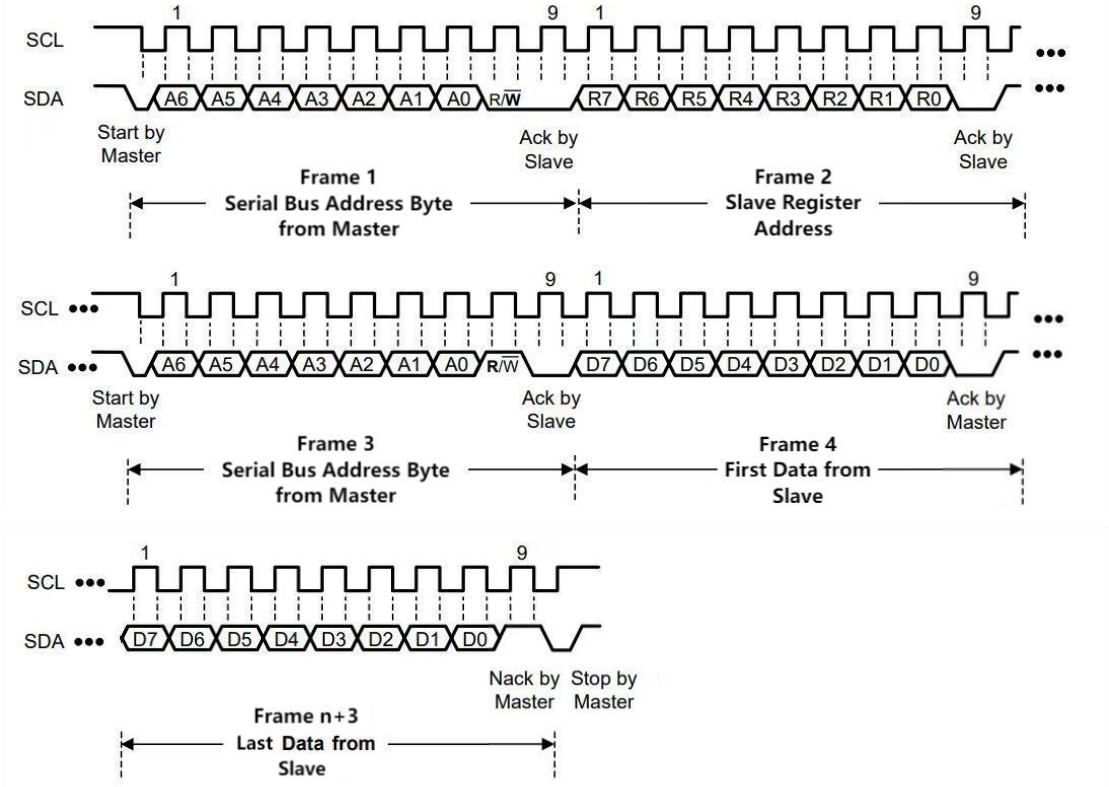


Figure 6.5.2-2 I2C Continuous Read Timing

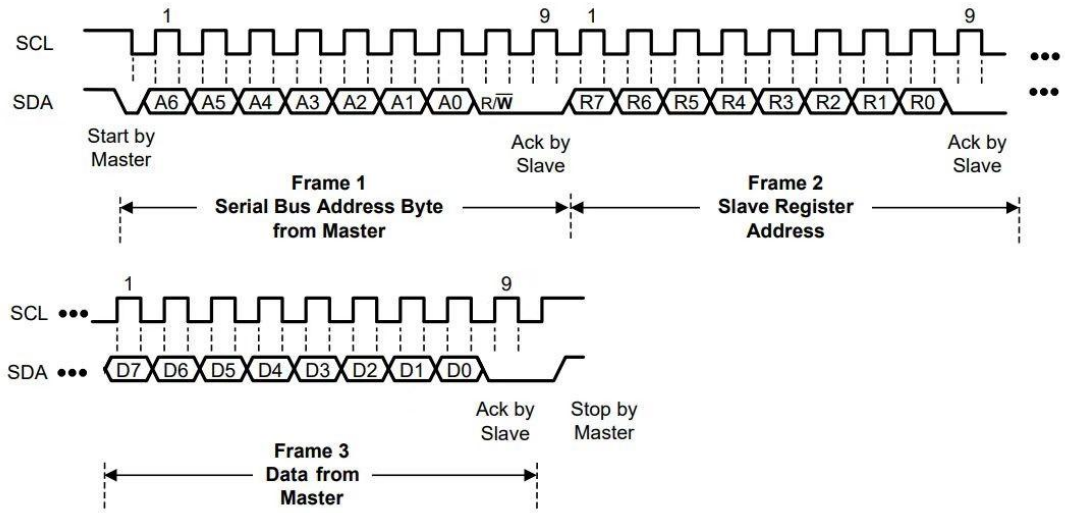


Figure 6.5.2-3 I2C Write Timing

6.6. Register Description

6.6.1. Register List

The MC12G and MC12T registers are categorized into three types: read-write, read-only, and write-only. The default values represent the sensor's initial state when powered on. Below is the complete register list.

Table 6.6.1 Register List

Address	Name	Default Value	Description
0x00	DATA_CH0_MSB	0x00	Channel 0 is read-only
0x01	DATA_CH0_LSB	0x00	
0x02	DATA_CH1_MSB	0x00	Channel 1 converts data for read-only access
0x03	DATA_CH1_LSB	0x00	
0x08	RCNT_CH0_MSB	0x40	Channel 0 counting time
0x09	RCNT_CH0_LSB	0x00	
0x0A	RCNT_CH1_MSB	0x40	Channel 1 counting time
0x0B	RCNT_CH1_LSB	0x00	
0x0E	SCNT_CH0	0x20	Channel 0 creation time
0x0F	SCNT_CH1	0x20	Channel 1 establishment time
0x11	FIN_DIV_CH0	0x70	Channel 0 Oscillator Signal Frequency Division
0x12	FREF_DIV_CH0	0x00	Channel 0 reference clock divider
0x13	FIN_DIV_CH1	0x70	Channel 1 Oscillator Signal Frequency Division
0x14	FREF_DIV_CH1	0x00	Channel 1 reference clock divider
0x17	STATUS	0x00	Status bit, read-only
0x19	TH_MSB	0x20	Single-channel alarm trigger threshold
0x1A	TH_LSB	0x00	
0x1B	TL_MSB	0x10	Single-channel alarm removal threshold
0x1C	TL_LSB	0x00	

0x1F	CFG	0x54	Channel conversion and INTB function configuration
0x20	CH_EN	0xC0	Channel Selection Configuration
0x22	RESET	0x00	Reset function, write-only
0x23	DRIVE_I_CH0	0x50	Channel 0 drive current and low voltage configuration
0x24	DRIVE_I_CH1	0x50	Channel 1 drive current
0x30	VC_SEL	0x00	Voltage configuration
0x33	GLITCH_FILTER_EN	0x01	Anti-glitch filter
0x7E	SENSOR_ID_MSB	0x01	Sensor ID, read-only
0x7F	SENSOR_ID_LSB	0x20	

6.6.2. DATA_CH0_MSB、DATA_CH0_LSB

Address 0x0, DATA_CH0_MSB

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DATA0							

Address 0x1, DATA_CH0_LSB

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DATA0							

DATA_CH0_MSB & DATA_CH0_LSB Description

Position	Scope	Operate	Default Value	Description
7:0	DATA0[15:8]	read only	0000 0000	It is a 16-bit data structure representing the conversion data of channel 0.
7:0	DATA0[7:0]	read only	0000 0000	

6.6.3. DATA_CH1_MSB、DATA_CH1_LSB

Address 0x2, DATA_CH1_MSB

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DATA1							

Address 0x3, DATA_CH1_LSB

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DATA1							

DATA_CH1_MSB & DATA_CH1_LSB Description

Position	Scope	Operate	Default Value	Description
7:0	DATA1[15:8]	read only	0000 0000	It is a 16-bit data structure representing the conversion data from channel 1.
7:0	DATA1[7:0]	read only	0000 0000	

6.6.4. RCNT_CH0_MSB、RCNT_CH0_LSB

Address 0x8, RCNT_CH0_MSB

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RCNT0							

Address 0x9, RCNT_CH0_LSB

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RCNT0							

RCNT_CH0_MSB & RCNT_CH0_LSB Description

Position	Scope	Operate	Default Value	Description
7:0	RCNT0[15:8]	read-write	0100 0000	16-bit data configuration for setting the counting duration of channel 0.
7:0	RCNT0[7:0]	read-write	0000 0000	

6.6.5. RCNT_CH1_MSB、RCNT_CH1_LSB

Address 0xA, RCNT_CH1_MSB

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RCNT1							

Address 0xB, RCNT_CH1_LSB

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RCNT1							

RCNT_CH1_MSB & RCNT_CH1_LSB Description

Position	Scope	Operate	Default value	Description
7:0	RCNT1[15:8]	read-write	0100 0000	16-bit data configuration for setting the counting duration of channel 1.
7:0	RCNT1[7:0]	read-write	0000 0000	

6.6.6. SCNT_CH0

Address 0xE, SCNT_CH0

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCNT0							

SCNT_CH0 Description

Position	Scope	Operate	Default Value	Description
7:0	SCNT0[7:0]	read-write	0010 0000	Settling time of channel 0.

6.6.7. SCNT_CH1

Address 0xF, SCNT_CH1

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCNT1							

SCNT_CH1 Description

Position	Scope	Operate	Default Value	Description
7:0	SCNT1[7:0]	read-write	0010 0000	Settling time of channel 1.

6.6.8. FIN_DIV_CH0

Address 0x11, FIN_DIV_CH0

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH0_FIN_DIV				RSV			

FIN_DIV_CH0 Description

Position	Scope	Operate	Default Value	Description
7:4	CH0_FIN_DIV [3:0]	read-write	0111	Set the oscillation signal frequency division ratio for channel 0 000: Non-frequency division, corresponding to value 0 0001:2 frequency division, corresponding to value 1 0010:4 frequency division, corresponding to value 2 0011:8 frequency division, corresponding to value 3 0100:16 frequency division, corresponding to value 4 0101:32 frequency division, corresponding to value 5 0110:64 frequency division, corresponding to value 6 0111:128 frequency division, corresponding to value 7 1xxx: 256 frequency division, corresponding to value 8 $f_{IN0} = f_{SENSOR0} / 2^{CH0\_FIN\_DIV}$
3:0	RSV	read-write	0000	The reserved position can only be written with 0

6.6.9. FREF_DIV_CH0

Address 0x12, FREF_DIV_CH0

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH0_FREF_DIV							

FREF_DIV_CH0 Description

Position	Scope	Operate	Default Value	Description
7:0	CH0_FREF_DIV [7:0]	read-write	0000 0000	Set the reference clock divider for channel 0 000000000-11111111: corresponds to values from 1 to 256 $f_{REF0} = f_{CLK} / (CH0\_FREF\_DIV + 1)$

6.6.10. FIN_DIV_CH1

Address 0x13, FIN_DIV_CH1

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH1_FIN_DIV				RSV			

FIN_DIV_CH1 Description

Position	Scope	Operate	Default Value	Description
7:4	CH1_FIN_DIV [3:0]	read-write	0111	Set the channel 1 output frequency division value 000: Non-frequency division, corresponding to value 0 0001:2 frequency division, corresponding to value 1

				0010:4 frequency division, corresponding to value 2 0011:8 frequency division, corresponding to value 3 0100:16 frequency division, corresponding to value 4 0101:32 frequency division, corresponding to value 5 0110:64 frequency division, corresponding to value 6 0111:128 frequency division, corresponding to value 7 1xxx: 256 frequency division, corresponding to value 8 $f_{IN1} = f_{SENSOR0} / 2^{CH0\_FIN\_DIV}$
3:0	RSV	read-write	0000	The reserved position can only be written with 0

6.6.11. FREF_DIV_CH1

Address 0x14, FREF_DIV_CH1

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH1_FREF_DIV							

FREF_DIV_CH1 Description

Position	Scope	Operate	Default Value	Description
7:0	CH1_FREF_DIV [7:0]	read-write	0000 0000	Set the reference clock divider for channel 1 000000000-11111111: corresponds to values from 1 to 256 $f_{REF1} = f_{CLK} / (CH1\_FREF\_DIV + 1)$

6.6.12. STATUS

Address 0x17, STATUS

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OF_CH1	OF_CH0	DRDY_CH1	DRDY_CH0	RSV		ALERT_CH1	ALERT_CH0

STATUS Description

Position	Scope	Operate	Default Value	Description
7	OF_CH1	a slight pause in reading	0	The DATA_CH1 overflow flag is cleared when reading data.
6	OF_CH0	a slight pause in reading	0	The DATA_CH0 overflow flag is cleared when reading data.
5	DRDY_CH1	a slight pause in reading	0	Channel 1 conversion completed. Data read cleared.
4	DRDY_CH0	a slight pause in reading	0	Channel 0 conversion completed. Read data cleared.
3:2	RSV	a slight pause in reading	00	Keep
1	ALERT_CH1	a slight pause in reading	0	Clear the alarm trigger status bit in channel 1 and read the data
0	ALERT_CH0	a slight pause in reading	0	Channel 0 alarm trigger status bit, read data cleared

6.6.13. TH_MSB、TH_LSB

Address 0x19, TH_MSB

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TH							

Address 0x1A, TH_LSB

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TH							

TH_MSB & TH_LSB Description

Position	Scope	Operate	Default Value	Description
7:0	TH[15:8]	read-write	0010 0000	Configure 16-bit data and set the single-channel alarm trigger threshold After channel switching is completed, if DATA_CHx exceeds the threshold (TH), the ALERT_CHx flag is set to 1.
7:0	TH[7:0]	read-write	0000 0000	

6.6.14. TL_MSB、TL_LSB

Address 0x1B, TL_MSB

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TL							

Address 0x1C, TL_LSB

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TL							

TL_MSB & TL_LSB description

Position	Scope	Operate	Default Value	Description
7:0	TL[15:8]	read-write	0001 0000	Configure 16-bit data and set the single-channel alarm threshold. After channel conversion is completed, if DATA_CHx<TL, the ALERT_CHx alarm status bit is set to 0.
7:0	TL[7:0]	read-write	0000 0000	

6.6.15. CFG

Address 0x1F, CFG

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
REF_CLK_SEL	INTB_EN	INTB_MODE	CR			OS	SD

CFG explain

Position	Scope	Operate	Default Value	Description
7	REF_CLK_SEL	read-write	0	Reference clock selection 0: Select internal clock

				1: Select external clock
6	INTB_EN	read-write	1	Enable INTB output 0: INTB does not output the flag 1: INTB output alarm flag or conversion completion flag
5	INTB_MODE	read-write	0	INTB Output Source Selection 0: INTB output alarm flag 1: INTB output conversion completion flag
4:2	CR[2:0]	read-write	101	Time interval for continuous transition mode Convert every 60 seconds Convert every 001:30s 010: Convert every 10 seconds 011: Convert every 5 seconds Convert every 100:2s 101: Convert every 1 second 110:0.5s Change once 111:0.25s Convert once
1:0	OS,SD	read-write	00	Set channel conversion mode 00: Continuous conversion 01: Stop conversion 10: Continuous conversion (00 when read back) 11: Single conversion

6.6.16. CH_EN

Address 0x20, CH_EN

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH1_EN	CH0_EN	RSV					INTB_CH

CH_EN Description

Position	Scope	Operate	Default Value	Description
7	CH1_EN	read-write	1	Channel 1 enable bit control 0: Channel 1 is off 1: Channel 1 is on
6	CH0_EN	read-write	1	Channel 0 enable bit control 0: Channel 0 is off 1: Channel 0 is on
5:1	RSV	read-write	00000	The reserved position can only be written with 0
0	INTB_CH	read-write	0	INTB port output selection 0: Output channel 0 status information 1: Output channel 1 status information

6.6.17. RESET

Address 0x22, RESET

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RESET							

RESET Description

Position	Scope	Operate	Default Value	Description
7:0	RESET[7:0]	read-write	0000 0000	0111 1010: Initiate software reset, restoring the sensor to its power-on initial state with all registers reverting to default values. Other values: invalid (Read back as 0000 0000)

6.6.18. DRIVE_I_CH0

Address 0x23, DRIVE_I_CH0

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I0				RSV			

Drive_I_Ch0 Description

Position	Scope	Operate	Default Value	Description
7:4	I0[3:0]	read-write	0101	Set the drive current for channel 0 0000：0.5mA 0001：1.0mA 0010：1.5mA 0011：2.0mA 0100：2.5mA 0101：3.0mA 0110：3.5mA 0111：4.0mA 1000：4.5mA 1001：5.0mA 1010：5.5mA 1011：6.0mA 1100：6.5mA 1101：7.0mA 1110：7.5mA 1111：8.0mA
3:0	RSV	read-write	0000	The reserved position can only be written with 0

6.6.19. DRIVE_I_CH1

Address 0x24, DRIVE_I_CH1

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I1				RSV			

Drive_I_Ch1 Description

Position	Scope	Operate	Default Value	Description
7:4	I1[3:0]	read-write	0101	Set the drive current for channel 1 0000：0.5mA 0001：1.0mA 0010：1.5mA 0011：2.0mA 0100：2.5mA 0101：3.0mA 0110：3.5mA 0111：4.0mA 1000：4.5mA 1001：5.0mA 1010：5.5mA 1011：6.0mA 1100：6.5mA 1101：7.0mA 1110：7.5mA 1111：8.0mA
3:0	RSV	read-write	0000	The reserved position can only be written with 0

6.6.20. VC_SEL

Address 0x30, VC_SEL

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSV				VC		RSV	

VC_SEL Description

Position	Scope	Operate	Default Value	Description
7:4	RSV	read-write	0000	The reserved position can only be written with 0
3:2	VC[1:0]	read-write	00	Set reference voltage 00：2.5V 01：3.0V 10：1.8V 11：2.0V
1:0	RSV	read-write	00	The reserved position can only be written with 0

6.6.21. GLITCH_FILTER_EN

Address 0x33, GLITCH_FILTER_EN

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSV							FILTER_EN

GLITCH_FILTER_EN Description

Position	Scope	Operate	Default Value	Description
7:1	RSV	read-write	0000 000	The reserved position can only be written with 0
0	FILTER_EN	read-write	1	Enable anti-glitch filter 0: Turn off anti-glitch filter 1: Turn on anti-glitch filter

6.6.22. DEVICE_ID_MSB、DEVICE_ID_LSB

Address 0x7E, DEVICE_ID MSB

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DEVICE_ID							

Address 0x7F, DEVICE_ID_LSB

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DEVICE_ID							

DEVICE_ID_MSB & DEVICE_ID_LSB Description

Position	Scope	Operate	Default Value	Description
7:0	DEVICE_ID[15:8]	read only	0000 0001	Device ID 0x0120
7:0	DEVICE_ID[7:0]	read only	0010 0000	

7. Application and Implementation

7.1 Typical Application Circuits

The MC12G and MC12T require external LC resonant circuits. The C_{SENSOR} in the diagram represents the capacitance under test, while L denotes the resonant inductor. After conversion, the MCU reads the sensor's DATA_CHx data and calculates the C_{SENSOR} value using the formula in Section 6.3.3. The VT signal is inversely proportional to temperature, and the MCU can determine the temperature by sampling and applying the formula in Section 6.3.8.

Beyond its standard application modes, the MC12G also functions as a capacitive switch. Upon power-on, the sensor automatically enters continuous conversion mode with 1-second measurement intervals. The INTB pin activates the alarm flag when DATA_CH0 exceeds the threshold (0x2000), and deactivates it when DATA_CH0 falls below the lower limit (0x1000).

The MC12G supports two capacitor connection configurations. For dual-electrode detection, one terminal of the capacitor connects to the C0A/C1A pins while the other terminal connects to the C0B/C1B pins, with the C0B/C1B pins internally grounded through the sensor (as shown in Figure 7.1-1). For single-terminal detection, the capacitor's positive terminal connects to the inductor L and the negative terminal to GND (as shown in Figure 7.1-2). To enable the sensor to enter low-power mode during non-conversion periods, two conditions must be met: when using internal clock, the CLKIN pin must be set to low level; when using external clock, the CLKIN pin

must also be set to low level during non-conversion periods.

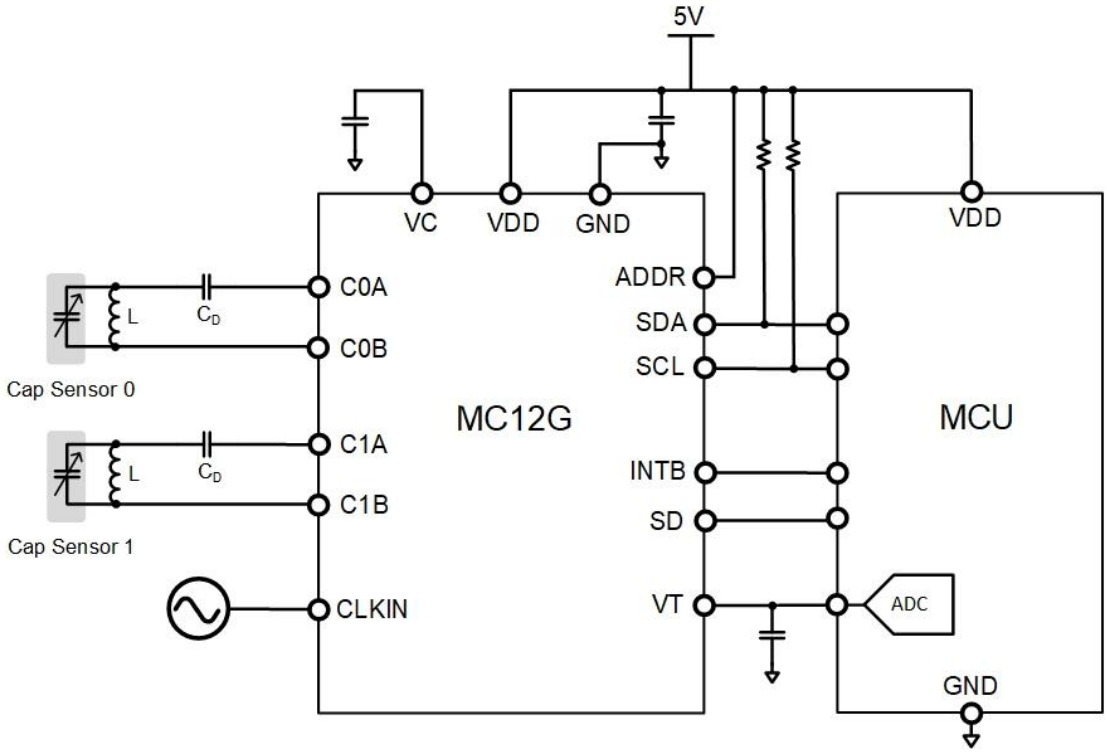


Figure 7.1-1: Typical Application Circuit Diagram of MC12G Dual-Electrode Detection

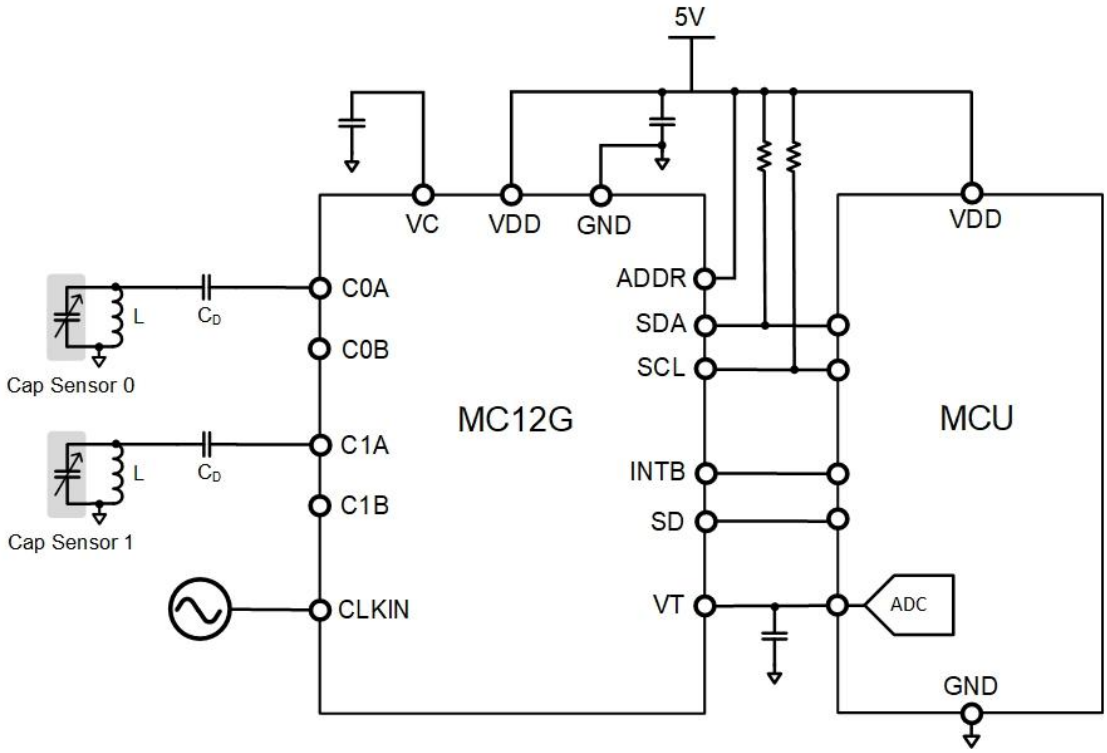


Figure 7.1-2: Typical Application Circuit Diagram of MC12G Single-Electrode Detection

The MC12T tester only supports connecting the positive terminal of the capacitor under test to

inductor L and the negative terminal to GND, as shown in Figure 7.1-3.

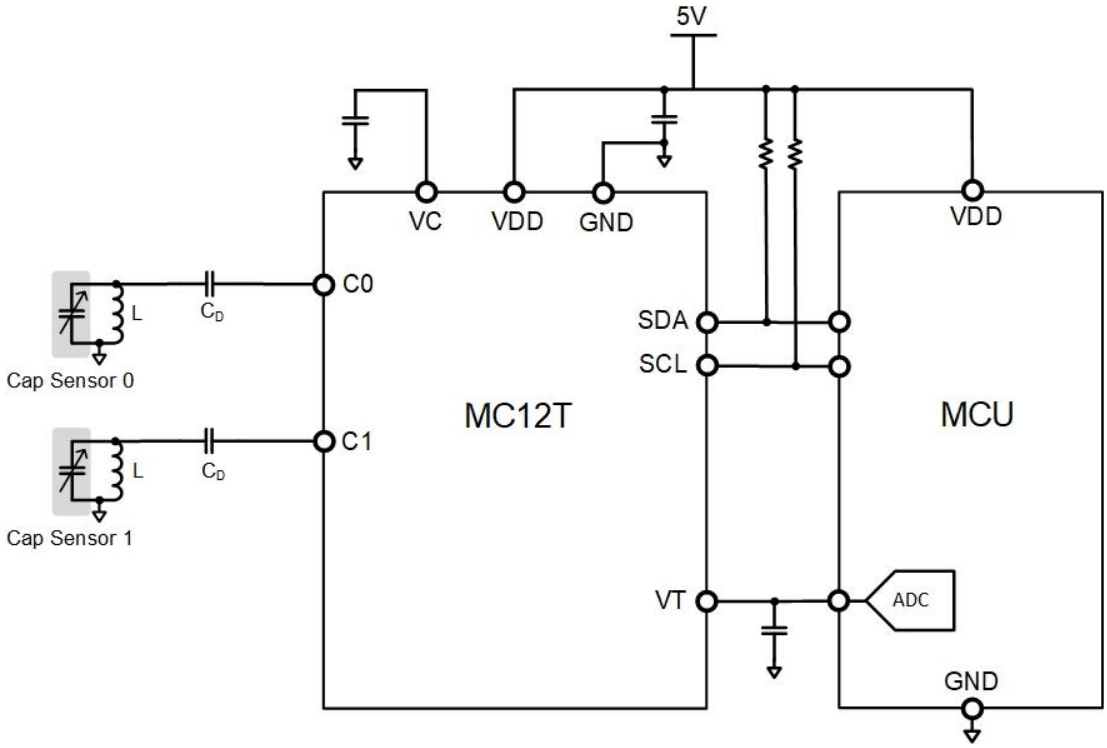


Figure 7.1-3: Typical Application Circuit Diagram of MC12T Single-Electrode Detection

For MC12G and MC12T, the recommended external capacitance for the VC pin is 4.7nF, and for the VT pin, it is 1nF.

7.2 Typical Application Examples

The single-channel application's transition time (T_{CV}) is 10ms, with an inductor of 100nH and a capacitor of 150pF. The total ground capacitance of the sensor's C0A pin and its parasitic capacitance is typically 66pF (C_P). The combined ground capacitance (C_F) of the parallel-connected C_P and C_{SENSOR} is:

$$C_F = \frac{C_P * C_D}{C_P + C_D} = 45.8pF$$

The maximum oscillation frequency is then calculated by LC resonance formula:

$$f_{SENSOR,MAX} = \frac{1}{2\pi * \sqrt{L * C_F}} = 74.3MHz$$

This is the maximum oscillation frequency. When the C_{SENSOR} is connected to the circuit, the oscillation frequency will decrease. Select the internal 2.4MHz clock of the sensor for counting. The configuration process of each relevant register is as follows:

i. Configure channel 0 conversion by setting the CH_EN register to 0x40.

ii. Configure the internal clock for counting by setting bit7 of the CFG register to 0.

iii. To ensure measurement accuracy, f_{REF} must satisfy the following conditions:

$$f_{REF0} = f_{CLK} / (CH0\_FREF\_DIV+1) > 2.5 * f_{SENSOR,MAX} / 2^{CH0\_FIN\_DIV}$$

f_{CLK}=2.4MHz. Setting CH0_FREF_DIV to 0 and CH0_FIN_DIV to 7 satisfies the specified requirements. Accordingly, configure the FREF_CH0_DIV register to 0x00 and the FIN_CH0_DIV register to 0x70.

iv. To ensure the oscillator starts oscillating while controlling the amplitude, set the drive current to 3mA and configure the DRIVE_I_CH0 register to 0x50. If oscillation still fails, gradually increase the drive current value.

v. To ensure sufficient setup time, set T_{SET0} to ≥100us and configure the SCNT_CH0 register to 0x0F, resulting in an actual T_{SET0} of 100us.

vi. Calculate the counting time T_{CNT}:

$$T_{CNT0} = T_{CV0} - T_{START} - T_{SET0} - T_{DELAY} = 10000 - 200 - 100 - 1.6 = 9.7ms$$

$$T_{CNT0} = RCNT0 / f_{REF0}$$

Based on the previous configuration, f_{REF0}=2.4MHz. Therefore, RCNT0=23280, with a maximum resolution of over 13 bits. Set the RCNT_CH0_MSB register to 0x5A and the RCNT_CH0_LSB register to 0xF0.

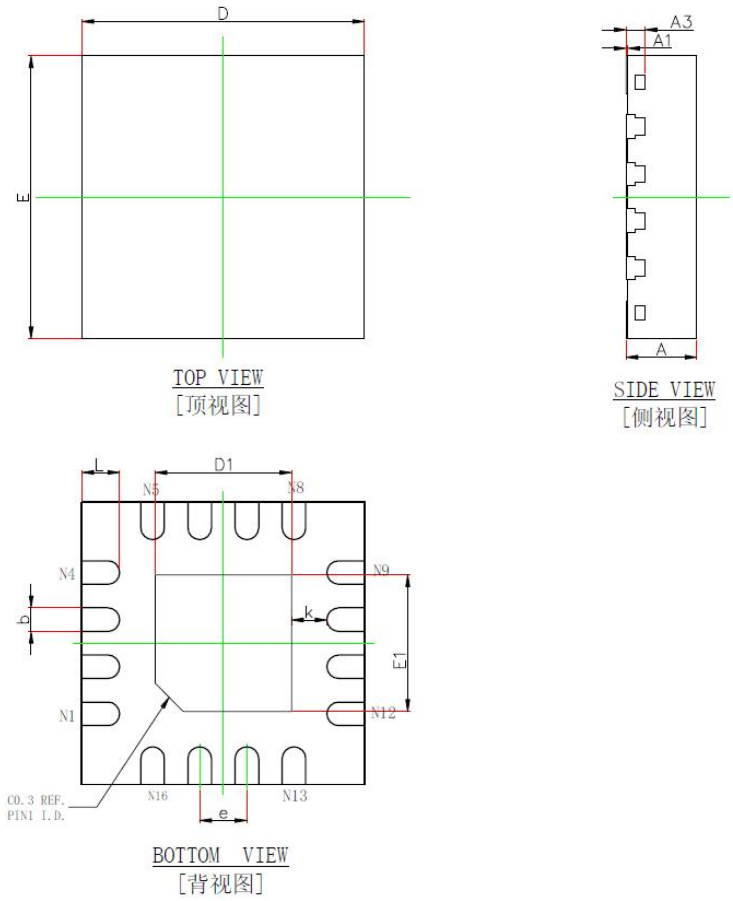
vii. For the MC12G, to utilize the interrupt signal from the INTB pin, set bit6 of the CFG register to 1 and bit0 to 0. This configuration enables INTB to output the comparison result of conversion data, with the comparison thresholds stored in the TH_MSB/TH_LSB and TL_MSB/TL_LSB registers respectively.

7.3 Inductance self-resonant Frequency

An inductor has a parasitic capacitance, which corresponds to a specific self-resonant frequency. To avoid entering the self-resonant state, it is recommended that the oscillation signal frequency f_{SENSOR} be less than 0.8 * f_{SR} in practical applications.

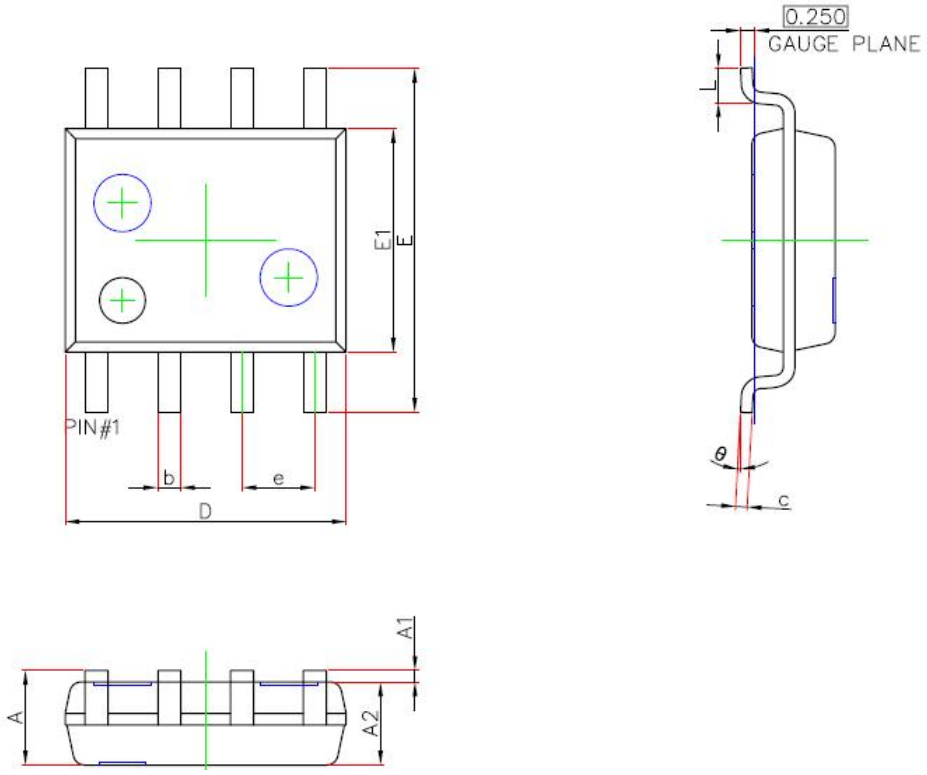
8. Package

8.1 MC12G QFN16 3.0*3.0*0.75mm Product Dimensions and Specifications Diagram



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.350	1.550	0.053	0.061
E1	1.350	1.550	0.053	0.061
k	0.375REF.		0.015REF.	
b	0.200	0.300	0.008	0.012
e	0.500BSC.		0.020BSC.	
L	0.300	0.500	0.012	0.020

8.2 MC12T SOP8 4.9*3.9*1.6mm Product Dimensions and Specifications Diagram



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

9. Ordering Information

Part Number	Package Type	Package Qty
MC12G	QFN16	5000
MC12T	SOP8	4000