20V N-Channel Signal MOSFET

Features

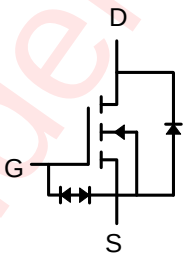
- N-Channel Switch with Low $R_{DS(ON)}$
- Surface Mount Package
- Operated at Low Logic Level Gate Drive
- ESD protected
- SOT723-3L Package

General Description

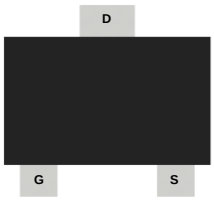
Product Summary	
V_{DS}	20V
$R_{DS(ON)}$	220mΩ (Typ.)@ V_{GS}= 2.5V
	170mΩ (Typ.)@ V_{GS}= 4.5V
I_D	0.75A

Applications

- Load/Power Switching
- Interfacing Switching
- Battery Management for Ultra Small Portable Electronics
- Logic Level Shift

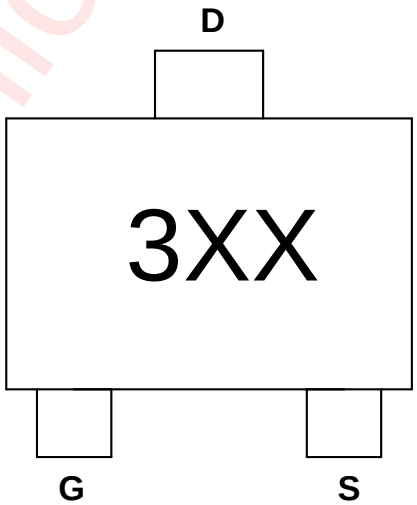


SOT723



Pin Configuration and Top Mark

AW402011NSTR
(Top View)



3 – AW402011NSTR
XX – Production Tracing Code

Ordering Information

Part Number	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW402011NSTR	SOT723-3L	3	MSL3	RoHS +HF	8000 units /tape & reel

Absolute Maximum Ratings (NOTE1)

Symbol	Parameter	Rating	Unit
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	±10	V
I_D	Drain Current(DC) (NOTE 5)	0.75	A
I_{DM}	Drain Current(Pulse) (NOTE 2,3)	1.8	A
P_D	Power Dissipation	0.2	W
T_J	Maximum Operating Junction Temperature	150	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C
V_{ESD}	Human Body Model (NOTE 6)	±1	kV

Thermal Information

Symbol	Parameter	Condition	Value	Unit
$R_{\theta JA}$	Maximum Junction to Ambient (NOTE 2, 4)	Steady-State	485	°C/W

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Mounted on FR-4 board using the minimum recommended pad size.

NOTE3: Test condition 10μs 25°C.

NOTE4: Thermal resistance from junction to ambient is highly dependent on PCB layout.

NOTE5: Rated according to $R_{\theta JA}$.

NOTE6: HBM Standards: ESDA/JEDEC JS-001-2017.

Static Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D= 250μA, V_{GS}= 0V	20	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}= 20V, V_{GS}= 0V	-	-	1	μA
I_{GSS}	Gate Leakage Current	V_{DS}= 0V, V_{GS}= ±10V	-	-	±20	μA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D= 250μA	0.35	-	1.1	V
$R_{DS(ON)}$	Static Drain to Source On-Resistance	V_{GS}= 4.5V, I_D= 0.15A	-	170	280	mΩ
		V_{GS}= 2.5V, I_D= 0.15A	-	220	360	mΩ
		V_{GS}= 1.8V, I_D= 0.15A		300	480	mΩ
V_{SD}	Diode Forward Voltage	I_S= 0.15A, V_{GS}= 0V	-	0.8	1.2	V
DYNAMIC PARAMETERS						
R_g	Gate Resistance	f= 1MHz	-	45	-	Ω
C_{iss}	Input Capacitance	V_{GS}= 0V, V_{DS}= 16V, f= 1MHz	-	55	-	pF
C_{oss}	Output Capacitance		-	11	-	pF
C_{rss}	Reverse Transfer Capacitance		-	11	-	pF
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{DS} = 10V,V_{GS} = 4.5V,I_D = 0.15A	-	0.96	-	nC
Q_{gs}	Gate Source Charge		-	0.11	-	nC
Q_{gd}	Gate Drain Charge		-	0.19	-	nC
$t_{d(on)}$	Turn-On Delay Time	V_{DS}= 10V, R_g= 10Ω, I_D =500mA V_{GS}= 4.5V,	-	5.2	-	ns
t_r	Turn-On Rise Time		-	4.3	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	18.7	-	ns
t_f	Turn-Off Fall Time		-	8.3	-	ns

Typical Electrical and Thermal Characteristics

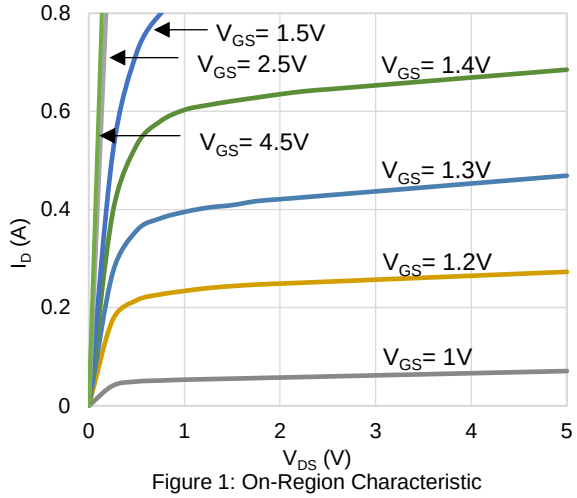


Figure 1: On-Region Characteristic

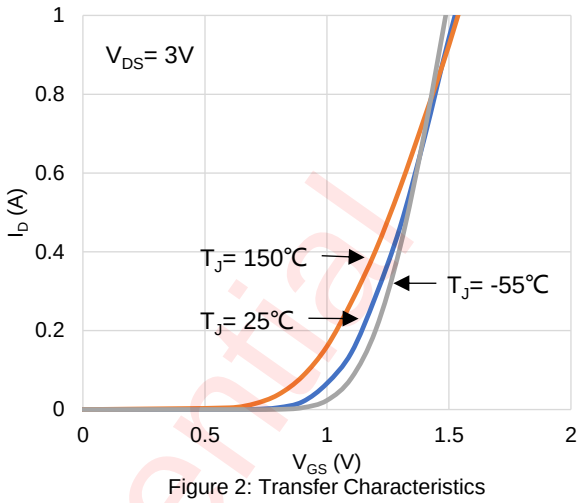


Figure 2: Transfer Characteristics

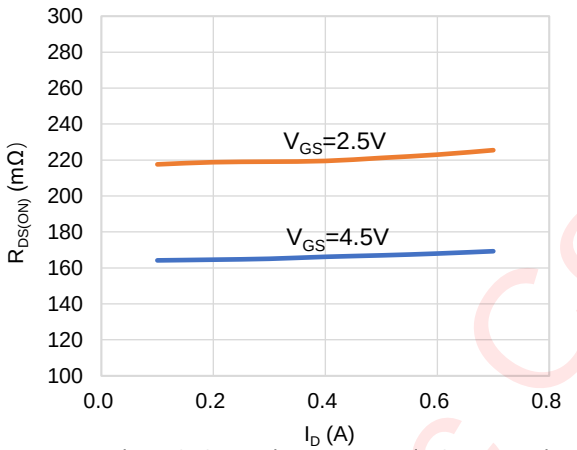


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

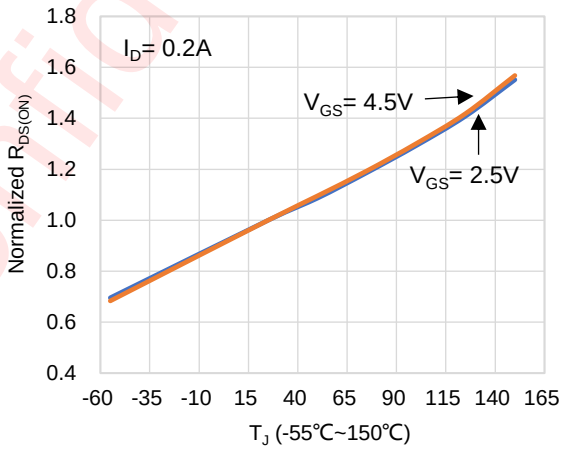


Figure 4: Normalized On-Resistance vs. Junction Temperature

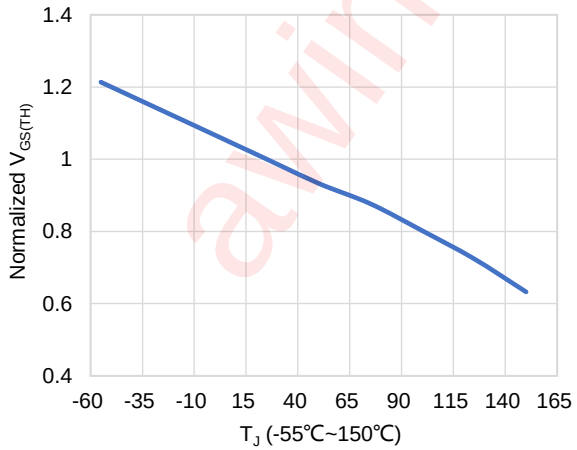


Figure 5: Normalized Gate Threshold Voltage vs. Junction Temperature

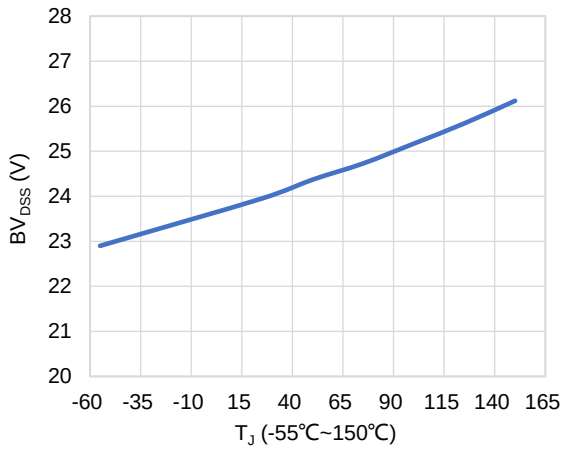


Figure 6: Drain-Source Breakdown Voltage vs. Junction Temperature

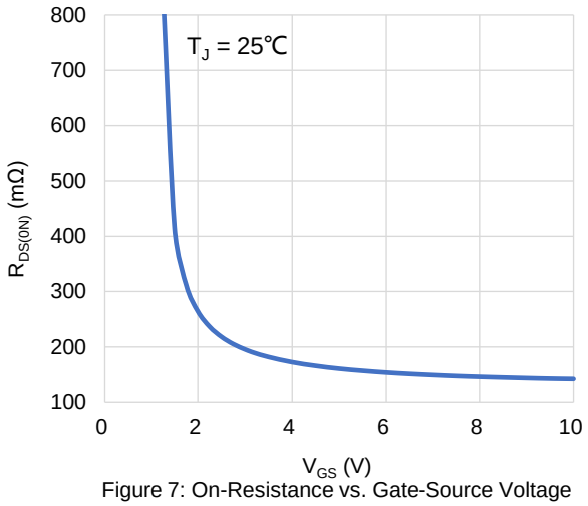


Figure 7: On-Resistance vs. Gate-Source Voltage

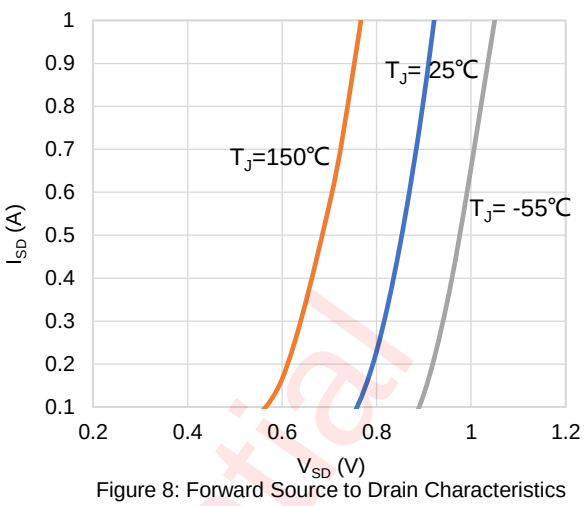


Figure 8: Forward Source to Drain Characteristics

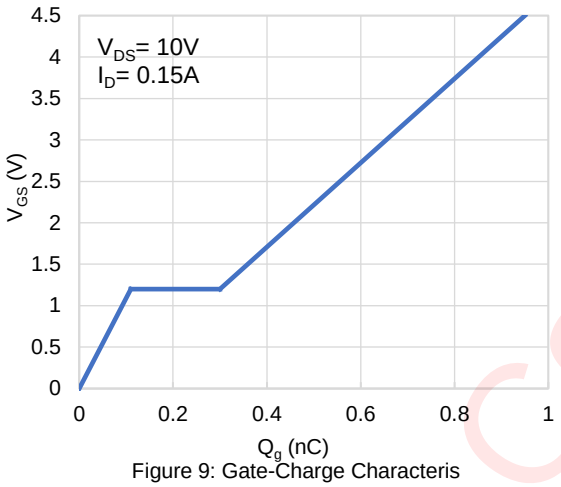


Figure 9: Gate-Charge Characteris

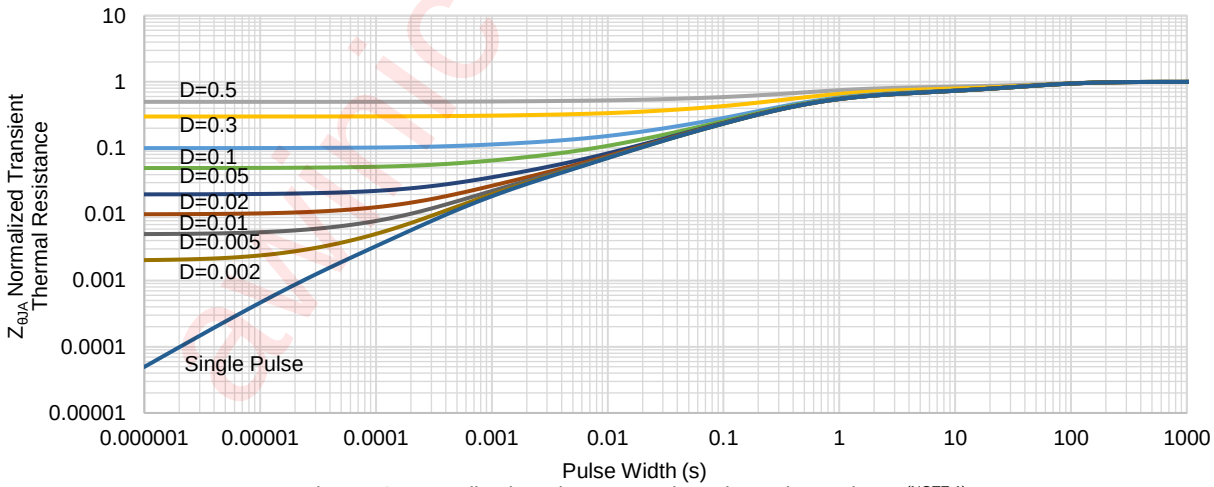
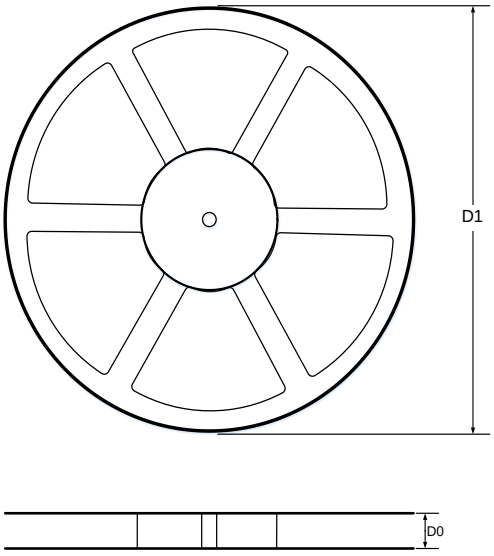


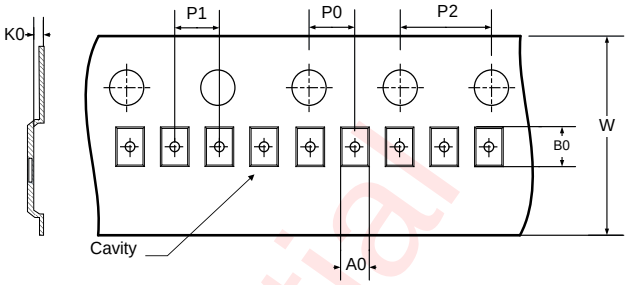
Figure 10: Normalized Maximum Transient Thermal Impedance (NOTE 1)

Tape and Reel Information

REEL DIMENSIONS

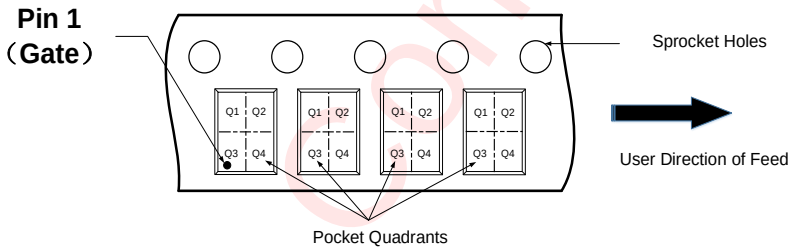


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1（Gate） ORIENTATION IN TAPE



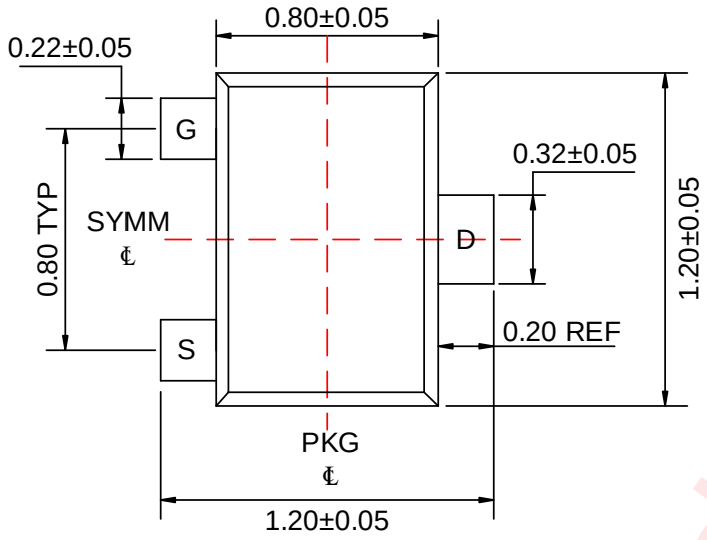
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

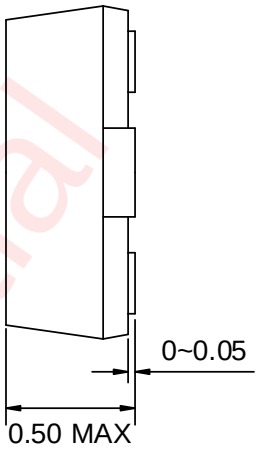
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 (Gate) Quadrant
178	9.5	1.45	1.31	0.61	2	2	4	8	Q3

All dimensions are nominal

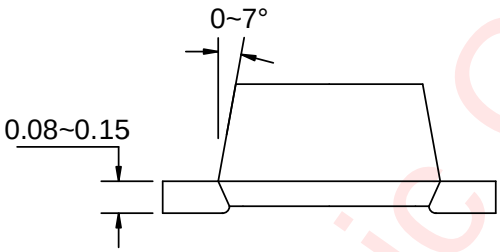
Package Description



Top View



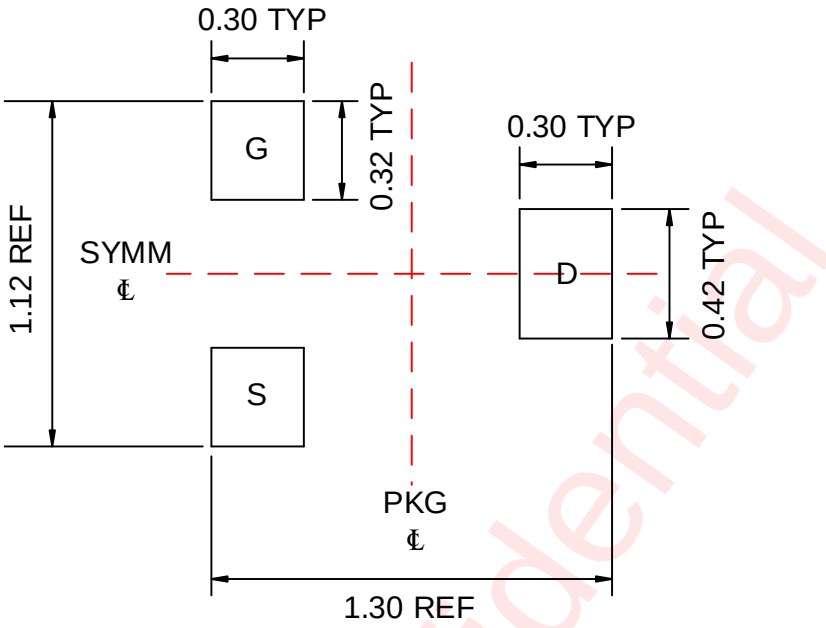
Side View

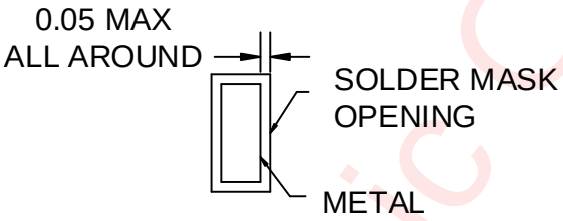


Side View

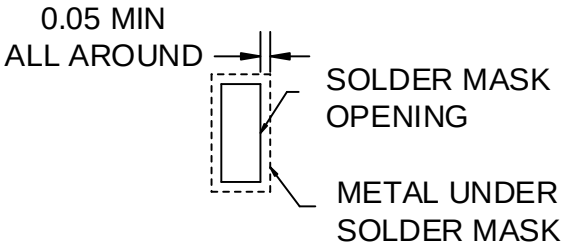
Unit：mm

Land Pattern Data





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Sep. 2022	Official Released
V1.1	Oct. 2022	Updated Page2 “Ordering Information” “Delivery Form” to “8000/tape and reel” Updated Page2 “Absolute Maximum Ratings” “V_{GS}” Rating to “±10”
V1.2	Dec. 2023	Updated Package Description and Land Pattern Data (Page7 and Page8)

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