Low Noise Amplifier with Gain Control for Low Band

Features

- Operating frequency: 600MHz to 960MHz
- Dynamic range 33dB, 7 gain steps
- Maximum power gain: 21.5dB
- Low noise figure: 0.7dB
- Small size, QFN 1.5mm x 1.1mm-11L package
- MIPI RFFE 3.0 Compatible
- USID selection via USID pin

Applications

- 5G Smartphones and tablets
- Multi-mode GSM/CDMA/WCDMA/LTE/NR Low Band receiving

General Description

The AW15058LQNR is a highly integrated multi-mode multi-gain LNA, dedicated to Low Band receiving.

The AW15058LQNR increases the overall system dynamic range and leads to more flexibility in the front-end with the gain control feature.

The AW15058LQNR is compatible with MIPI V3.0 control interface, which is a key requirement for many cellular transceivers.

The AW15058LQNR is provided in a compact QFN 1.5mm x 1.1mm-11L package.

The pin configuration is shown in Figure2. The functional block diagram is shown in Figure3.

Typical Application Circuit

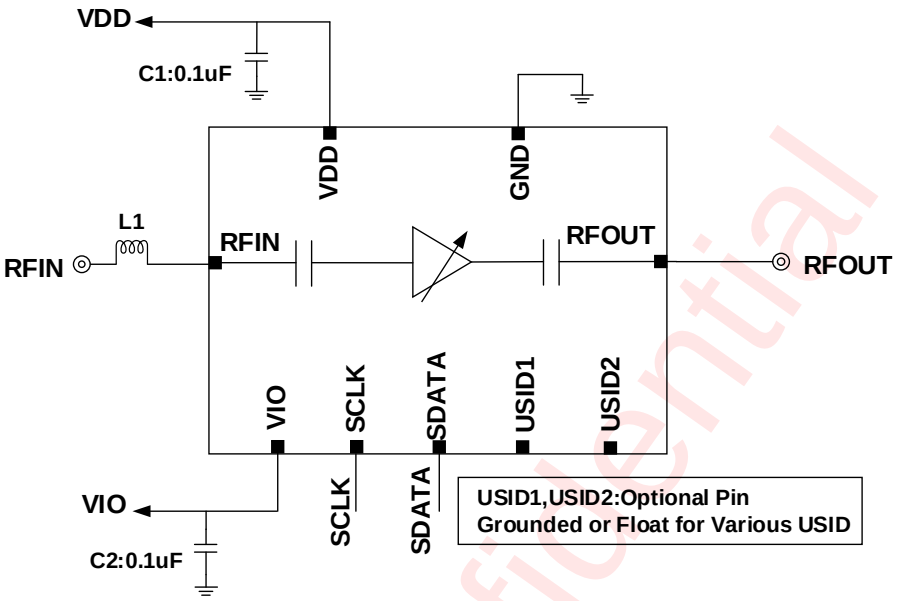
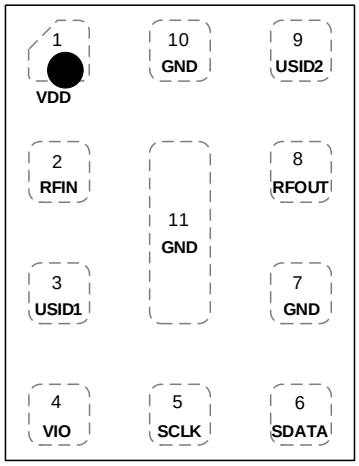


Figure 1 Typical Application Circuit

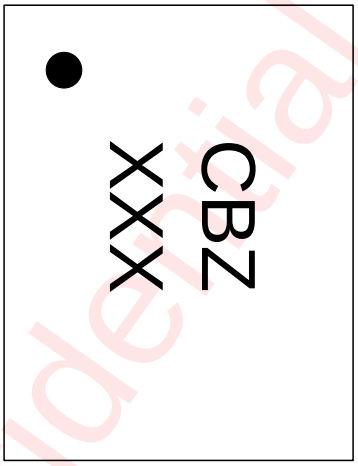
Component	Matching Band	Vendor	Type	Part Number & value
L1	600MHz–660MHz	Murata	Wired inductor, high Q	LQW15AN, 43nH
	700MHz–830MHz	Murata	Wired inductor, high Q	LQW15AN, 30nH
	830MHz –960MHz	Murata	Wired inductor, high Q	LQW15AN, 22nH

Pin Configuration And Top Mark

AW15058LQNR
(Top View)



AW15058LQNR Marking
(Top View)



CBZ- AW15058LQNR
XXX- Production Tracing Code

Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	VDD	1.2/1.8V for LNA
2	RFIN	RF input port
3	USID1	External USID1 pin
4	VIO	1.8V for MIPI
5	SCLK	MIPI interface clock input
6	SDATA	MIPI interface data read/write
7	GND	Ground
8	RFOUT	RF output port
9	USID2	External USID2 pin
10	GND	Ground
11	GND	Ground

Functional Block Diagram

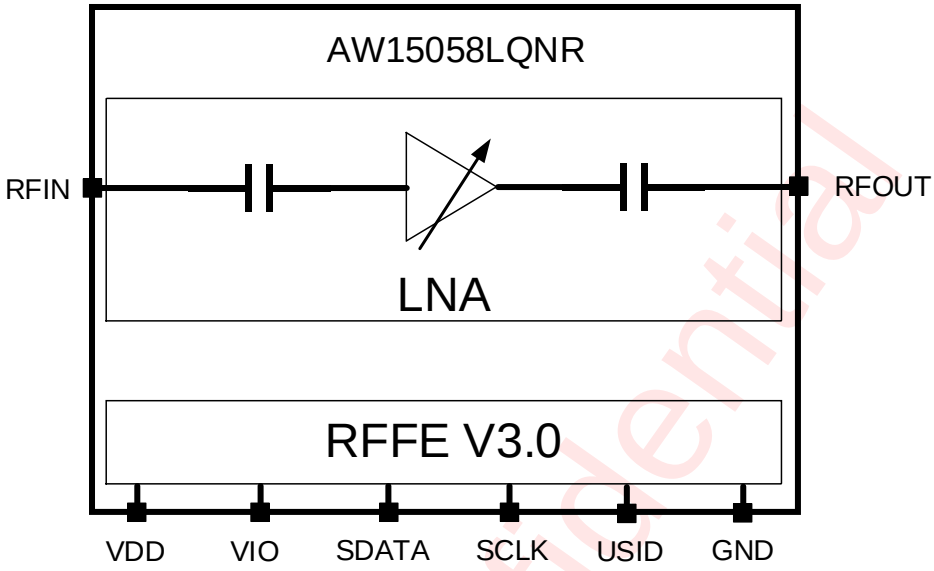


Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW15058LQNR	-40℃～90℃	QFN 1.5mmX1.1mm -11L	CBZ	MSL1	ROHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS	Condition	RANGE
Supply Voltage VIO for MIPI	T_A=+25 °C	-0.3V to +2.2V
Supply Voltage VDD	T_A=+25 °C	-0.3V to +2.2V
Interface Input Voltage Range SDATA, SCLK,USID	T_A=+25 °C	-0.3V to +2.2V
Max input power (Gain mode)	CW, VSWR=1:1,T_A=+25 °C	25dBm
Maximum Junction temperature T_{JMAX}		125 °C
Operating free-air temperature range		-40°C to 90°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD		
HBM (Human Body Model)(NOTE 2)		±2000V
CDM (Charged Device Model)(NOTE 3)		±1000V

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE3: All pins. Test method: ESDA/JEDEC JS-002-2018.

Truth Table

Mode Select	Udr_00<0>	Udr_01<4>
LNA disable	0	0
LNA enable	1	0
	0	1
	1	1

Register Name	Register Address	State		Data(HEX)
LNA Gain Control	0x01	830-960MHz	G7	10
			G6	11
			G5	13
			G4	15
			G3	16
			G2	18
			G1	19
		700-830MHz	G7	D0
			G6	D1
			G5	D3
			G4	D5
			G3	D6
			G2	D8
			G1	D9
		600-660MHz	G7	F0
			G6	F1
			G5	F3
			G4	F5
			G3	F6
			G2	F8
			G1	F9

Electrical Characteristics

DC Specifications

PARAMETER	Symbol	TEST CONDITION	MIN	TYP	MAX	UNIT
VIO Supply Voltage	V_{IO}		1.62	1.8	1.98	V
VIO Supply Current	I_{IO}				30	μA
SDATA,SCLK,USID Input Voltage High	V_{IH}	Must not exceed V_{IO} voltage	0.8*V_{IO}	V_{IO}	1.98	V
SDATA,SCLK,USID Input Voltage Low	V_{IL}	Must not exceed V_{IO} voltage	0		0.2*V_{IO}	V
VDD Supply Voltage	V_{DD}		1.08	1.2	1.35	V
			1.62	1.8	1.98	V
VDD Supply Current	$I_{DD,LOW}$	Low Power Mode		0.1	5.0	μA
RF turn on time	T_{ON}	From LNA off mode to within 0.5dB gain error of steady state gain			1.0	μs
RF turn off time	T_{OFF}	From LNA enabled to less than -20dB S21			1.0	μs
Gain settling time	T_{SW}	Gain switching between any two of gain gears to be within 0.5dB gain error of steady state gain			1.0	μs

Typically, V_{DD}=1.2V and T_A=+25°C, V_{IO}=1.8V, All data measured on AW15058LQNR's EVB

PARAMETER	Symbol	TEST CONDITION	MIN	TYP	MAX	UNIT
RF Characteristics @ 600MHz-660MHz						
VDD Supply Current	G7			7.0	9.0	mA
	G6			6.0	8.0	mA
	G5			4.5	6.0	mA
	G4			3.5	5.0	mA
	G3			2.8	4.0	mA
	G2			0.06	0.1	mA
	G1			0.06	0.1	mA
Gain	G7		19.0	21.5	23.0	dB
	G6		16.0	18.5	20.5	dB
	G5		10.0	13.0	15.0	dB
	G4		4.0	6.5	8.0	dB
	G3		-2.0	0.5	2.0	dB
	G2		-8.0	-5.8	-4.0	dB
	G1		-14.0	-11.8	-10.0	dB
NF	G7	PCB loss subtracted		0.8	1.1	dB
	G6			0.9	1.2	dB
	G5			1.0	1.5	dB
	G4			3.0	4.0	dB
	G3			4.5	5.5	dB
	G2			6.0	7.5	dB
	G1			12.0	13.0	dB
IIP3	G7	P1 = P2 = -49dBm	-11.0	-8.0		dBm
	G6	P1 = P2 = -46dBm	-9.5	-6.5		dBm
	G5	P1 = P2 = -40dBm	-8.0	-5.0		dBm
	G4	P1 = P2 = -34dBm	-3.0	0		dBm
	G3	P1 = P2 = -28dBm	-0.5	2.5		dBm
	G2	P1 = P2 = -22dBm	15.0	20.0		dBm
	G1	P1 = P2 = -16dBm	15.0	20.0		dBm
P1dB	G7		-19.0	-16.0		dBm
	G6		-16.0	-13.0		dBm
	G5		-14.5	-11.5		dBm
	G4		-11.5	-8.5		dBm
	G3		-11.5	-8.5		dBm
	G2		2.0	5.0		dBm
	G1		2.0	5.0		dBm
Input Return Loss	G1-G7		6.0	10.0		dB

PARAMETER	Symbol	TEST CONDITION	MIN	TYP	MAX	UNIT
Output Return Loss	G1-G7		6.0	10.0		dB
Reverse Isolation	G7		27	33		dB
K	G1-G7	LNA mode	1.0			
RF Characteristics @ 700MHz-830MHz						
VDD Supply Current	G7			7.0	9.0	mA
	G6			6.0	8.0	mA
	G5			4.5	6.0	mA
	G4			3.5	5.0	mA
	G3			2.8	4.0	mA
	G2			0.06	0.1	mA
	G1			0.06	0.1	mA
Gain	G7		19.0	21.5	23.0	dB
	G6		16.0	18.5	20.0	dB
	G5		10.0	12.5	14.0	dB
	G4		4.0	7.0	8.5	dB
	G3		-2.0	1.0	2.0	dB
	G2		-8.0	-6.0	-4.0	dB
	G1		-14.0	-11.5	-10.0	dB
NF	G7	PCB loss subtracted		0.8	1.1	dB
	G6			0.9	1.2	dB
	G5			1.0	1.5	dB
	G4			2.8	4.0	dB
	G3			4.4	5.5	dB
	G2			5.9	7.5	dB
	G1			11.5	13.0	dB
IIP3	G7	P1 = P2 = -49dBm	-10.5	-7.5		dBm
	G6	P1 = P2 = -46dBm	-9.0	-6.0		dBm
	G5	P1 = P2 = -40dBm	-8.0	-5.0		dBm
	G4	P1 = P2 = -34dBm	-5.0	-2.0		dBm
	G3	P1 = P2 = -28dBm	-2.0	1.5		dBm
	G2	P1 = P2 = -22dBm	17.0	22.0		dBm
	G1	P1 = P2 = -16dBm	17.0	22.0		dBm
P1dB	G7		-19.0	-16.0		dBm
	G6		-16.0	-13.0		dBm
	G5		-14.0	-11.0		dBm
	G4		-12.0	-9.0		dBm
	G3		-11.5	-8.5		dBm
	G2		2.0	6.0		dBm

PARAMETER	Symbol	TEST CONDITION	MIN	TYP	MAX	UNIT
	G1		2.0	6.0		dBm
Input Return Loss	G1-G7		6.0	10.0		dB
Output Return Loss	G1-G7		6.0	10.0		dB
Reverse Isolation	G7	G7	27	33		dB
K	G1-G7		1.0			
RF Characteristics @ 830MHz-960MHz						
VDD Supply Current	G7			7.0	9.0	mA
	G6			6.0	8.0	mA
	G5			4.5	6.0	mA
	G4			3.5	5.0	mA
	G3			2.5	4.0	mA
	G2			0.06	0.1	mA
	G1			0.06	0.1	mA
Gain	G7		19.0	21.5	23.0	dB
	G6		16.0	18.5	20.0	dB
	G5		10.0	12.5	14.0	dB
	G4		4.0	6.8	8.5	dB
	G3		-2.0	0.8	2.0	dB
	G2		-8.0	-5.5	-4.0	dB
	G1		-14.0	-11.5	-10.0	dB
NF	G7	PCB loss subtracted		0.7	1.1	dB
	G6			0.9	1.2	dB
	G5			1.0	1.5	dB
	G4			2.6	4.0	dB
	G3			4.4	5.5	dB
	G2			5.0	7.5	dB
	G1			9.6	13.0	dB
IIP3	G7	P1 = P2 = -49dBm	-10.0	-7.0		dBm
	G6	P1 = P2 = -46dBm	-7.8	-4.8		dBm
	G5	P1 = P2 = -40dBm	-7.3	-4.3		dBm
	G4	P1 = P2 = -34dBm	-4.5	-1.5		dBm
	G3	P1 = P2 = -28dBm	-1.0	2.0		dBm
	G2	P1 = P2 = -22dBm	18.0	23.0		dBm
	G1	P1 = P2 = -16dBm	20.0	25.0		dBm
P1dB	G7		-20.0	-17.0		dBm
	G6		-16.5	-13.5		dBm
	G5		-14.5	-11.5		dBm
	G4		-12.0	-9.0		dBm

PARAMETER	Symbol	TEST CONDITION	MIN	TYP	MAX	UNIT
	G3		-11.0	-8.0		dBm
	G2		2.0	7.0		dBm
	G1		2.0	7.0		dBm
Input Return Loss	G1-G7		6.0	10.0		dB
Output Return Loss	G1-G7		6.0	10.0		dB
Reverse Isolation	G7	G7	27	31		dB
K	G1-G7		1.0			

Typically, V_{DD}=1.8V and T_A=+25°C, V_{IO}=1.8V, All data measured on AW15058LQNR's EVB

PARAMETER	Symbol	TEST CONDITION	MIN	TYP	MAX	UNIT
RF Characteristics @ 600MHz-660MHz						
VDD Supply Current	G7			7.1	9.0	mA
	G6			6.5	8.0	mA
	G5			5.0	6.0	mA
	G4			3.8	5.0	mA
	G3			2.8	4.0	mA
	G2			0.07	0.1	mA
	G1			0.07	0.1	mA
Gain	G7		19.0	21.5	23.5	dB
	G6		16.0	19.0	21.0	dB
	G5		10.0	13.2	15.0	dB
	G4		4.0	6.5	8.5	dB
	G3		-2.0	0.5	2.0	dB
	G2		-8.0	-6.0	-4.0	dB
	G1		-14.0	-12.0	-10.0	dB
NF	G7	PCB loss subtracted		0.8	1.1	dB
	G6			0.9	1.2	dB
	G5			1.0	1.5	dB
	G4			3.0	4.0	dB
	G3			4.5	5.5	dB
	G2			6.2	7.5	dB
	G1			11.8	13.0	dB

PARAMETER	Symbol	TEST CONDITION	MIN	TYP	MAX	UNIT
IIP3	G7	P1 = P2 = -49dBm	-10.2	-7.2		dBm
	G6	P1 = P2 = -46dBm	-9.0	-6.0		dBm
	G5	P1 = P2 = -40dBm	-8.3	-5.3		dBm
	G4	P1 = P2 = -34dBm	-3.0	0		dBm
	G3	P1 = P2 = -28dBm	-0.5	2.5		dBm
	G2	P1 = P2 = -22dBm	15.0	20.0		dBm
	G1	P1 = P2 = -16dBm	15.0	20.0		dBm
P1dB	G7		-17.0	-14.0		dBm
	G6		-14.5	-11.5		dBm
	G5		-12.5	-9.5		dBm
	G4		-9.8	-6.8		dBm
	G3		-10.0	-7.0		dBm
	G2		2.0	5.0		dBm
	G1		2.0	5.0		dBm
Input Return Loss	G1-G7		6.0	10.0		dB
Output Return Loss	G1-G7		6.0	10.0		dB
Reverse Isolation	G7	G7	27	35		dB
K	G1-G7		1.0			
RF Characteristics @ 700MHz-830MHz						
VDD Supply Current	G7			7.1	9.0	mA
	G6			6.5	8.0	mA
	G5			5.0	6.0	mA
	G4			3.8	5.0	mA
	G3			2.5	4.0	mA
	G2			0.07	0.1	mA
	G1			0.07	0.1	mA
Gain	G7		19.0	21.5	23.0	dB
	G6		16.0	19.0	20.5	dB
	G5		10.0	13.0	14.5	dB
	G4		4.0	7.0	9.0	dB
	G3		-2.0	1.0	2.5	dB
	G2		-8.0	-5.5	-4.0	dB
	G1		-14.0	-11.5	-10.0	dB
NF	G7	PCB loss subtracted		0.8	1.1	dB
	G6			0.9	1.2	dB
	G5			1.0	1.5	dB
	G4			2.8	4.0	dB
	G3			4.2	5.5	dB

PARAMETER	Symbol	TEST CONDITION	MIN	TYP	MAX	UNIT
	G2			5.9	7.5	dB
	G1			11.7	13.0	dB
IIP3	G7	P1 = P2 = -49dBm	-9.0	-6.0		dBm
	G6	P1 = P2 = -46dBm	-8.0	-5.0		dBm
	G5	P1 = P2 = -40dBm	-7.5	-4.5		dBm
	G4	P1 = P2 = -34dBm	-5.0	-2.0		dBm
	G3	P1 = P2 = -28dBm	-1.5	1.5		dBm
	G2	P1 = P2 = -22dBm	16.5	21.5		dBm
	G1	P1 = P2 = -16dBm	17.0	22.0		dBm
P1dB	G7		-17.5	-14.5		dBm
	G6		-15.0	-12.0		dBm
	G5		-12.5	-9.5		dBm
	G4		-10.5	-7.5		dBm
	G3		-10.5	-7.5		dBm
	G2		2.0	6.0		dBm
	G1		2.0	6.0		dBm
Input Return Loss	G1-G7		6.0	10.0		dB
Output Return Loss	G1-G7		6.0	10.0		dB
Reverse Isolation	G7	G7	27	34		dB
K	G1-G7		1.0			
RF Characteristics @ 830MHz-960MHz						
VDD Supply Current	G7			7.1	9.0	mA
	G6			6.5	8.0	mA
	G5			5.0	6.0	mA
	G4			3.8	5.0	mA
	G3			2.7	4.0	mA
	G2			0.07	0.1	mA
	G1			0.07	0.1	mA
Gain	G7		19.0	22.0	23.0	dB
	G6		16.0	19.0	20.5	dB
	G5		10.0	13.0	14.5	dB
	G4		4.0	7.0	9.0	dB
	G3		-2.0	1.0	2.5	dB
	G2		-8.0	-5.5	-4.0	dB
	G1		-14.0	-11.5	-10.0	dB
NF	G7	PCB loss subtracted		0.7	1.1	dB
	G6			0.8	1.2	dB
	G5			1.0	1.5	dB

PARAMETER	Symbol	TEST CONDITION	MIN	TYP	MAX	UNIT
	G4			2.6	4.0	dB
	G3			4.4	5.5	dB
	G2			5.0	7.5	dB
	G1			9.6	13.0	dB
IIP3	G7	P1 = P2 = -49dBm	-8.5	-5.5		dBm
	G6	P1 = P2 = -46dBm	-7.0	-4.0		dBm
	G5	P1 = P2 = -40dBm	-7.0	-4.0		dBm
	G4	P1 = P2 = -34dBm	-4.0	-1.0		dBm
	G3	P1 = P2 = -28dBm	-1.5	1.5		dBm
	G2	P1 = P2 = -22dBm	17.0	22.0		dBm
	G1	P1 = P2 = -16dBm	17.0	22.0		dBm
P1dB	G7		-18.5	-15.5		dBm
	G6		-15.0	-12.0		dBm
	G5		-13.0	-10.0		dBm
	G4		-10.5	-7.5		dBm
	G3		-10.0	-7.0		dBm
	G2		2.0	7.0		dBm
	G1		2.0	7.0		dBm
Input Return Loss	G1-G7		6.0	10.0		dB
Output Return Loss	G1-G7		6.0	10.0		dB
Reverse Isolation	G7	G7	27	32		dB
K	G1-G7		1.0			

MIPI RFFE Specification

The MIPI RFFE interface is working in systems following the MIPI Alliance Specification for RF Front-End Control Interface version 3.0.

TABLE1: MIPI FEATURES

Feature	Supported	Comment
MIPI RFFE 3.0 standard	Yes	
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Masked write command sequence	Yes	Indicated as MW in below register mapping tables
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz for read and write
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz for write
Half speed read	Yes	
Full speed read/Full speed write	Yes	
Longer Reach RFFE Bus Length Feature	Yes	
Programmable driver strength	Yes	
Programmable Group SID	Yes	
Programmable USID	Yes	
Trigger functionality	Yes	
Extended Triggers and Trigger Masks	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID select pin	Yes	

TABLE2: Start-up Behavior

Feature	State	Comment
Power status	Low power mode	Low power mode after start-up
Trigger function	Enable	Enable after start-up. Programmable via register

MIPI Read and Write Timing

Register 0 write:

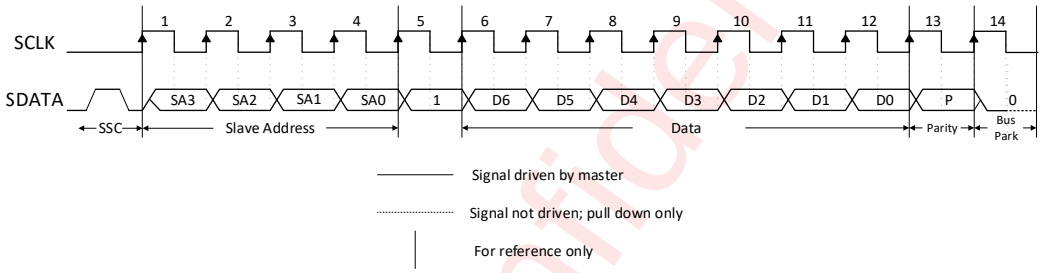


Figure 4 Register 0 write command sequence

Register write:

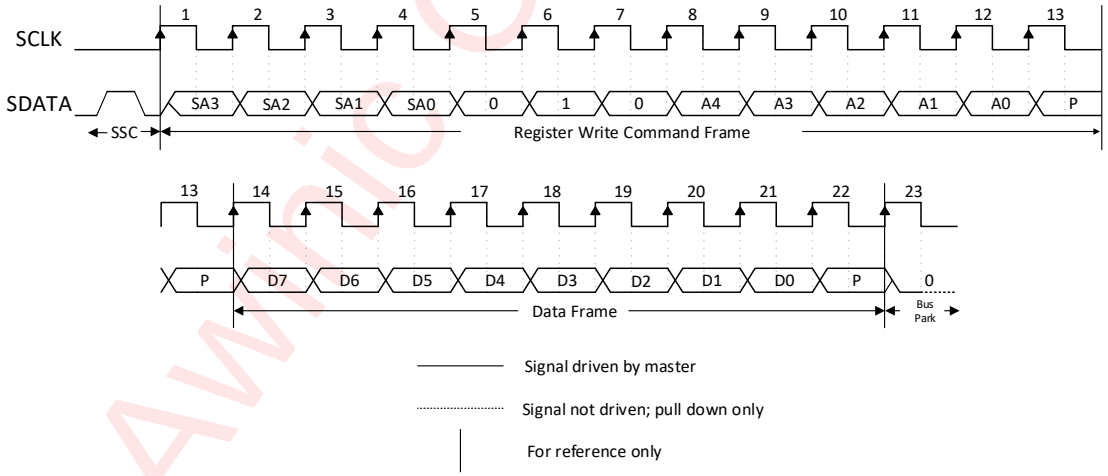


Figure 5 Register write command sequence

Register read:

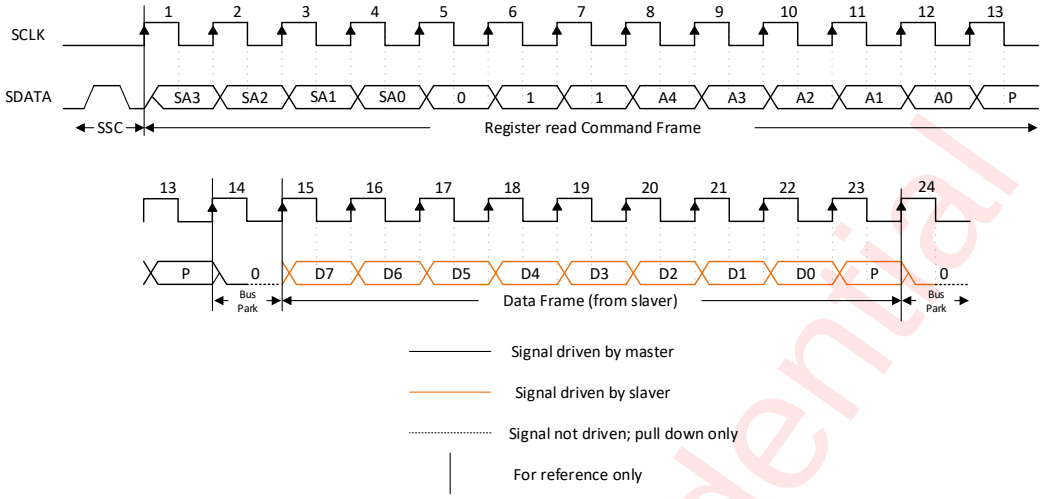


Figure 6 Register read command sequence

Extended Register write:

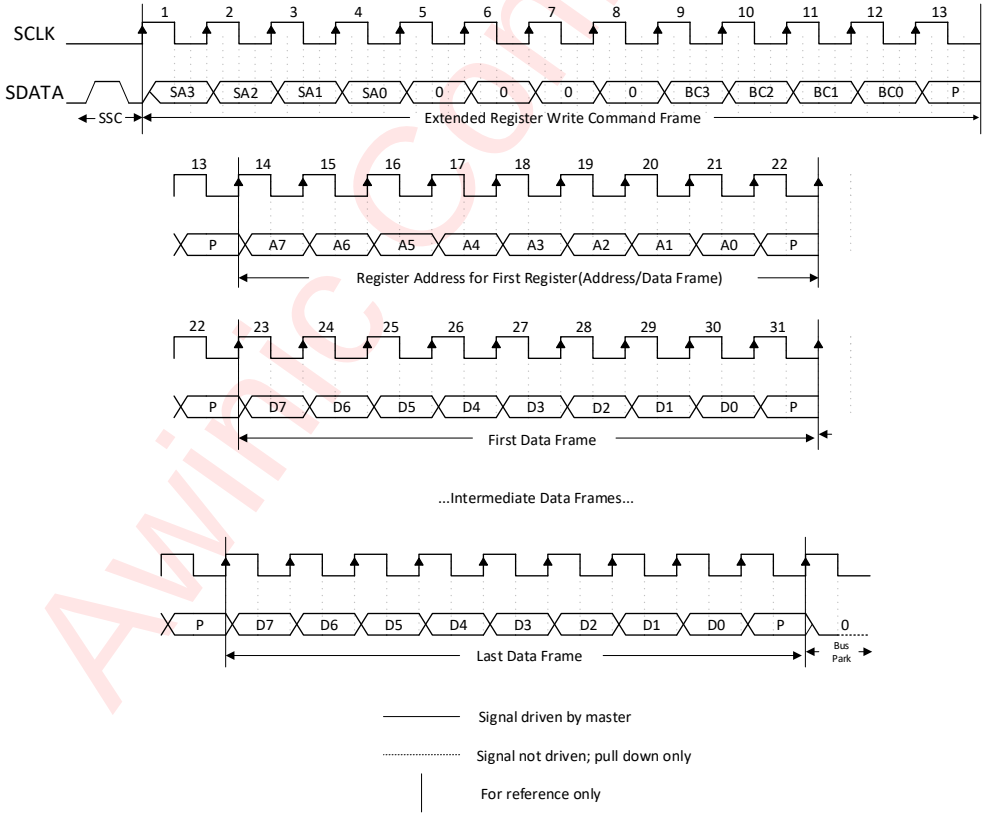


Figure 7 Extended Register write command sequence

Extended Register read:

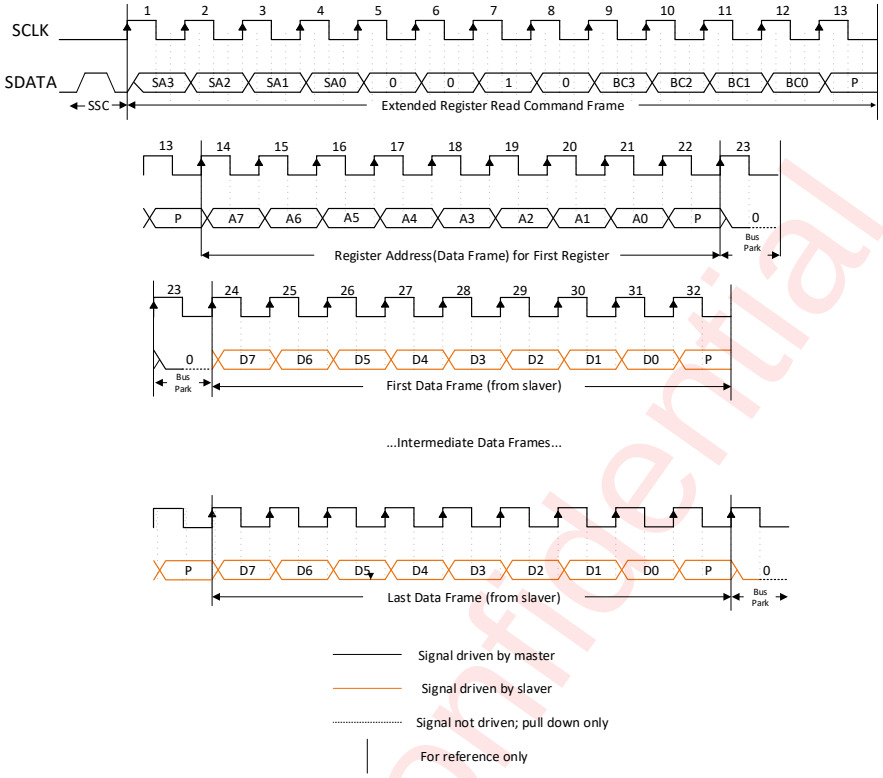


Figure 8 Extended Register read command sequence

Masked write:

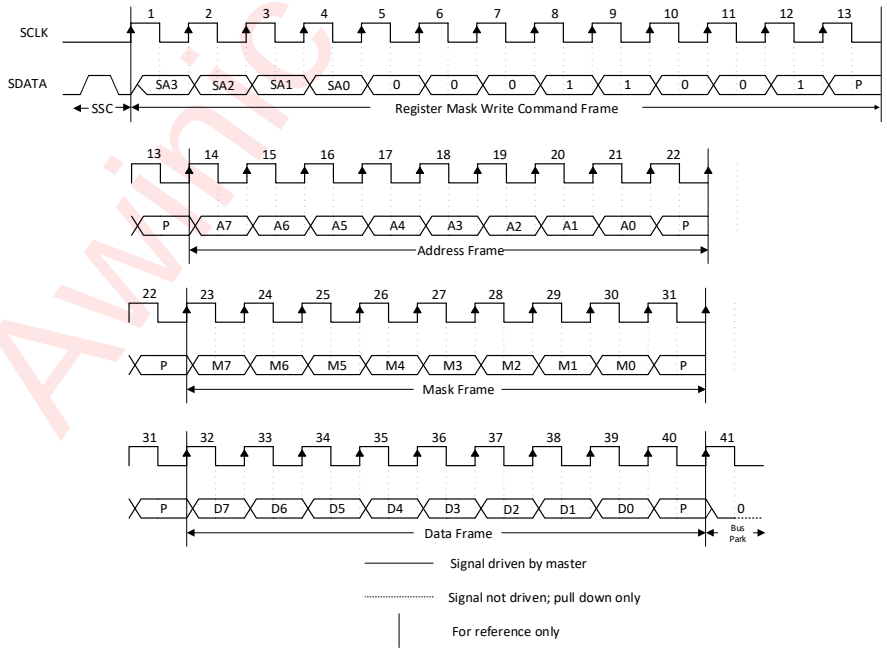


Figure 9 Masked Write Command Sequence

Register Configuration

Register Detailed Description

Reg Name	Address	Data Bits	Bits Name	Default	State	RW	Trigger Support
LNA Enable	0x0000	7:1	Reserved	000000	Reserved	RW MW	T1
		0	LNA Enable1	0	0：LNA Disable (LNA Enable2 must be 0 meanwhile) 1：LNA Enable		
LNA Gain Control	0x0001	7:5	Band Select	000	000：830~960MHz 110：700~830MHz 111：600~660MHz	RW MW	Extended TRIGGER UDR_SET_A
		4	LNA Enable2	0	0：LNA Disable (LNA Enable1 must be 0 meanwhile) 1：LNA Enable		
		3:0	LNA Gain Control	0000	0000：G7 0001：G6 0011：G5 0101：G4 0110：G3 1000：G2 1001：G1 other：Reserved		
UDR_SET_A CONTROL	0x0013	3:0	cTrig A define	0000	0b0000：UDR_SET_A used Extended Trigger 3 0b0001：UDR_SET_A used Extended Trigger 4 0b0010：UDR_SET_A used Extended Trigger 5 0b0011：UDR_SET_A used Extended Trigger 6 0b0100：UDR_SET_A used Extended Trigger 7 0b0101：UDR_SET_A	RW MW	NO

					used Extended Trigger 8 0b0110：UDR_SET_A used Extended Trigger 9 0b0111：UDR_SET_A used Extended Trigger 10 others：Trigger Masked		
PM_TRIG	0x001C	7	PWR_MODE [1], Operation Mode	1	1: Low Power Mode 0: Normal Operation Mode	RW	NO
		6	PWR_MODE [0], State bit Vector	0	0: No action (ACTIVE) 1: Powered Reset		
		5:3	TRIGGER_MASK_2/1/0	000	0: Data writes to registers tied to TRIGGER_2/1/0 is held in shadow registers until the TRIGGER_2/1/0 bit is set to 1. 1: Data writes to registers tied to TRIGGER_2 go directly to the active registers.		
		2:0	TRIGGER_2/1/0	000	0: No action. Data is held in shadow registers. 1: Data is transferred from shadow registers to active registers for registers tied to TRIGGER_2/1/0.		
PRODUCT_ID	0x001D	7:0	PRODUCT_ID [7:0]	0x1C	PRODUCT_ID<7:0>	R	NO
MANUFACTURER_ID	0x001E	7:0	MANUFACTURER_ID[7:0]	0x49	MANUFACTURER_ID <7:0>	R	NO
MAIN_USID	0x001F	7:4	MANUFACTURER_ID[11:8]	0000	MANUFACTURER_ID <11:8>	R	NO
		3:0	USID[3:0]	0x8	8： USID2=Grounded, USID1=Grounded	RW	NO

					9： USID2=Grounded, USID1=Float or VIO 10： USID2=Float or VIO, USID1=Grounded 11： USID2=Float or VIO, USID1=Float or VIO		
EXT_PRODUCT_ID	0x0020	7:0	EXT_PRODUCT_ID[7:0]	0x00	0x00	R	NO
REV_ID	0x0021	7:0	REVISION ID	0x01	0x01	R	NO
GROUP_SID	0x0022	7:4	GSID0[3:0]	0000	Bits 3:0 – Primary Group Slave ID[3:0]	R	NO
		3:0	GSID1[3:0]	0000	Bits 3:0 – Secondary Group Slave ID[3:0]	R	NO
UDR_RST	0x0023	7	UDR_RST	0	0: Normal Operation 1: Software Reset	RW	NO
BUS_LD	0X002B	0	BUS_LD	0	RFFE drive strength select. Programs the drive strength of the SDATA driver in readback modes 0: 50PF 1: 80PF	RW	NO
TEST_PATT	0x002C	7:0	TEST_PATT	0xD2		R	NO
EXT_TRIGGER_A_MASK	0x002D	7:0	EXT_TRIGGER_MASK_[10:3]	0x00	Bits 7 – Extended Trigger Masks 10 Bits 6 – Extended Trigger Masks 9 Bits 5 – Extended Trigger Masks 8 Bits 4 – Extended Trigger Masks 7 Bits 3 – Extended Trigger Masks 6 Bits 2 – Extended Trigger Masks 5 Bits 1 – Extended Trigger Masks 4 Bits 0 – Extended	RW	NO

					Trigger Masks 3 0: Mask Enable 1: Mask Disable		
EXT_TRIGGER_A	0x002E	7:0	EXT_TRIGGER_[10:3]	0x00	Bits 7 – Extended Trigger Register 10 Bits 6 – Extended Trigger Register 9 Bits 5 – Extended Trigger Register 8 Bits 4 – Extended Trigger Register 7 Bits 3 – Extended Trigger Register 6 Bits 2 – Extended Trigger Register 5 Bits 1 – Extended Trigger Register 4 Bits 0 – Extended Trigger Register 3 0: No action. 1: Action	RW	NO
EXT_TRIG_CNT3	0x0038	7:0	EXT_TRIG_CNT_3[8:1]	0x00	Bits 7:0 – Timed-Trigger Counter 3	RW	NO
EXT_TRIG_CNT4	0x0039	7:0	EXT_TRIG_CNT_4[8:1]	0x00	Bits 7:0 – Timed-Trigger Counter 4	RW	NO
EXT_TRIG_CNT5	0x003A	7:0	EXT_TRIG_CNT_5[8:1]	0x00	Bits 7:0 – Timed-Trigger Counter 5	RW	NO
EXT_TRIG_CNT6	0x003B	7:0	EXT_TRIG_CNT_6[8:1]	0x00	Bits 7:0 – Timed-Trigger Counter 6	RW	NO
EXT_TRIG_CNT7	0x003C	7:0	EXT_TRIG_CNT_7[8:1]	0x00	Bits 7:0 – Timed-Trigger Counter 7	RW	NO
EXT_TRIG_CNT8	0x003D	7:0	EXT_TRIG_CNT_8[8:1]	0x00	Bits 7:0 – Timed-Trigger Counter 8	RW	NO
EXT_TRIG_CNT9	0x003E	7:0	EXT_TRIG_CNT_9[8:1]	0x00	Bits 7:0 – Timed-Trigger Counter 9	RW	NO
EXT_TRIG_CNT10	0x003F	7:0	EXT_TRIG_CNT_10[8:1]	0x00	Bits 7:0 – Timed-Trigger Counter 10	RW	NO

Power On and Off Sequence

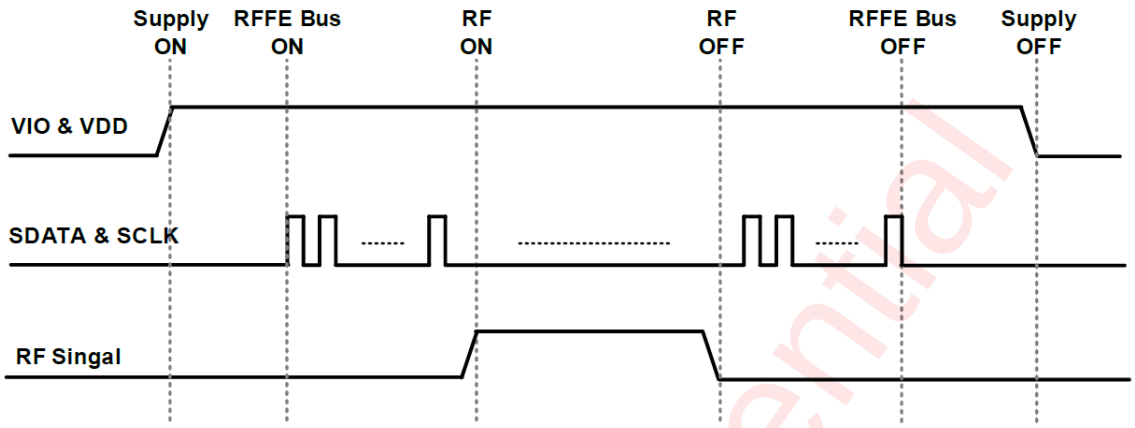


Figure 10 Power On and Power Off Sequence

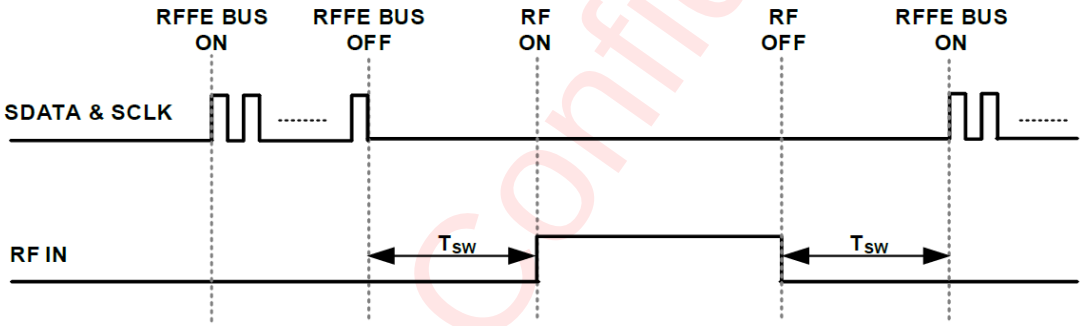


Figure 11 RF Power switching sequence

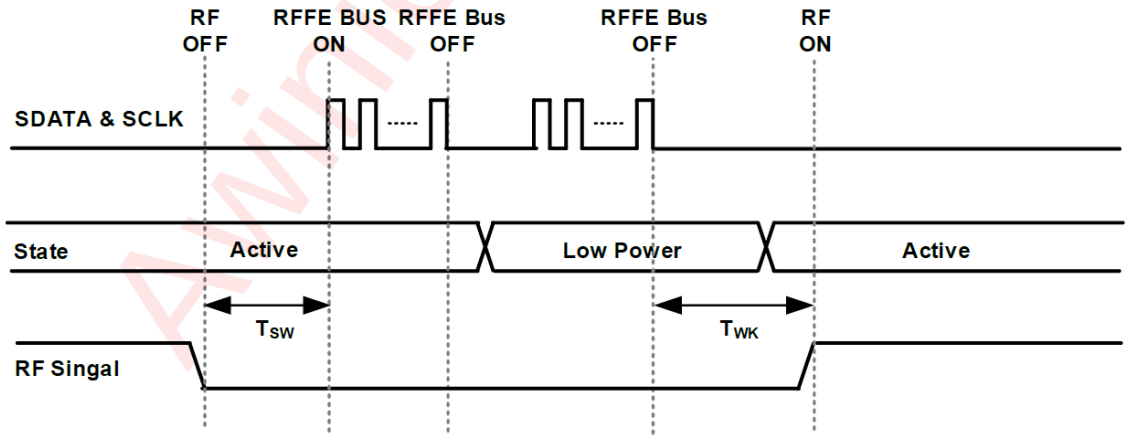
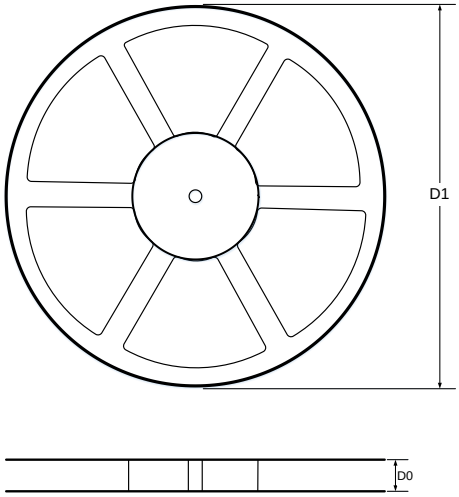


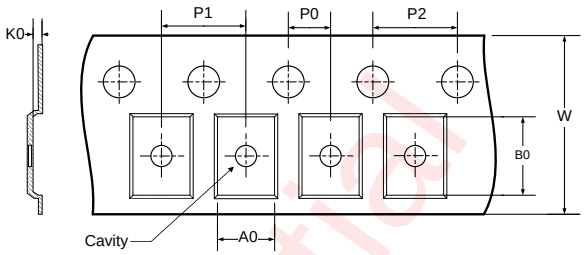
Figure 12 Enter and Exit Low Power State Sequences

Tape and Reel Information

REEL DIMENSIONS

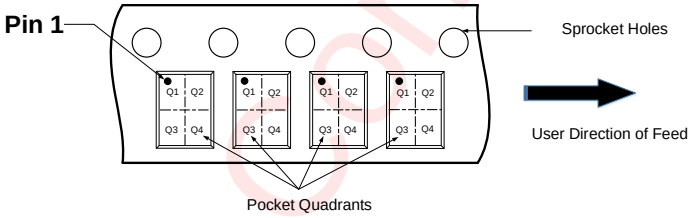


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: The above picture is for reference only. Please refer the value in the table below for actual size.

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.3	1.7	0.6	2	4	4	8	Q1

All dimensions are nominal

Figure 13 Tape and Reel

Package Description

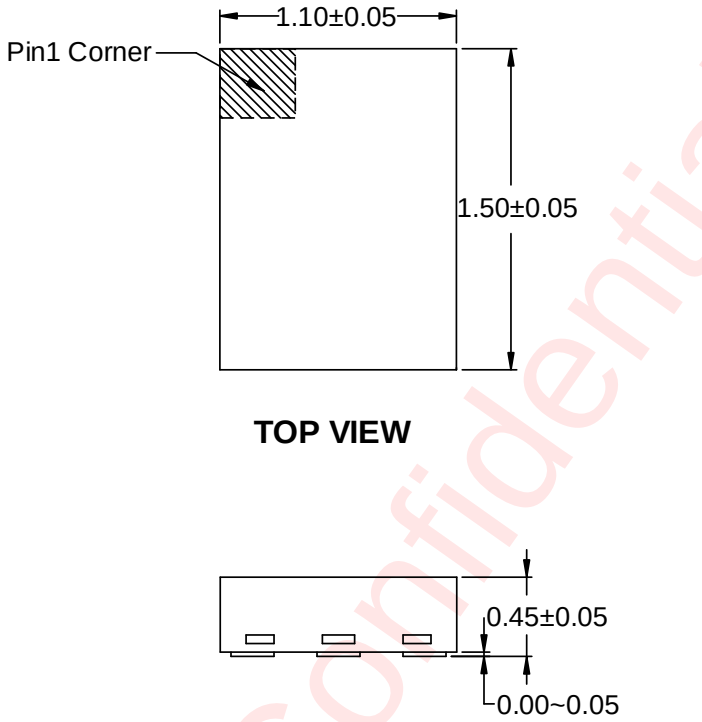


Figure 14 Package Outline

Land Pattern Data

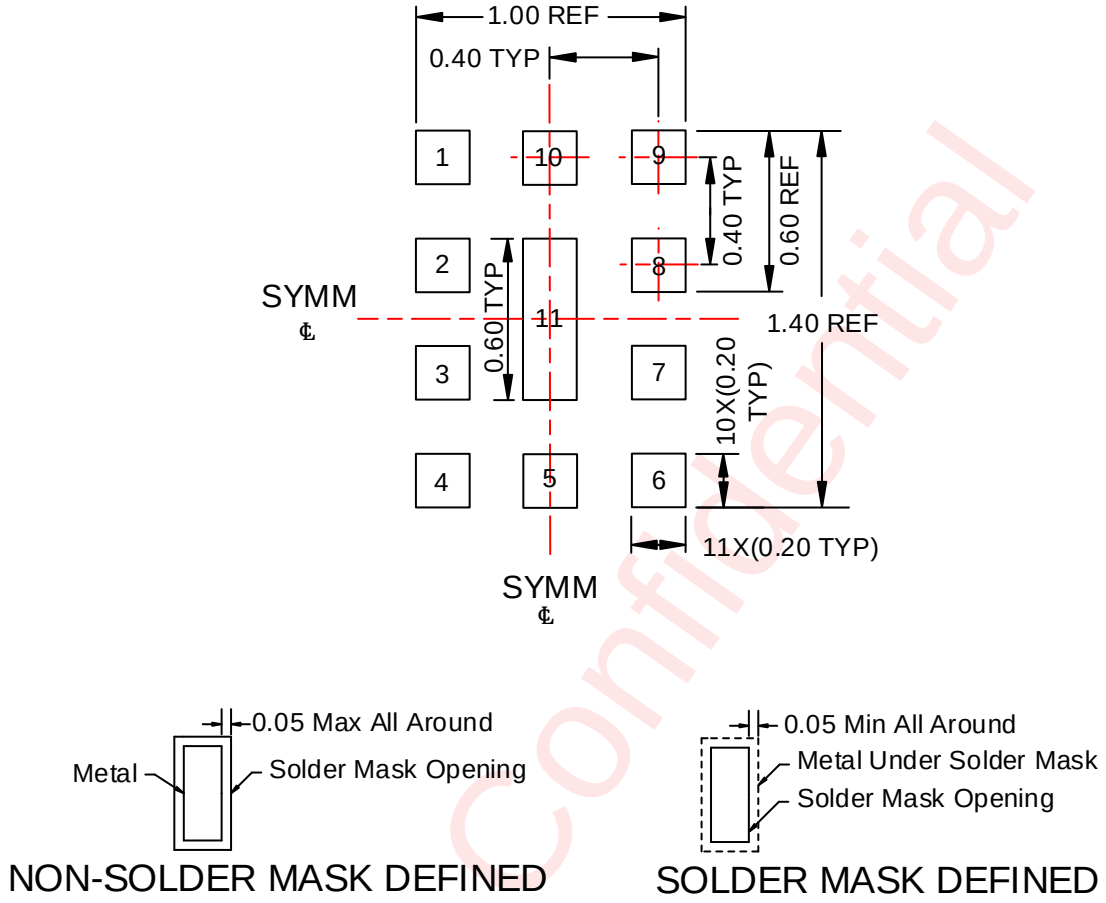


Figure 15 Land Pattern Data

Revision History

Version	Date	Change Record
V1.0	Jun. 2023	Officially Released
V1.1	Aug. 2023	Added RF Characteristics Limit
V1.2	Aug. 2025	Update Revision ID Register

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