

SP4T Switch with MIPI for 5G TRX

Features

- Broadband frequency range: 0.1 to 6.0 GHz
- Low insertion loss: 1.00dB typical @ 6GHz
- High isolation: 23dB typical @ 6GHz
- P0.1dB @ 38dBm
- MIPI RFFE V2.1 compatible Interface
- 50-Ohm termination enabling at isolation mode
- FCLGA 1.1mm X1.1mm X0.47mm-9L package

Applications

- Cellular 2G/3G/4G/5G TRX
- Cellular modems, tablets and USB Devices
- Other RF front-end modules

General Description

The AW13504TFLR is a SP4T switch with low insertion loss and high isolation. It can be used to support band switching for cellular 2G/3G/4G/5G, data cards and tablets.

The symmetrical design of internal ports makes it convenient for PCB routing and adjustment of receiving and transmitting signals. The band/mode switching is realized by the MIPI RFFE 2.1 Interface.

The AW13504TFLR is provided in a compact FCLGA 1.1mm X1.1mm X0.47mm-9L package.

Typical Application Circuit

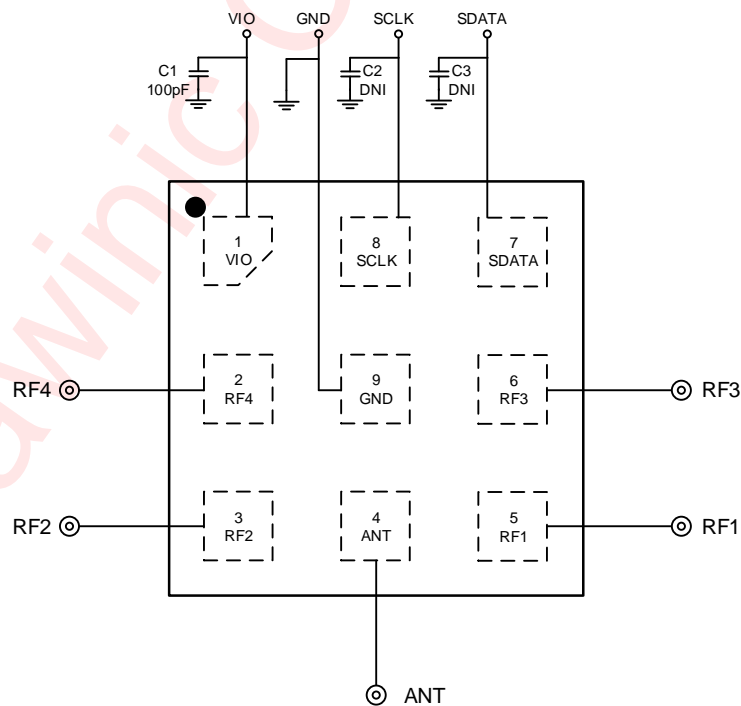


Figure 1 Typical Application Circuit

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Pin Configuration and Top Mark

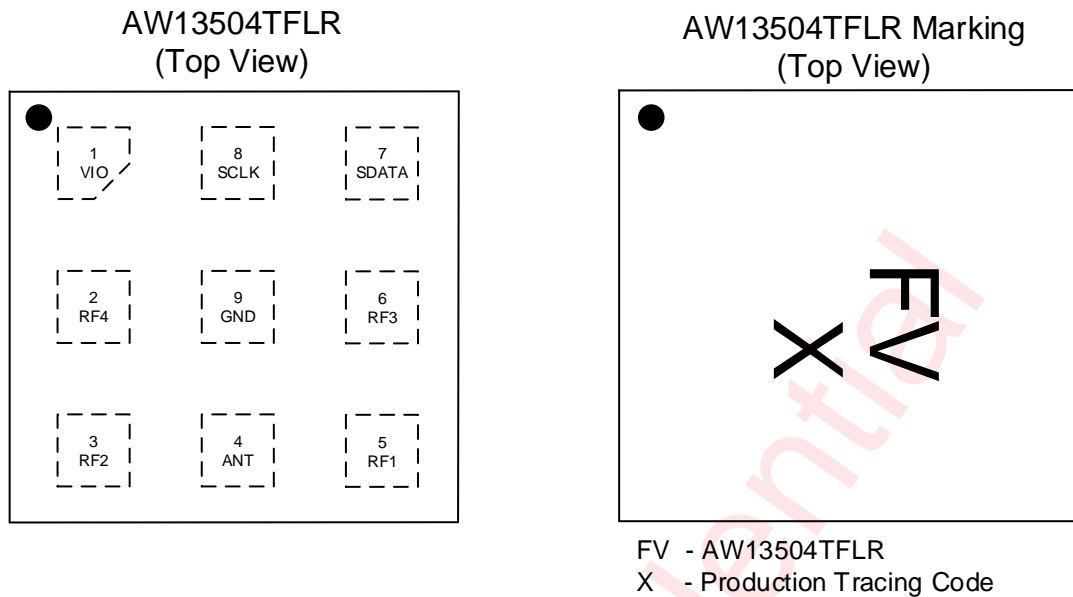


Figure 2 Pin Configuration and Top Mark

Pin Definition

| No. | NAME | DESCRIPTION |
|-----|-------|-------------------|
| 1 | VIO | Voltage Supply |
| 2 | RF4 | RF Port4 |
| 3 | RF2 | RF Port2 |
| 4 | ANT | Antenna |
| 5 | RF1 | RF Port1 |
| 6 | RF3 | RF Port3 |
| 7 | SDATA | RFFE Data Signal |
| 8 | SCLK | RFFE Clock Signal |
| 9 | GND | Ground |

Functional Block Diagram

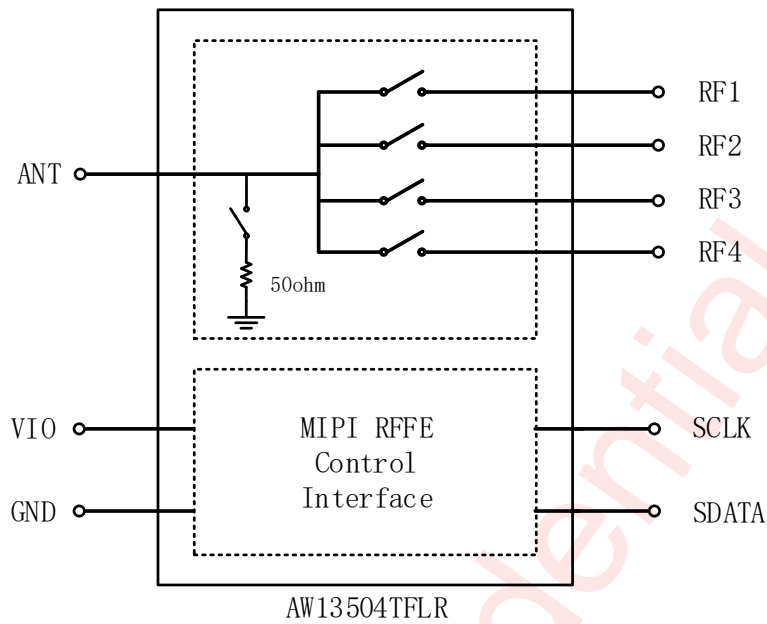


Figure 3 Functional Block Diagram

Ordering Information

| Part Number | Temperature | Package | Marking | Moisture Sensitivity Level | Environmental Information | Delivery Form |
|-------------|-------------|------------------------------------|---------|----------------------------|---------------------------|------------------------------|
| AW13504TFLR | -40°C~85°C | FCLGA 1.1mmX1.1mm X0.47mm-9L | FV | MSL3 | ROHS+HF | 4500 units/ Tape and Reel |

Absolute Maximum Ratings (NOTE1)

| PARAMETERS | RANGE |
|--------------------------------------|-----------------|
| Supply Voltage Range V_{IO} | -0.3V to +2.2 V |
| RRFFE Bus Voltage (SDATA, SCLK) | -0.3V to +2.2 V |
| Max input power(RF1/RF2/RF3/RF4/ANT) | 39dBm |
| Operating Free-air Temperature Range | -40°C to 85°C |
| Storage Temperature T_{STG} | -65°C to 150°C |
| ESD <small>(NOTE 2)</small> | |
| HBM | ±1000V |
| CDM | ±500V |

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017. CDM test method is ESDA/JEDEC JS-002-2018.

Electrical Characteristics

$V_{IO}=1.8V$, $P_{IN}=0dBm$, $Temp=+25^{\circ}C$, $Z_0=50\Omega$. Unless otherwise noted

| PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT | |
|--------------------------|--|---|--------------|----------|--------------|---------|
| DC Specifications | | | | | | |
| V_{IO} | Supply Voltage | 1.65 | 1.8 | 1.95 | V | |
| I_{IO} | Supply Current | Active Mode | - | 50 | 100 | μA |
| | | Low Power Mode | - | 2 | 10 | μA |
| V_{IH} | SDATA,SCLK Control Voltage High | Must not exceed V_{IO} voltage | $0.8*V_{IO}$ | V_{IO} | 1.95 | V |
| V_{IL} | SDATA,SCLK Control Voltage Low | Must not exceed V_{IO} voltage | 0 | 0 | $0.2*V_{IO}$ | V |
| T_{ON} | Wakeup Time | From end of Low Power State 50% SCLK to 90% of final RF amplitude | - | 2.5 | 5 | μs |
| T_{SW} | Switching Time One RF port to another | From end of RFFE Sequence to 90% of final RF amplitude | - | 1.3 | 2 | μs |
| RF Specifications | | | | | | |
| IL | Insertion loss (ANT to RFx) | 617-960MHz | - | 0.35 | - | dB |
| | | 960-2170 MHz | - | 0.49 | - | dB |
| | | 2170-2700 MHz | - | 0.60 | - | dB |
| | | 3300-4200 MHz | - | 0.65 | - | dB |
| | | 4400-5000 MHz | - | 0.69 | - | dB |
| | | 5150-5925 MHz | - | 1.00 | - | dB |
| ISO | Isolation (ANT_RF1 vs RFx) | 617-960MHz | - | 47 | - | dB |
| | | 960-2170 MHz | - | 38 | - | dB |
| | | 2170-2700 MHz | - | 36 | - | dB |
| | | 3300-4200 MHz | - | 30 | - | dB |
| | | 4400-5000 MHz | - | 26 | - | dB |
| | | 5150-5925 MHz | - | 25 | - | dB |
| ISO | Isolation (ANT_RF2 vs RFx) | 617-960MHz | - | 47 | - | dB |
| | | 960-2170 MHz | - | 37 | - | dB |
| | | 2170-2700 MHz | - | 35 | - | dB |
| | | 3300-4200 MHz | - | 30 | - | dB |
| | | 4400-5000 MHz | - | 28 | - | dB |
| | | 5150-5925 MHz | - | 26 | - | dB |
| ISO | Isolation (ANT_RF3 vs RFx) | 617-960MHz | - | 47 | - | dB |
| | | 960-2170 MHz | - | 36 | - | dB |
| | | 2170-2700 MHz | - | 34 | - | dB |
| | | 3300-4200 MHz | - | 27 | - | dB |
| | | 4400-5000 MHz | - | 25 | - | dB |
| | | 5150-5925 MHz | - | 23 | - | dB |

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|--------------------|--------------------------------------|------------------------|-----|-----|-----|------|
| ISO | Isolation (ANT_RF4 vs RFx) | 617-960MHz | - | 45 | - | dB |
| | | 960-2170 MHz | | 36 | | dB |
| | | 2170-2700 MHz | | 33 | | dB |
| | | 3300-4200 MHz | | 27 | | dB |
| | | 4400-5000 MHz | | 24 | | dB |
| | | 5150-5925 MHz | | 23 | | dB |
| RL | Return Loss (ANT/RF1/RF2/RF3/RF4) | 617-960MHz | - | 30 | - | dB |
| | | 960-2170 MHz | | 18 | | dB |
| | | 2170-2700 MHz | | 17 | | dB |
| | | 3300-4200 MHz | | 15 | | dB |
| | | 4400-5000 MHz | | 13 | | dB |
| | | 5150-5925 MHz | | 10 | | dB |
| 2fo | Second harmonics | PIN=+26dBm, 900MHz | - | -85 | - | dBm |
| | | PIN=+35dBm, 900MHz | - | -65 | - | dBm |
| | | PIN=+26dBm, 1900MHz | - | -90 | - | dBm |
| | | PIN=+33dBm, 1900MHz | - | -77 | - | dBm |
| 3fo | Third harmonics | PIN=+26dBm, 900MHz | - | -82 | - | dBm |
| | | PIN=+35dBm, 900MHz | - | -55 | - | dBm |
| | | PIN=+26dBm, 1900MHz | - | -80 | - | dBm |
| | | PIN=+33dBm, 1900MHz | - | -62 | - | dBm |
| P _{0.1dB} | 0.1dB Compression Point | 900MHz, CW VSWR=1:1 | - | 38 | - | dBm |

Timing Requirements

- Once V_{IO} is powered down to 0 V, wait at least 10 μs to reapply power to V_{IO} .

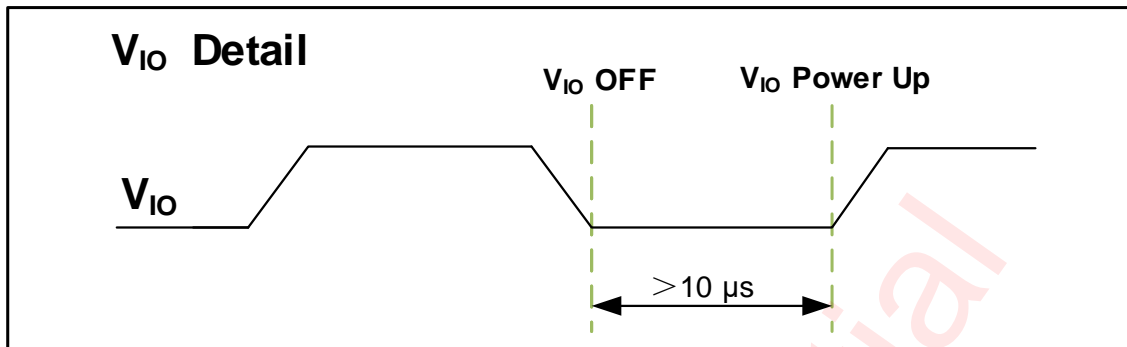


Figure 4 Digital Supply Detail

- Before applying RF power, V_{IO} must be turned on for at least 20 μs .

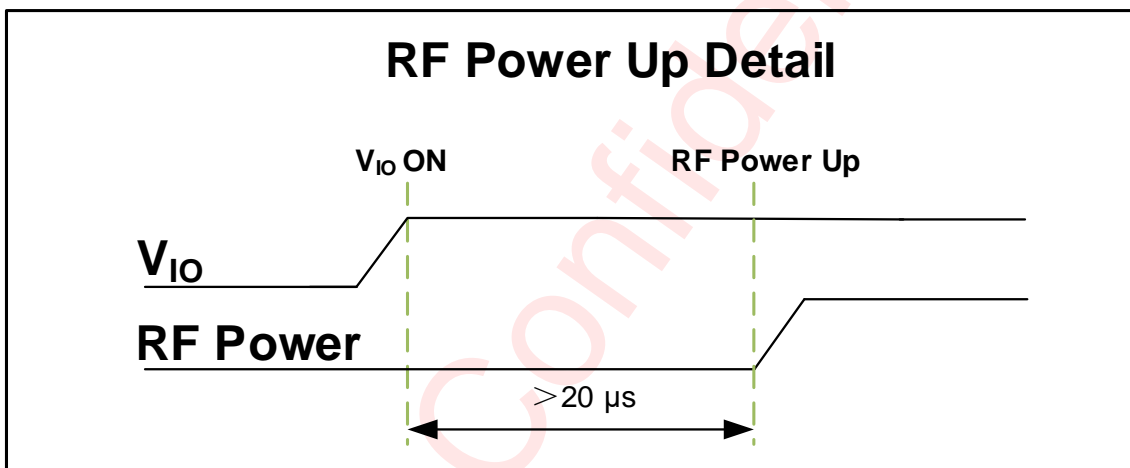


Figure 5 RF Power-Up Detail

- Before sending SDATA/SCLK, V_{IO} must be applied for at least 800 ns to ensure correct data transmission. And after the RFFE bus is idle, wait at least 20 μs to apply the RF signal.

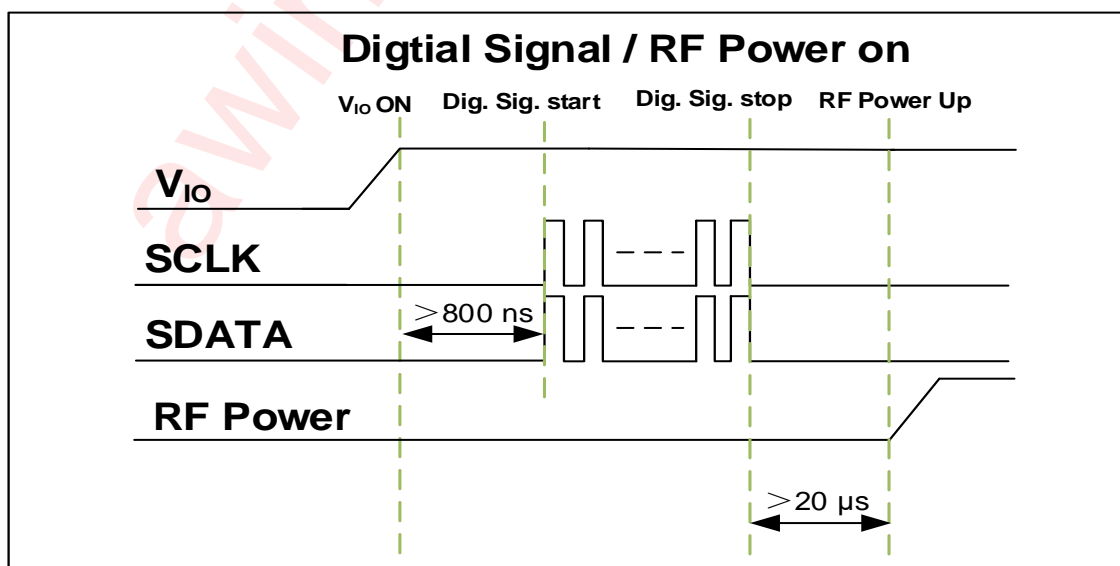


Figure 6 Digital Signal / RF Power-On Detail

4. There shall be no RFFE bus operations during RF Signal active to protect the device. So RF input signal shall be applied after RFFE bus operations being finished and be removed before RFFE bus operations being started.

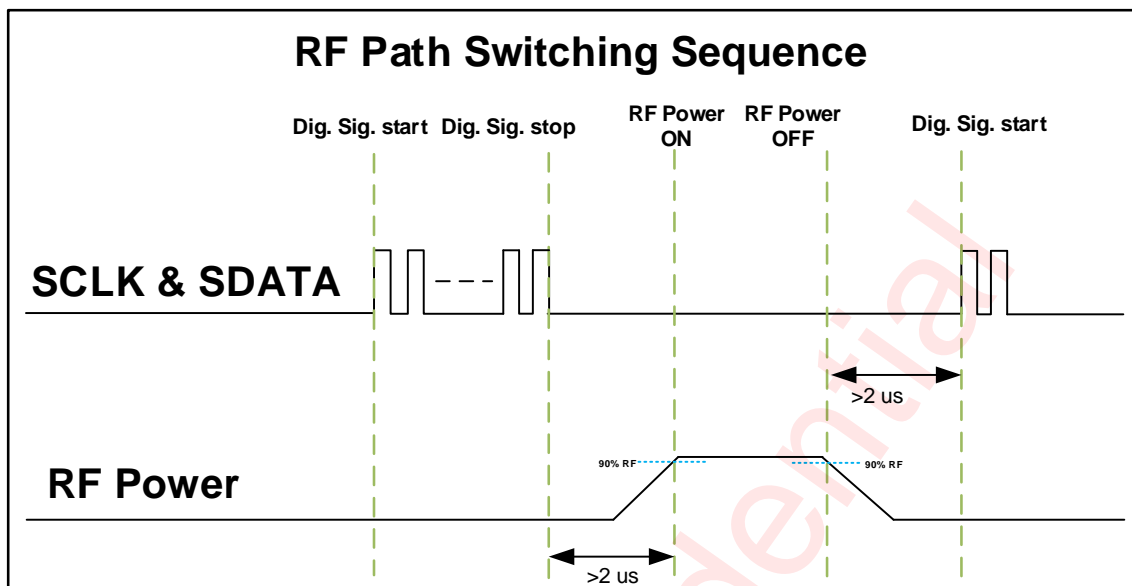


Figure 7 RF Path Switching Sequence

5. If "Lower Power Mode" is used, there must be a 10 μs delay before exiting "Lower Power Mode".

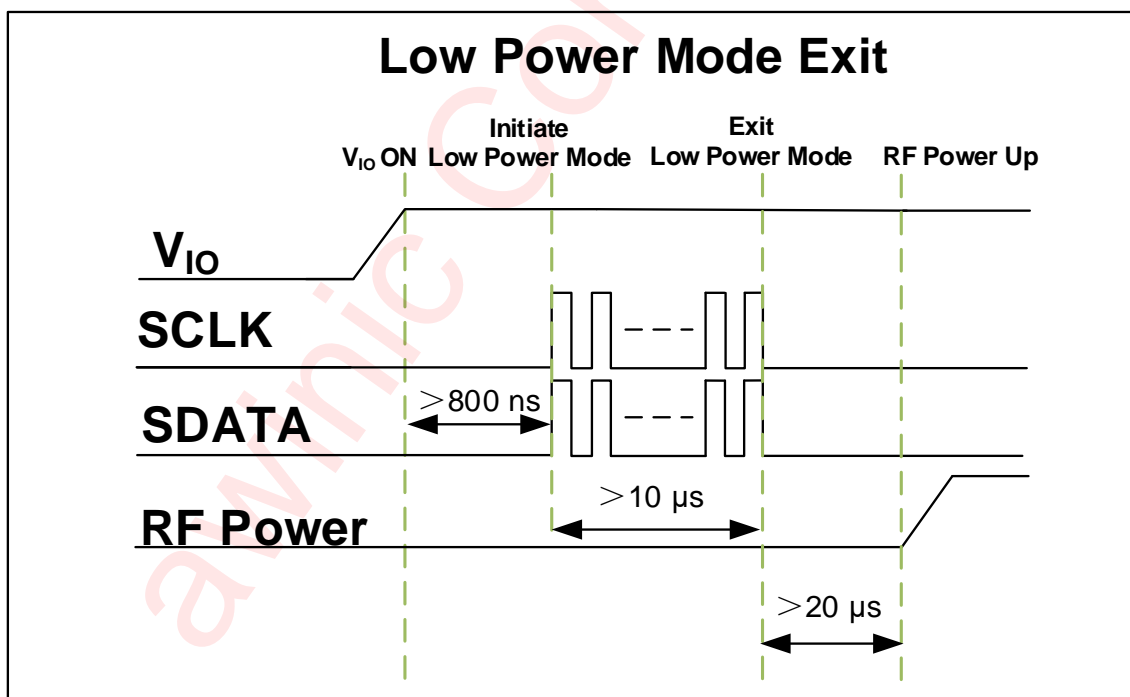


Figure 8 Lower Power Mode Exit Timing

MIPI RFFE Specification

The MIPI RFFE interface is working in systems following the MIPI Alliance Specification for RF Front-End Control Interface version 2.1.

TABLE1: MIPI FEATURES

| Feature | Supported | Comment |
|--|-----------|--|
| MIPI RFFE 2.1 standard | Yes | |
| Register 0 write command sequence | Yes | |
| Register read and write command sequence | Yes | |
| Extended register read and write command sequence | Yes | |
| Masked write command sequence | Yes | Indicated as MW in below register mapping tables |
| Support for standard frequency range operations for SCLK | Yes | Up to 26 MHz for read and write |
| Support for extended frequency range operations for SCLK | Yes | Up to 52 MHz for write |
| Half speed read | Yes | |
| Full speed read/Full speed write | Yes | |
| Longer Reach RFFE Bus Length Feature | Yes | |
| Programmable driver strength | Yes | |
| Programmable Group SID | Yes | |
| Programmable USID | Yes | Support for three registers write and extended write sequences |
| Trigger functionality | Yes | |
| Extended Triggers and Trigger Masks | Yes | |
| Broadcast / GSID write to PM TRIG register | Yes | |
| Reset | Yes | Via VIO, PM TRIG or software register |
| Status / error sum register | Yes | |
| Extended product ID register | Yes | |
| Revision ID register | Yes | |
| Group SID register | Yes | |
| USID select pin | No | |

TABLE2: Start-up Behavior

| Feature | State | Comment |
|------------------|----------------|--|
| Power status | Low power mode | Low power mode after start-up |
| Trigger function | Enable | Enable after start-up. Programmable via register |

MIPI Read and Write Timing

Register 0 write:

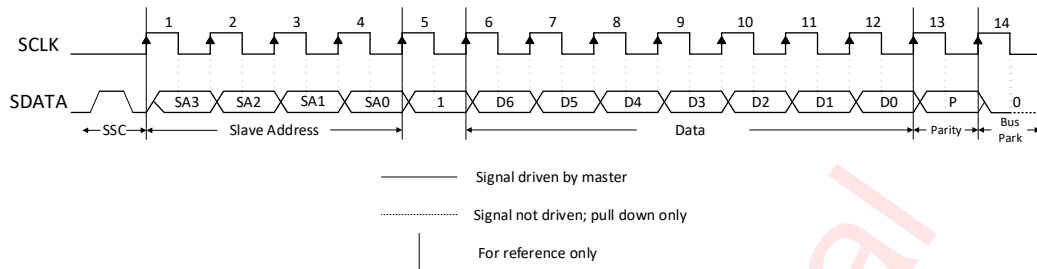


Figure 9 Register 0 Write Command Sequence

Register write:

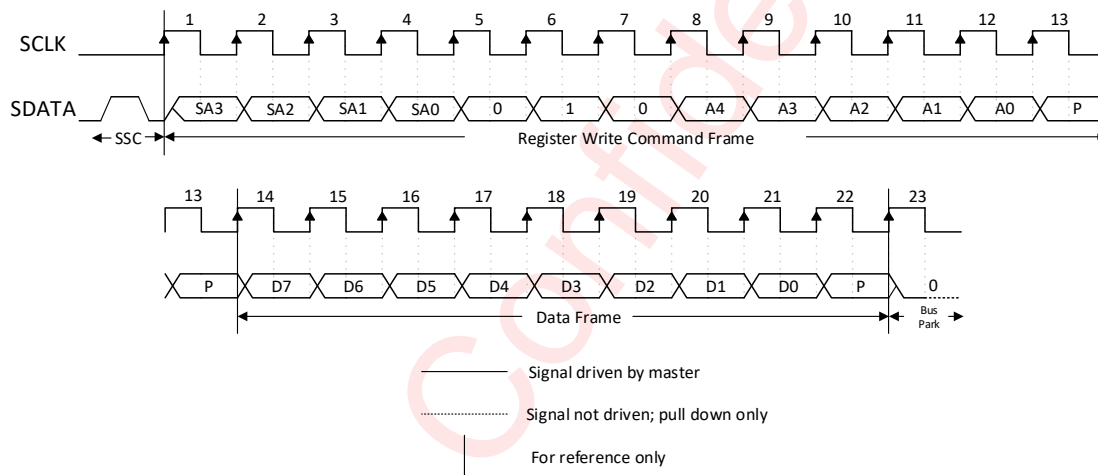


Figure 10 Register Write Command Sequence

Register read:

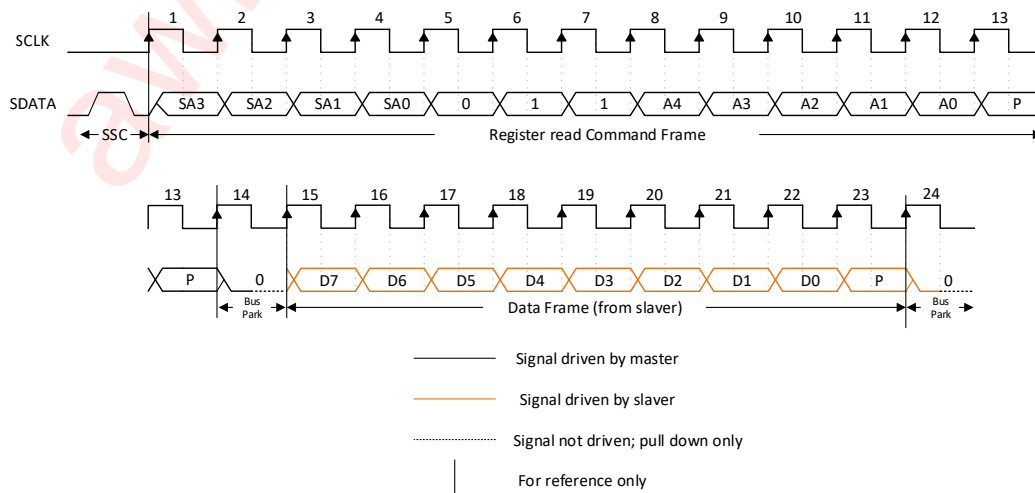


Figure 11 Register Read Command Sequence

Extended Register write:

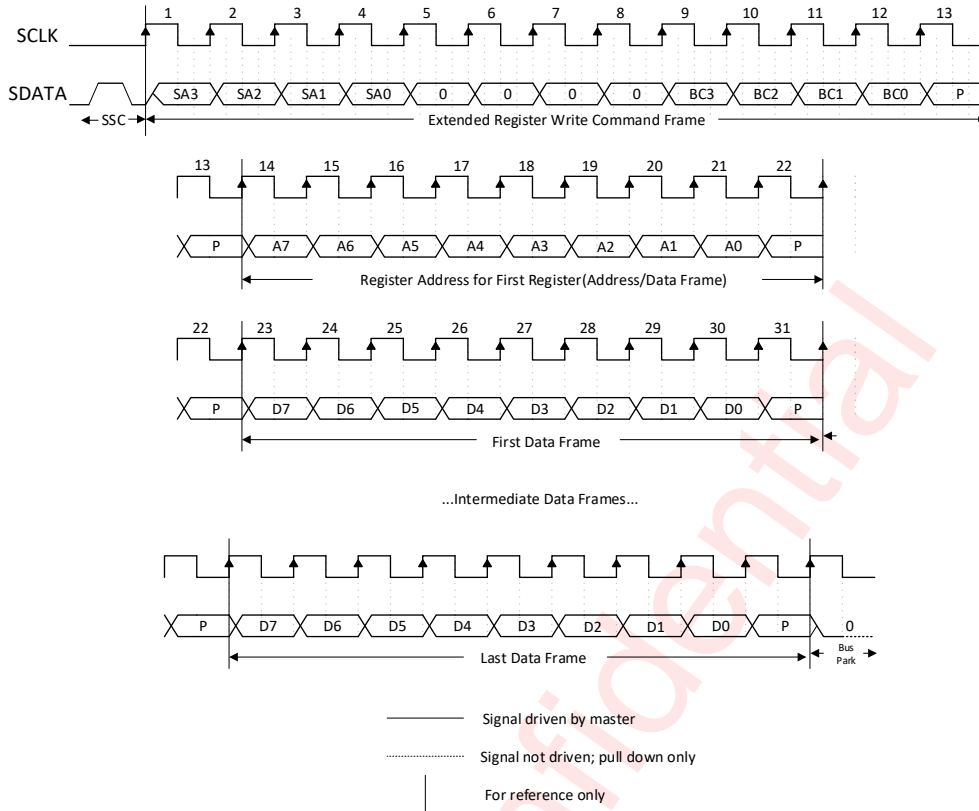


Figure 12 Extended Register Write Command Sequence

Extended Register read:

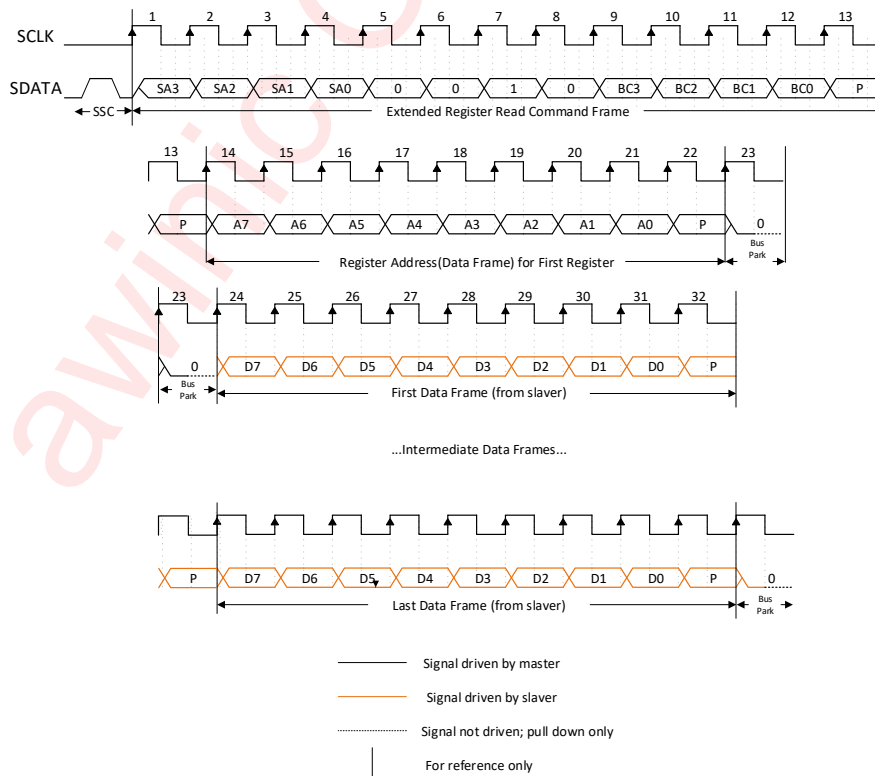


Figure 13 Extended Register Read Command Sequence

Masked write:

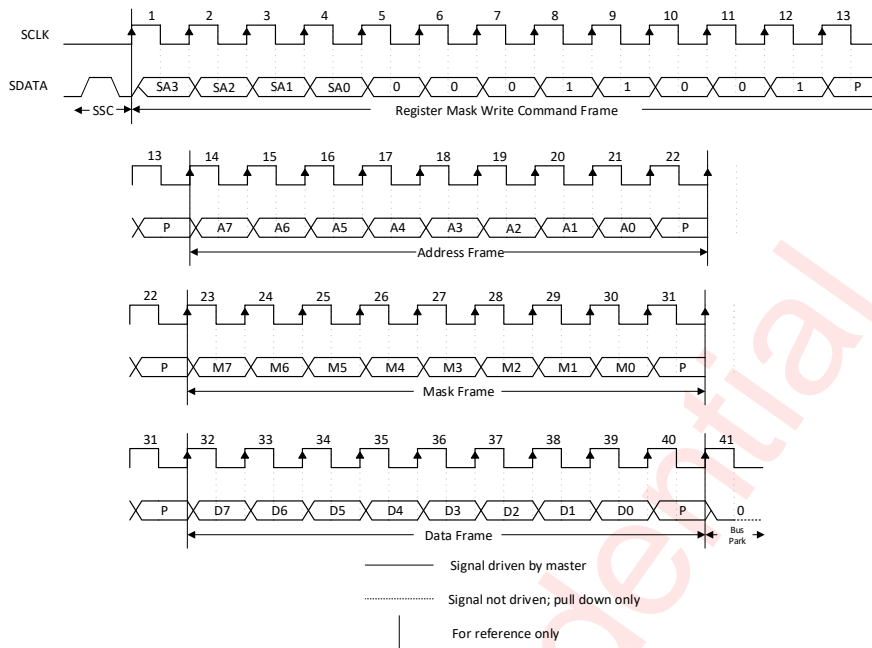


Figure 14 Masked Write Command Sequence

Register Configuration

Register Detailed Description

REGISTER_0 : Mode Control Register(Address 0000h)

| Bit | Symbol | Description | R/W | B/G | Trig | Default |
|-----|-----------|--|----------|-----|-------------|---------|
| 7:0 | MODE_CTRL | 00000000: Isolation (ALL OFF) xxxxxxx1: RF1 on xxxxxx1x: RF2 on xxxxx1xx: RF3 on xxxx1xxx: RF4 on xxx1xxxx: ANT connected to a 50Ω (x—either 0 or 1) | RW MW | No | Yes 0-10 | 0x00 |

RFFE_STATUS : RFFE Status Register(Address 001Ah)

| Bit | Symbol | Description | R/W | B/G | Trig | Default |
|-----|---------------|---|-----|-----|------|---------|
| 7 | UDR_RST | Reset all configurable non-RFFE reserved register to default values 0: normal operation 1: software reset | W | No | No | 0 |
| 6 | CMD_FR_P_ERR | Command Frame received with a parity error | RW | No | No | 0 |
| 5 | CMD_LEN_ERR | Command Sequence received with an incorrect length | RW | No | No | 0 |
| 4 | ADDR_FR_P_ERR | Address Frame received with a parity error | RW | No | No | 0 |
| 3 | DATA_FR_P_ERR | Data Frame received with a parity error | RW | No | No | 0 |
| 2 | RD_INVLD_ADDR | Read Command Sequence received with an invalid address | RW | No | No | 0 |
| 1 | WR_INVLD_ADDR | Write Command Sequence received with an invalid address | RW | No | No | 0 |
| 0 | BID_GID_ERR | Read Command Sequence received with a BSID or GSID | RW | No | No | 0 |

GSID0_1 : Group ID 0-1 Register(Address 001Bh)

| Bit | Symbol | Description | R/W | B/G | Trig | Default |
|-----|--------|-----------------|-----|-----|------|---------|
| 7:4 | GSID0 | Group Slave ID0 | RW | No | No | 0000 |
| 3:0 | GSID1 | Group Slave ID1 | RW | No | No | 0000 |

PM_TRIG : Pwr_mode and Trig Register(Address 001Ch)

| Bit | Symbol | Description | R/W | B/G | Trig | Default |
|-----|-------------------|--|-----|-----|------|---------|
| 7 | PWR_MODE[1] | 0: Normal Operation 1: Low Power - Antenna in isolation | RW | Yes | No | 1 |
| 6 | PWR_MODE[0] | 0: active 1: start up – Reset all register to default | RW | Yes | No | 0 |
| 5:3 | Trigger Mask[2:0] | Setting bit Trigger Mask[N] disables Trigger[N] Trigger Mask[N] updates before Trigger[N] is processed <i>Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register. If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.</i> | RW | No | No | 000 |
| 2:0 | Trigger[2:0] | Setting bit Trigger[N] loads Trigger[N]'s associated registers <i>Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[0], [1], and [2] will always read as 0.</i> | W | Yes | No | 000 |

PRODUCT_ID : Product ID Register(Address 001Dh)

| Bit | Symbol | Description | R/W | B/G | Trig | Default |
|-----|---------|--------------------------------|-----|-----|------|---------|
| 7:0 | PROD_ID | Lower eight bits of Product ID | R | No | No | 0x08 |

MANUFACTURER_ID : Manufacture ID Register(Address 001Eh)

| Bit | Symbol | Description | R/W | B/G | Trig | Default |
|-----|--------|-------------------------------------|-----|-----|------|---------|
| 7:0 | MFG_ID | Lower eight bits of Manufacturer ID | R | No | No | 0x49 |

MAN_USID : User ID Register(Address 001Fh)

| Bit | Symbol | Description | R/W | B/G | Trig | Default |
|-----|--------|------------------------------------|-----|-----|------|---------|
| 7:4 | MFG_ID | Upper four bits of Manufacturer ID | R | No | No | 0000 |
| 3:0 | USID | Unique Slave ID | RW | No | No | 1000 |

EXT_PRODUCT_ID : Extend Product ID Register(Address 0020h)

| Bit | Symbol | Description | R/W | B/G | Trig | Default |
|-----|---------|--------------------------------|-----|-----|------|---------|
| 7:0 | PROD_ID | Upper eight bits of Product ID | R | No | No | 0x00 |

GSID2_3 : Group ID 2-3 Register(Address 0022h)

| Bit | Symbol | Description | R/W | B/G | Trig | Default |
|-----|--------|-----------------|-----|-----|------|---------|
| 7:4 | GSID2 | Group Slave ID2 | R/W | No | No | 0000 |
| 3:0 | GSID3 | Group Slave ID3 | R/W | No | No | 0000 |

UDR_RST : UDR Reset Register(Address 0023h)

| Bit | Symbol | Description | R/W | B/G | Trig | Default |
|-----|----------|---|-----|-----|------|---------|
| 7 | UDR_RST | Reset all configurable non-RFFE reserved register to default values 0: normal 1: software reset | R/W | Yes | No | 0 |
| 6:0 | RESERVED | Reserved | R/W | No | No | 0x00 |

ERR_SUM : Error Command Status Register(Address 0024h)

| Bit | Symbol | Description | R/W | B/G | Trig | Default |
|-----|---------------|---|-----|-----|------|---------|
| 7 | SPARE | Reserved for future use | R/W | No | No | 0 |
| 6 | COM_FR_P_ERR | Command Frame received with a parity error | R/W | No | No | 0 |
| 5 | COM_LEN_ERR | Command Sequence received with an incorrect length | R/W | No | No | 0 |
| 4 | ADDR_FR_P_ERR | Address Frame received with a parity error | R/W | No | No | 0 |
| 3 | DATA_FR_P_ERR | Data Frame received with a parity error | R/W | No | No | 0 |
| 2 | RD_INVLD_ADDR | Read Command Sequence received with an invalid address | R/W | No | No | 0 |
| 1 | WR_INVLD_ADDR | Write Command Sequence received with an invalid address | R/W | No | No | 0 |
| 0 | BID_GID_ERR | Read Command Sequence received with a BSID or GSID | R/W | No | No | 0 |

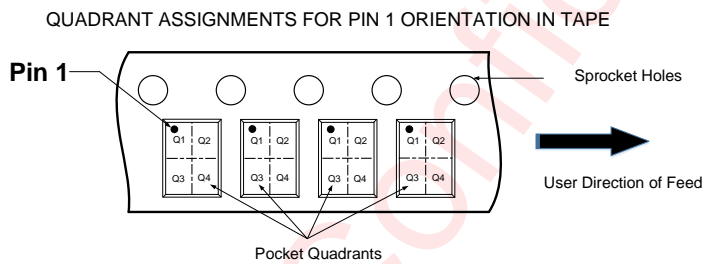
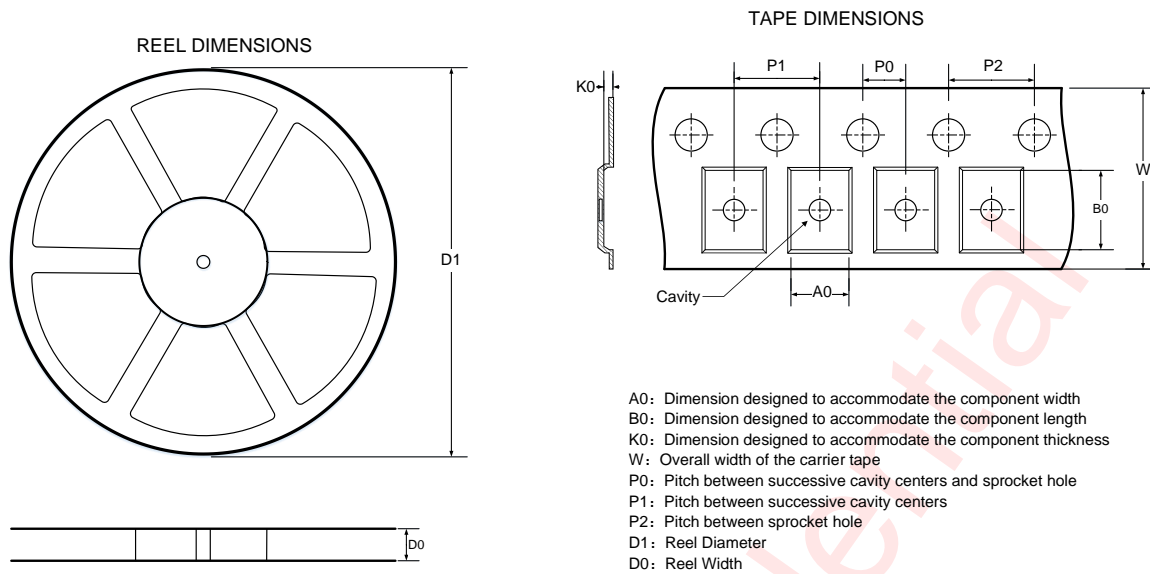
EXT_TRIG_MASK : Extend Trig Mask Register(Address 002Dh)

| Bit | Symbol | Description | R/W | B/G | Trig | Default |
|-----|--------------------|--|-----|-----|------|---------|
| 7:0 | Trigger Mask[10:3] | <p>Setting bit Trigger Mask[N] disables Trigger[N]</p> <p>If using an Extended Write to update both Trigger Mask and Trigger, than Trigger Mask[N] updates before Trigger[N] is processed</p> <p><i>Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register. If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.</i></p> | RW | No | No | 0xFF |

EXT_TRIG : Extend Trig Register(Address 002Eh)

| Bit | Symbol | Description | R/W | B/G | Trig | Default |
|-----|---------------|--|-----|-----|------|---------|
| 7:0 | Trigger[10:3] | <p>Setting bit Trigger[N] loads Trigger[N]'s associated registers</p> <p><i>Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[10 - 3] will always read as 0.</i></p> | W | Yes | No | 0x00 |

Tape and Reel Information



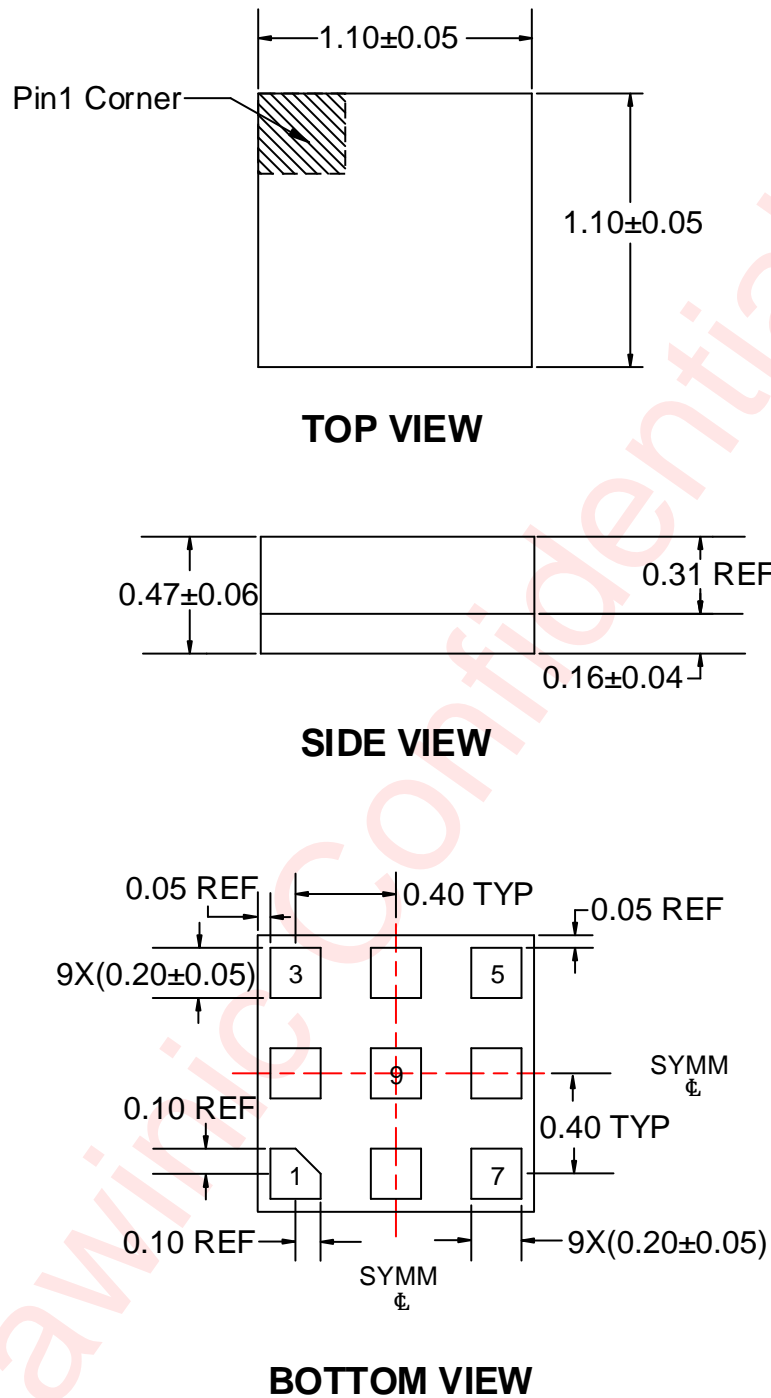
DIMENSIONS AND PIN 1 ORIENTATION

| D1 (mm) | D0 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---------|---------|---------|---------|---------|---------|---------|---------|--------|---------------|
| 180 | 8.4 | 1.25 | 1.25 | 0.6 | 2 | 4 | 4 | 8 | Q1 |

All dimensions are nominal

Figure 15 Tape and Reel

Package outline dimensions



Unit:mm

Figure 16 Package Outline

Revision History

| Version | Date | Change Record |
|---------|-----------|---------------------|
| V1.0 | Apr. 2022 | Officially Released |

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