

N-Channel Enhancement Mode Power MOSFET

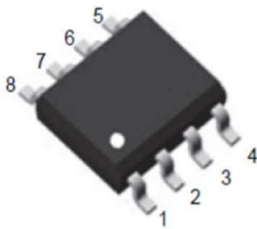
Features

- $V_{DS} = 40V$, $I_D = 14 A$
 $R_{DS(ON)} < 10 m\Omega @ V_{GS} = 10V$
 $R_{DS(ON)} < 17 m\Omega @ V_{GS} = 4.5V$

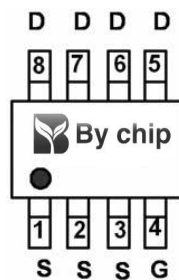
General Features

- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free and Green Available

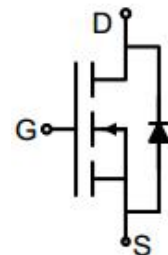
100% UIS TESTED!
 100% ΔV_{ds} TESTED!



SOP-8



pin assignment



Schematic diagram

Maximum ratings, at $T_A = 25^\circ C$, unless otherwise specified

| Symbol | Parameter | Rating | Unit |
|----------------|---|---------------------|------------|
| $V_{(BR)DSS}$ | Drain-Source breakdown voltage | 40 | V |
| V_{GS} | Gate-Source voltage | ± 20 | V |
| I_S | Diode continuous forward current | $T_A = 25^\circ C$ | 3.8 A |
| I_D | Continuous drain current @ $V_{GS} = 10V$ | $T_A = 25^\circ C$ | 14 A |
| | | $T_A = 100^\circ C$ | 9 A |
| I_{DM} | Pulse drain current tested ① | $T_A = 25^\circ C$ | 56 A |
| P_D | Maximum power dissipation | $T_A = 25^\circ C$ | 3.1 W |
| MSL | | Level 3 | |
| T_{STG}, T_J | Storage and junction temperature range | -55 to 150 | $^\circ C$ |

Thermal Characteristics

| Symbol | Parameter | Typical | Unit |
|-----------------|---|---------|--------------|
| $R_{\theta JL}$ | Thermal Resistance, Junction-to-Lead | 24 | $^\circ C/W$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | 40 | $^\circ C/W$ |

Electrical Characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|--|--|--|------|------|-----------|------------|
| Static Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise stated) | | | | | | |
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}=0V, I_D=250\mu A$ | 40 | -- | -- | V |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS}=40V, V_{GS}=0V$ | -- | -- | 1 | μA |
| | Zero Gate Voltage Drain Current($T_j=125^\circ\text{C}$) | $V_{DS}=40V, V_{GS}=0V$ | -- | -- | 100 | μA |
| I_{GSS} | Gate-Body Leakage Current | $V_{GS}=\pm 20V, V_{DS}=0V$ | -- | -- | ± 100 | nA |
| $V_{GS(TH)}$ | Gate Threshold Voltage | $V_{DS}=V_{GS}, I_D=250\mu A$ | 1.0 | | 3.0 | V |
| $R_{DS(ON)}$ | Drain-Source On-State Resistance ^② | $V_{GS}=10V, I_D=10A$ | -- | | 10 | m Ω |
| $R_{DS(ON)}$ | Drain-Source On-State Resistance ^② | $V_{GS}=4.5V, I_D=6A$ | -- | | 17 | m Ω |
| Dynamic Electrical Characteristics @ $T_j = 25^\circ\text{C}$ (unless otherwise stated) | | | | | | |
| C_{iss} | Input Capacitance | $V_{DS}=20V, V_{GS}=0V,$ $f=1\text{MHz}$ | 1115 | 1315 | 1515 | pF |
| C_{oss} | Output Capacitance | | 85 | 100 | 115 | pF |
| C_{rss} | Reverse Transfer Capacitance | | 65 | 80 | 95 | pF |
| R_g | Gate Resistance | $f=1\text{MHz}$ | -- | 1.7 | -- | Ω |
| $Q_g(10V)$ | Total Gate Charge | $V_{DS}=20V, I_D=10A,$ $V_{GS}=10V$ | -- | 22 | -- | nC |
| $Q_g(4.5V)$ | Total Gate Charge | | -- | 12 | -- | nC |
| Q_{gs} | Gate-Source Charge | | -- | 4.5 | -- | nC |
| Q_{gd} | Gate-Drain Charge | | -- | 4.2 | -- | nC |
| Switching Characteristics | | | | | | |
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DD}=20V,$ $I_D=10A,$ $R_G=3.0\Omega,$ $V_{GS}=10V$ | -- | 7.5 | -- | ns |
| t_r | Turn-on Rise Time | | -- | 3.8 | -- | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 24 | -- | ns |
| t_f | Turn-Off Fall Time | | -- | 5.5 | -- | ns |
| Source- Drain Diode Characteristics @ $T_j = 25^\circ\text{C}$ (unless otherwise stated) | | | | | | |
| V_{SD} | Forward on voltage | $I_{SD}=10A, V_{GS}=0V$ | -- | 0.8 | 1.2 | V |
| t_{rr} | Reverse Recovery Time | $T_j=25^\circ\text{C}, I_{SD}=10A,$ $V_{GS}=0V$ $di/dt=500A/\mu s$ | -- | 8.5 | -- | ns |
| Q_{rr} | Reverse Recovery Charge | | -- | 8 | -- | nC |

NOTE:

- ① Repetitive rating; pulse width limited by max junction temperature.
 ② Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

Typical Characteristics

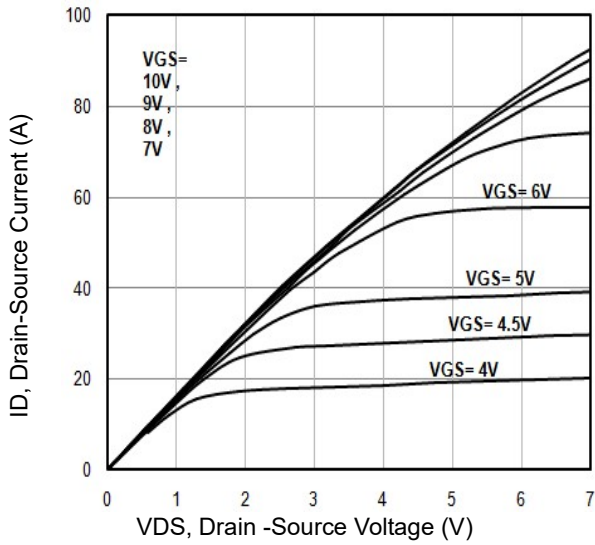


Fig1. Typical Output Characteristics

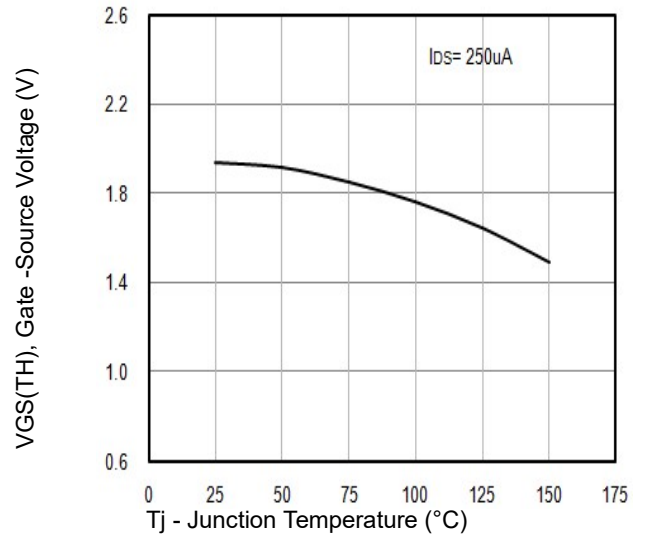


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. T_j

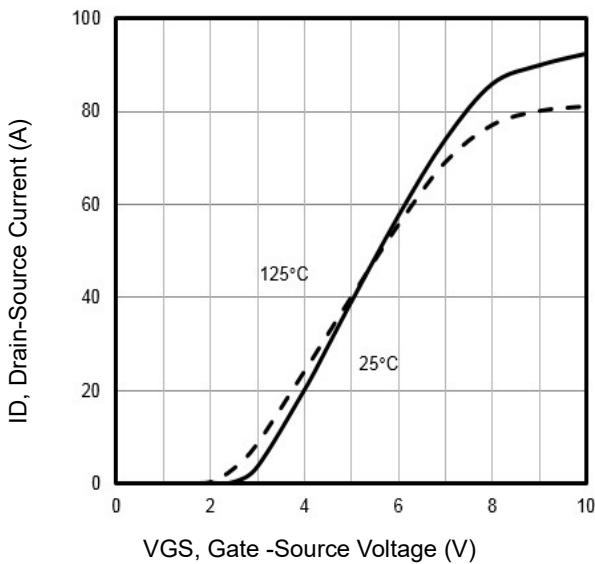


Fig3. Typical Transfer Characteristics

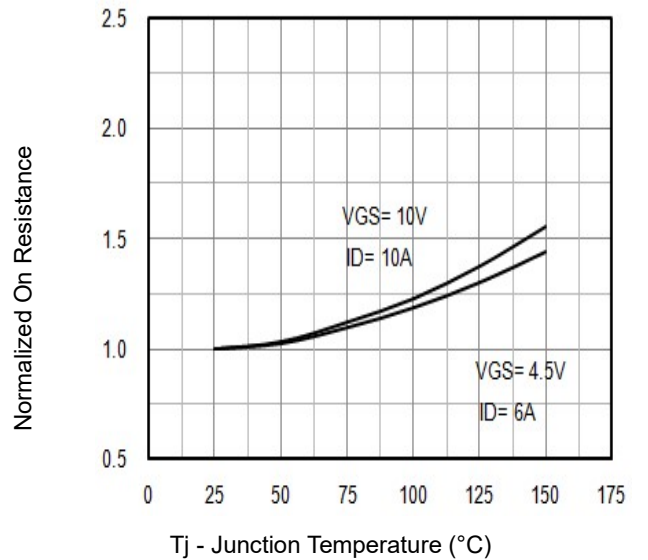


Fig4. Normalized On-Resistance Vs. T_j

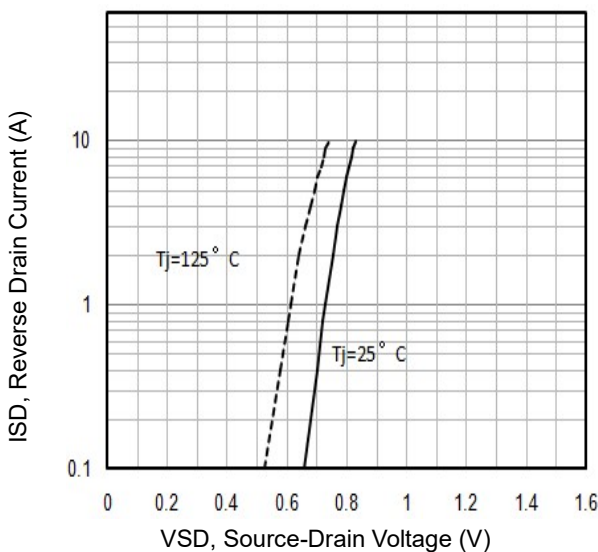


Fig5. Typical Source-Drain Diode Forward Voltage

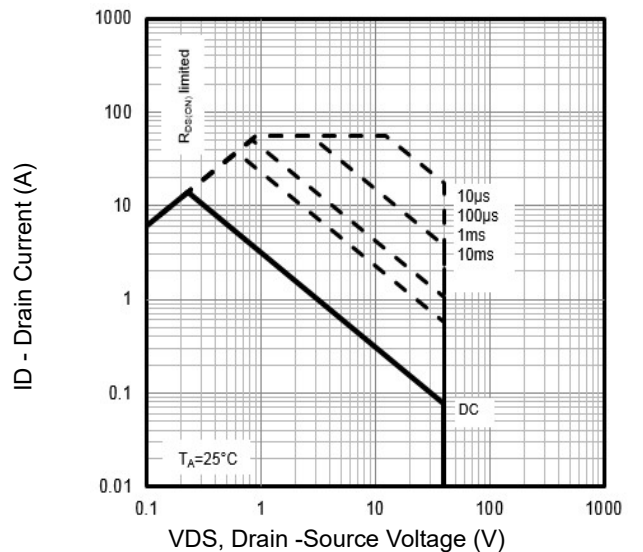


Fig6. Maximum Safe Operating Area

Typical Characteristics

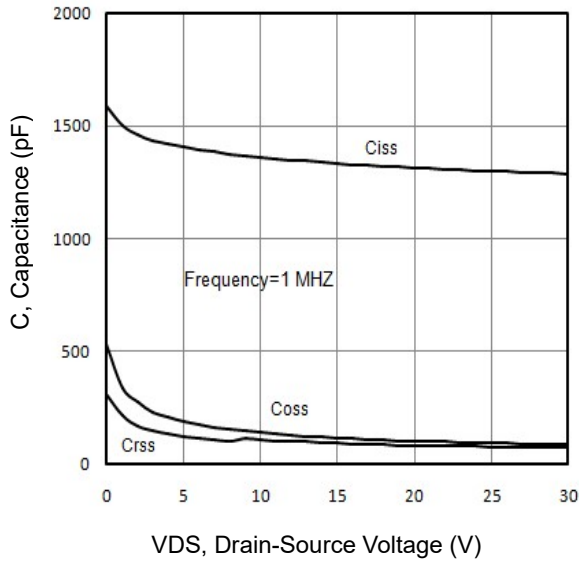


Fig7. Typical Capacitance Vs. Drain-Source Voltage

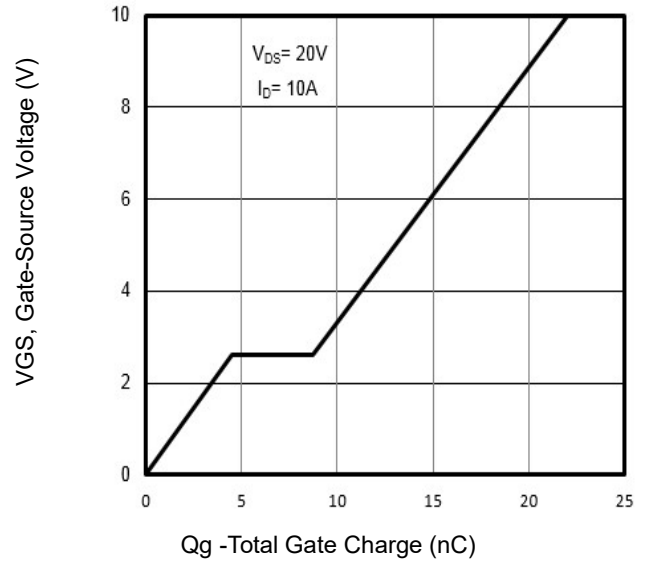


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

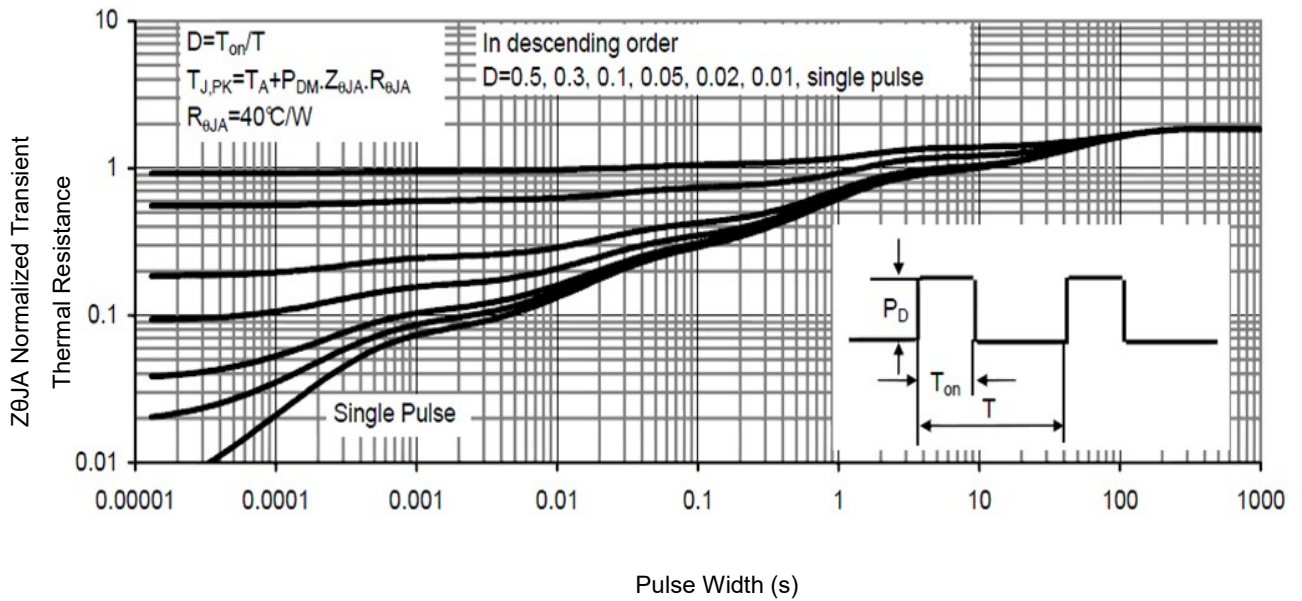


Fig9. Normalized Maximum Transient Thermal Impedance

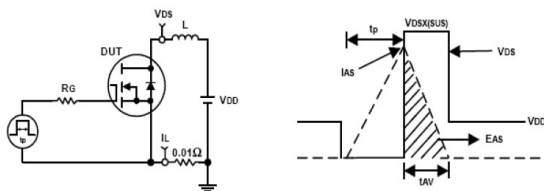


Fig10. Unclamped Inductive Test Circuit and waveforms

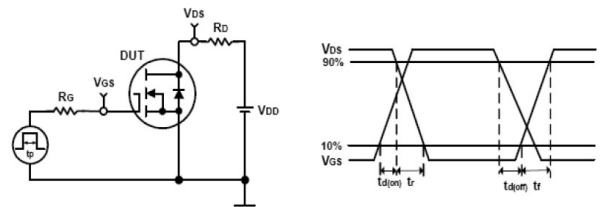


Fig11. Switching Time Test Circuit and waveforms