IAUC120N04S6N010ATMA1-VB Datasheet

N-Channel 40V (D-S) MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	40
$R_{DS(on)}$ (Ω) at V_{GS} = 10 V	0.00086
$R_{DS(on)}$ (Ω) at V_{GS} = 4.5 V	0.00116
Q_g typ. (nC)	59.2
I_D (A) [a, g]	180
Configuration	Single

FEATURES

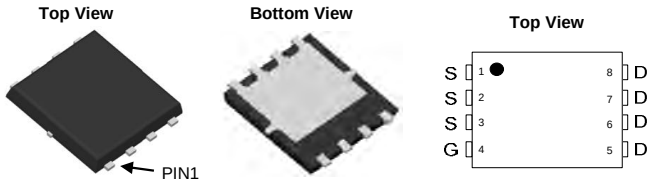
- Trench Gen IV power MOSFET
- 100 % R_g and UIS tested
- Q_{gd}/Q_{gs} ratio < 1 optimizes switching characteristics

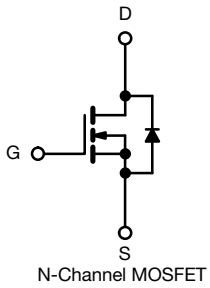
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Synchronous rectification
- OR-ing
- High power density DC/DC
- VRMs and embedded DC/DC
- DC/AC inverters
- Load switch

DFN5X6





ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	40	V
Gate-source voltage		V_{GS}	+20, -16	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	180 [g]	A
	T_C = 70 °C		144 [g]	
	T_A = 25 °C		72 [b, c]	
	T_A = 70 °C		36 [b, c]	
Pulsed drain current (t = 100 µs)		I_{DM}	720	
Continuous source-drain diode current	T_C = 25 °C	I_S	90	
	T_A = 25 °C		5.6 [b, c]	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	45	
Single pulse avalanche Energy		E_{AS}	101	mJ
Maximum power dissipation	T_C = 25 °C	P_D	100	W
	T_C = 70 °C		64	
	T_A = 25 °C		6.25 [b, c]	
	T_A = 70 °C		4 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [d, e]			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient [b, f]	t ≤ 10 s	R_{thJA}	15	20	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	0.95	1.25	

Notes

a. Based on T_C = 25 °C
b. Surface mounted on 1" x 1" FR4 board
c. t = 10 s
d. The DFN5x 6 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
f. Maximum under steady state conditions is 54 °C/W
g. Package limited

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	40	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA	-	25	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	-5.6	-	
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1	-	2.2	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = +20, -16 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 55 °C	-	-	10	
On-state drain current [a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	50	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A	-	0.00086	-	Ω
		V_{GS} = 4.5 V, I_D = 15 A	-	0.00116	-	
Forward transconductance [a]	g_{fs}	V_{DS} = 10 V, I_D = 20 A	-	106	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	-	8445	-	pF
Output capacitance	C_{oss}		-	1310	-	
Reverse transfer capacitance	C_{rss}		-	110	-	
C_{rss}/C_{iss} ratio			-	0.013	0.026	
Total gate charge	Q_g	V_{DS} = 20 V, V_{GS} = 10 V, I_D = 60 A	-	129	194	nC
		V_{DS} = 20 V, V_{GS} = 4.5 V, I_D = 60 A	-	59.2	89	
Gate-source charge	Q_{gs}		-	25	-	
Gate-drain charge	Q_{gd}		-	13	-	
Output charge	Q_{oss}	V_{DS} = 20 V, V_{GS} = 0 V	-	61	-	
Gate resistance	R_g	f = 1 MHz	0.2	0.7	1.2	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 20 V, R_L = 1 Ω, I_D ≅ 60 A, V_{GEN} = 10 V, R_g = 1 Ω	-	19	38	ns
Rise time	t_r		-	10	20	
Turn-off delay time	$t_{d(off)}$		-	53	106	
Fall time	t_f		-	10	20	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 20 V, R_L = 1 Ω, I_D ≅ 60 A, V_{GEN} = 4.5 V, R_g = 1 Ω	-	56	112	
Rise time	t_r		-	159	318	
Turn-off delay time	$t_{d(off)}$		-	54	108	
Fall time	t_f		-	36	72	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_C = 25 °C	-	-	180	A
Pulse diode forward current (t_p = 100 µs)	I_{SM}		-	-	720	
Body diode voltage	V_{SD}	I_S = 30 A	-	0.71	1.1	V
Body diode reverse recovery time	t_{rr}	I_F = 30 A, di/dt = 100 A/µs, T_J = 25 °C	-	64	128	ns
Body diode reverse recovery charge	Q_{rr}		-	116	232	nC
Reverse recovery fall time	t_a		-	40	-	ns
Reverse recovery rise time	t_b		-	24	-	

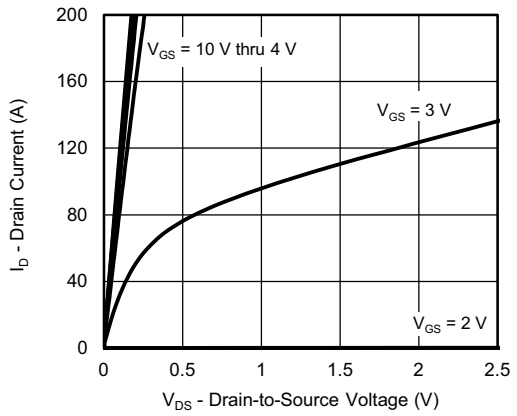
Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

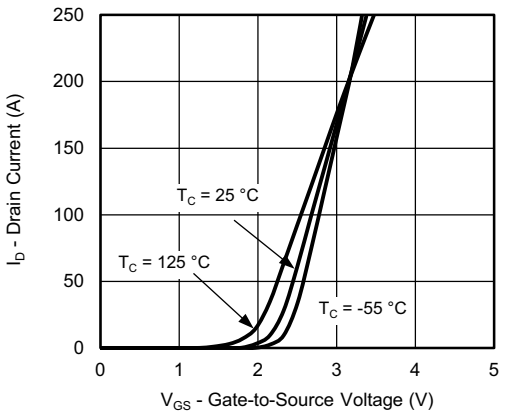
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

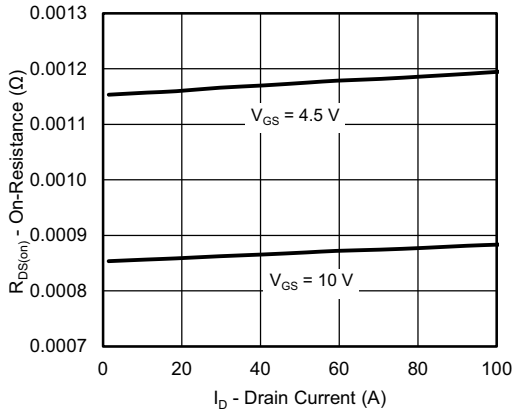
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



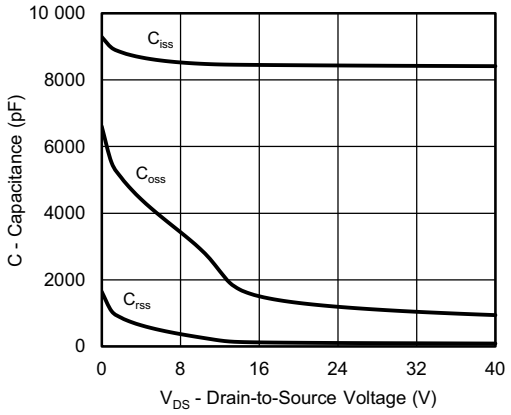
Output Characteristics



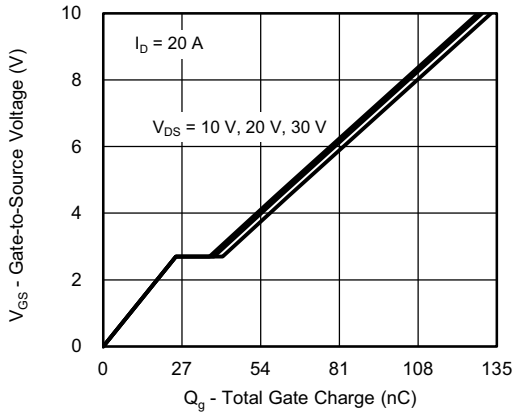
Transfer Characteristics



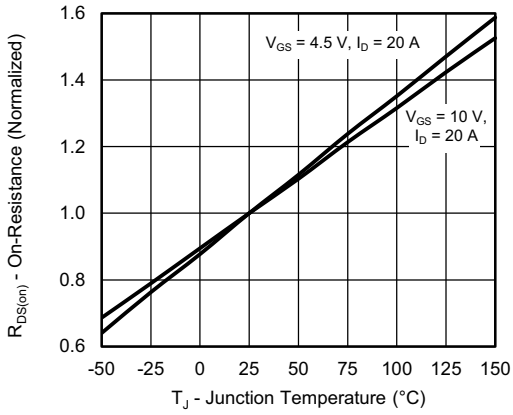
On-Resistance vs. Drain Current



Capacitance

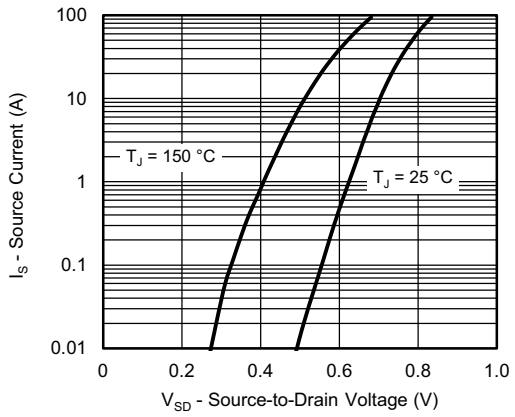


Gate Charge

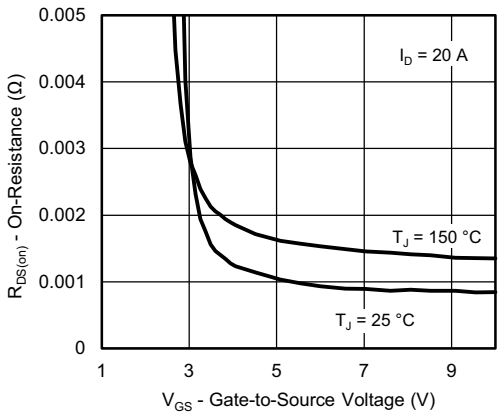


On-Resistance vs. Junction Temperature

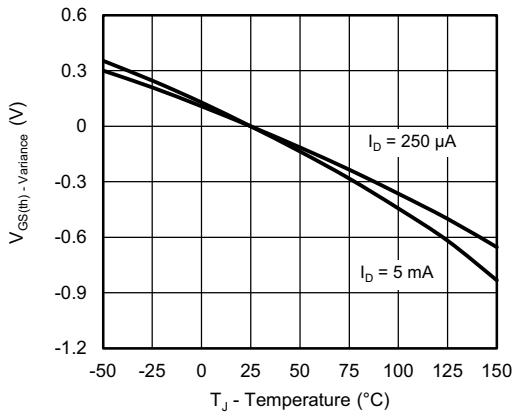
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



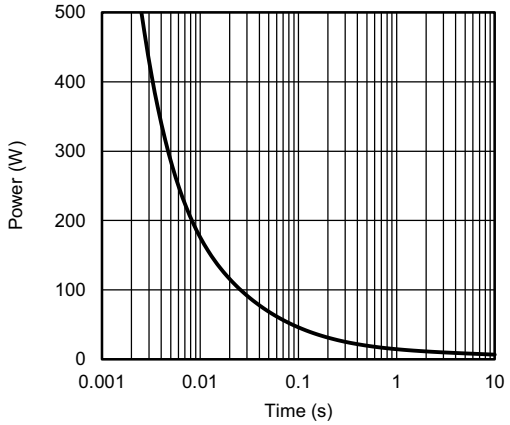
Source-Drain Diode Forward Voltage



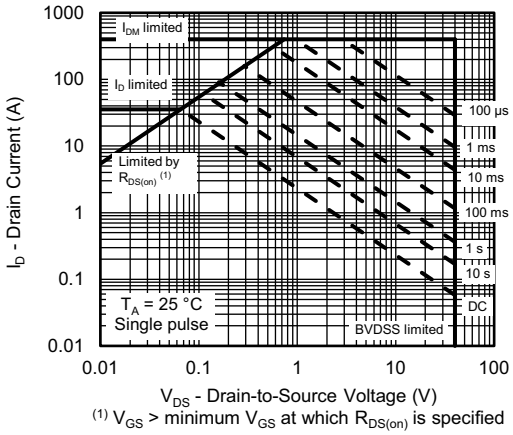
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

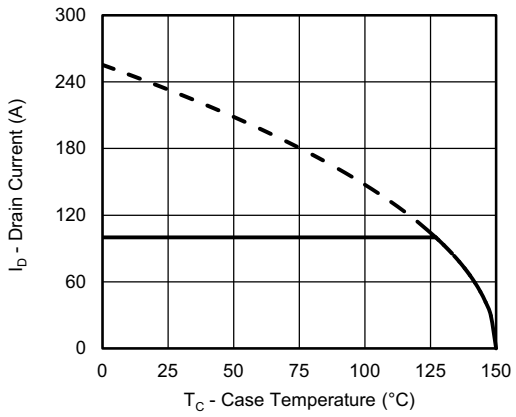


Single Pulse Power, Junction-to-Ambient

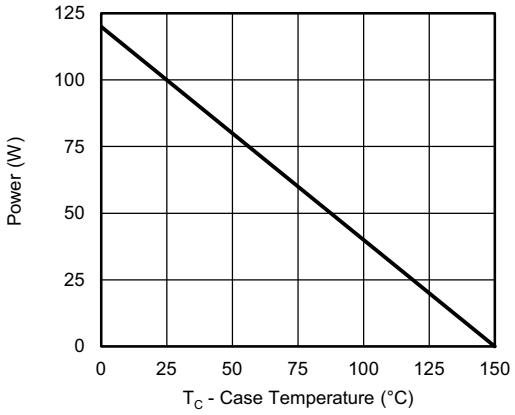


Safe Operating Area

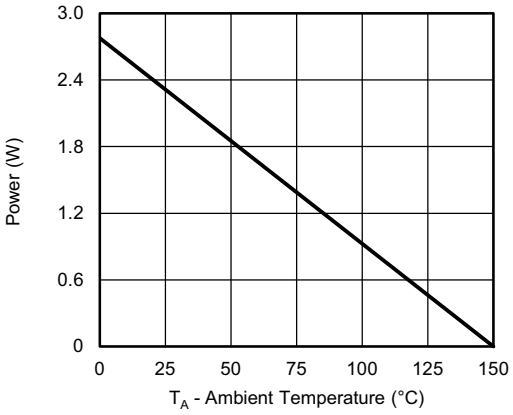
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]



Power, Junction-to-Case

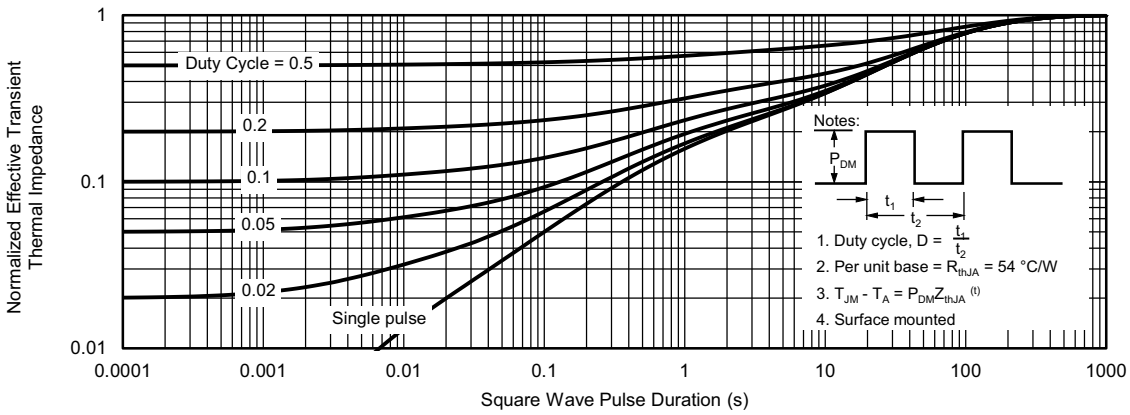


Power, Junction-to-Ambient

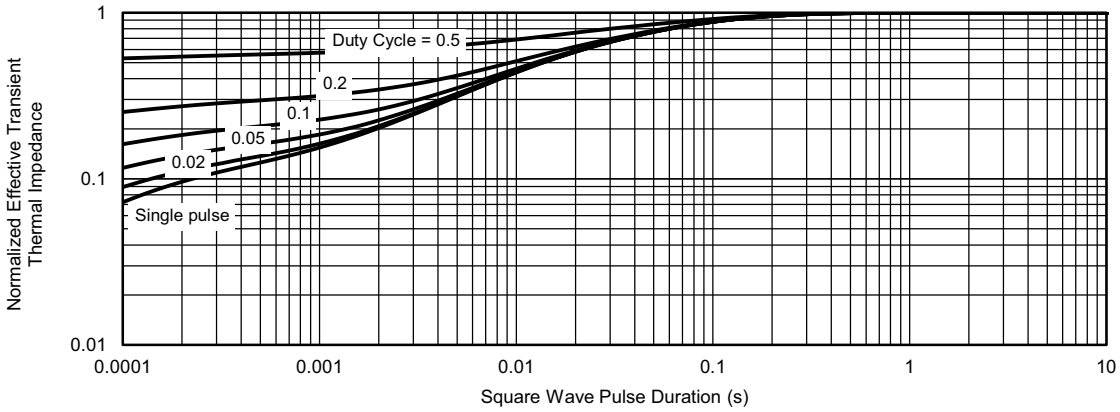
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

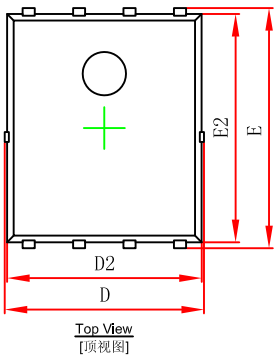


Normalized Thermal Transient Impedance, Junction-to-Ambient

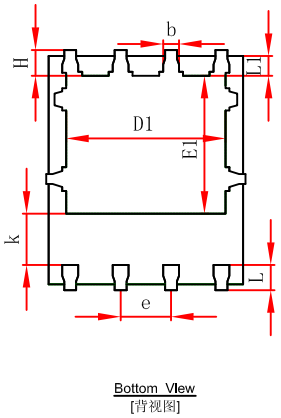


Normalized Thermal Transient Impedance, Junction-to-Case

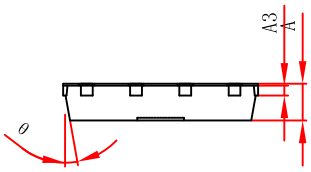
PDFNWB5x6-8L Package Outline Dimensions



Top View
[顶视图]



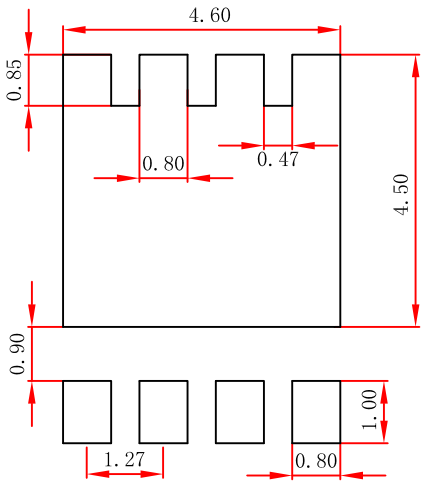
Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

PDFNWB5x6-8L Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

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