18V, 300mA Ultra-Low Quiescent current Linear Regulator

Features

- Input voltage range: 2.7V to 18V
- Available in fixed voltage option: 1.8V, 3.3V, 5V
- Output voltage tolerances of ±2%
- Rated output current: 300mA
- Ultra-Low Quiescent current: typical 1.5μA
- Typical 400mV dropout voltage @ I_{OUT}=100mA
- Internal short-circuit current limit
- Internal thermal overload protection
- SOT23-3L package

Applications

E-meters, Water Meters and Gas Meters

Fire Alarm, Smoke Detector

Appliances and White Goods

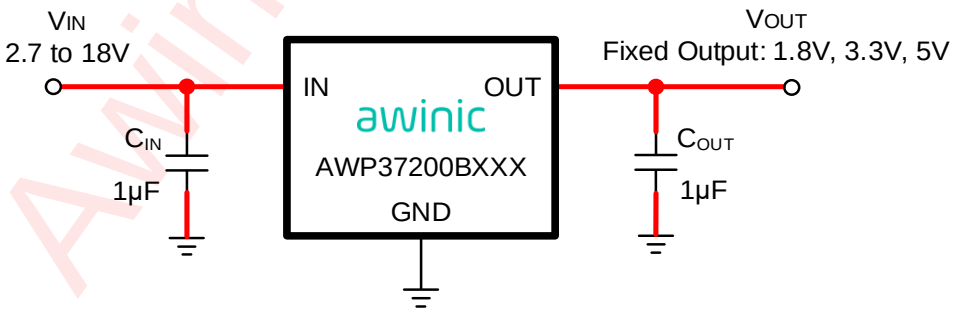
General Description

AWP37200BXXX is a ultra-low quiescent current regulator features low dropout voltage and low current in the standby mode. With less than 1.5μA quiescent current at no load, the AWP37200BXXX is ideally suited for standby micro-control-unit systems, especially for always-on applications like E-meters, fire alarms, smoke detectors and other battery operated systems.

With adequate heat sinking, the AWP37200BXXX can deliver 300mA output current. Current limiting is included to limit the peak output current to a safe value. The AWP37200BXXX retains all of the features that are common to low dropout regulators including a low dropout PMOS pass device, short circuit protection, and thermal shutdown..

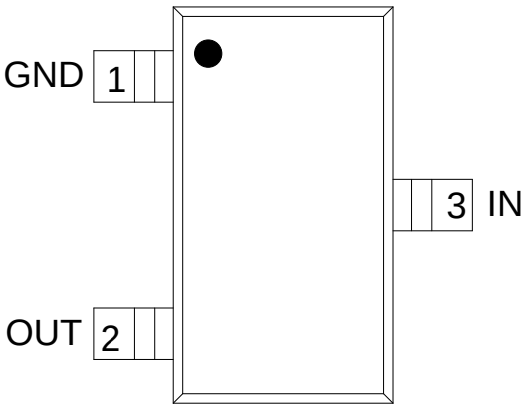
The AWP37200BXXX is available in SOT23-3L package, which is useful for cost-effective board manufacturing.

Typical Application Circuit

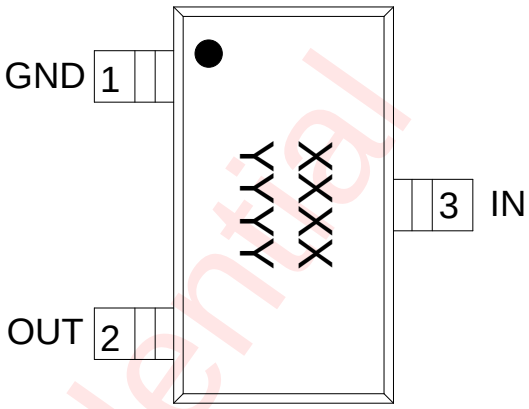


Pin Configuration And Top Mark

AWP37200BXXXSTR
Top View



AWP37200BXXXSTR Marking
Top View

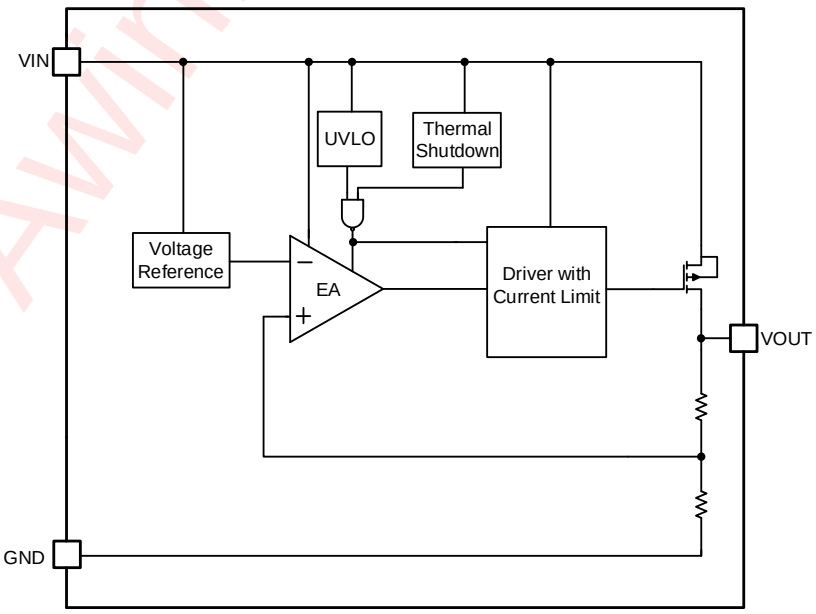


XXXX - AWP37200BXXXSTR
YYYY - Production Tracing Code

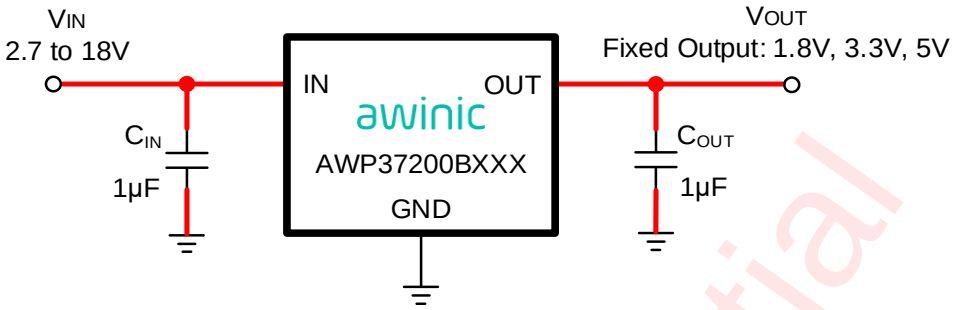
Pin Definition

No.	NAME	DESCRIPTION
1	GND	Ground.
2	OUT	Regulated output voltage pin. Put a 1μF or more ceramic capacitor at the output pin.
3	IN	Input supply pin. Put a 1μF or more bypass capacitor at the power supply.

Functional Block Diagram



Typical Application Circuit



AWP37200BXXX Application Circuit

Notice for typical application circuits:

Capacitance of C_{IN} should be 1μF or more and C_{OUT} should be 1μF or more. The effective capacitance of C_{OUT} ≥ 0.5μF is recommended to assure the stability of circuit. The rated voltage of C_{IN} and C_{OUT} should be higher than V_{IN} and V_{OUT} voltage.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWP37200B180STR	-40°C～105°C	SOT23-3L	4YDB	MSL3	ROHS+HF	3000 units/ Tape and Reel
AWP37200B330STR	-40°C～105°C	SOT23-3L	BCPY	MSL3	ROHS+HF	3000 units/ Tape and Reel
AWP37200B500STR	-40°C～105°C	SOT23-3L	U3UY	MSL3	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Input voltage range		-0.3V to 20V
Maximum operating junction temperature T_{J_MAX}		125°C
Recommended operating temperature T_A		-40°C to 105°C
Storage temperature T_{STG}		-65°C to 150°C
Junction-to-ambient thermal resistance $R_{\theta JA}$(NOTE2)		190°C/W
Lead temperature (soldering 10 seconds)		260°C
ESD	HBM (Human body model)(NOTE3)	±2kV
	CDM(Charged device model) (NOTE4)	±1.5kV

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Thermal resistances follow JEDEC 2S2P standards, and is usually highly dependent on PCB layout.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS-001-2023.

NOTE4: All pins. Test Condition: ESDA/JEDEC JS-002-2022.

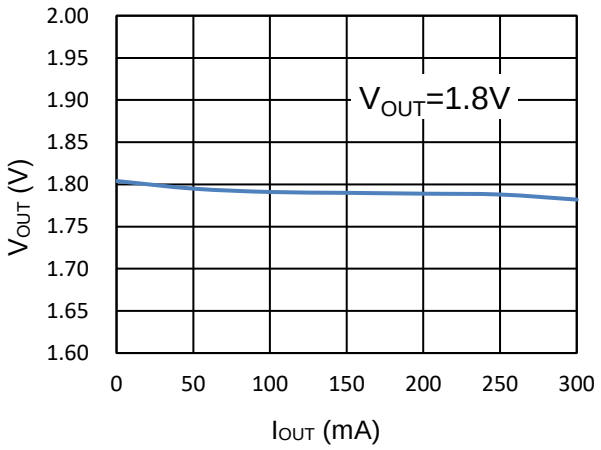
Electrical Characteristics

V_{IN}=12V, I_{OUT}=1mA, C_{IN}=C_{OUT}=1μF, T_J=25°C (unless otherwise noted)

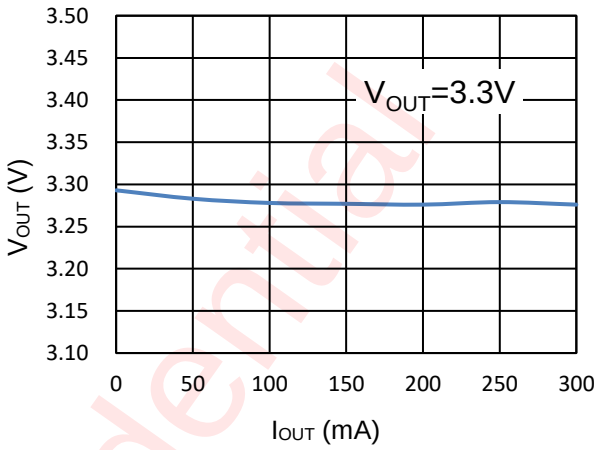
PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range			2.7		18	V
V_{OUT}	Output Voltage Accuracy			-2		2	%
$LINE_{Reg}$	Line Regulation	V_{IN}=V_{OUT}+1V to 18V			2		mV
$LOAD_{Reg}$	Load Regulation	I_{OUT}=1mA to 100mA			20		mV
$V_{dropout}$	Dropout Voltage	I_{OUT}=100mA, When V_{OUT} falls to 98%*$V_{OUT(SET)}$			400		mV
I_Q	Quiescent Current	I_{OUT}=0mA			1.5		μA
PSRR	Power Supply Ripple Rejection	I_{OUT}=30mA	f=1kHz		70		dB
			f=10kHz		78		
I_{CL}	Output Current Limit	V_{OUT}=90%*$V_{OUT(SET)}$		300	620		mA
T_{SDH}	Thermal Shutdown Threshold	Temperature Rising			140		°C
T_{SDL}	Thermal Shutdown Reset Threshold	Temperature Falling			120		°C

Typical Characteristics

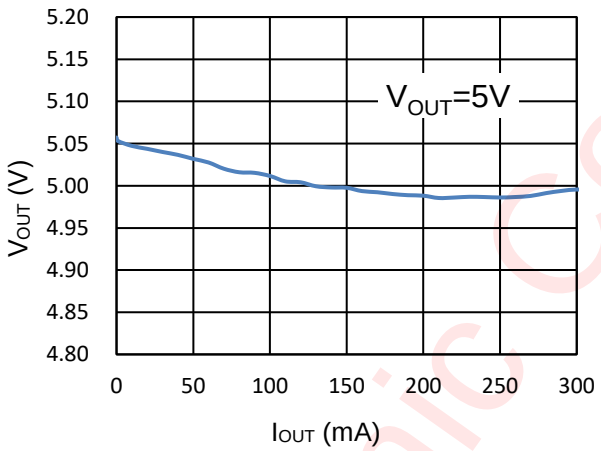
V_{IN}=V_{OUT}+2V, I_{OUT}=1mA, C_{IN}=C_{OUT}=1μF, T_J=25°C. In Typical Application Circuit, unless otherwise noted.



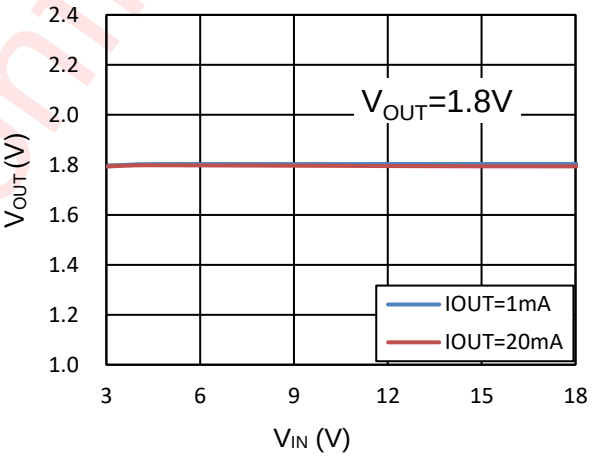
Output Voltage vs Output Current



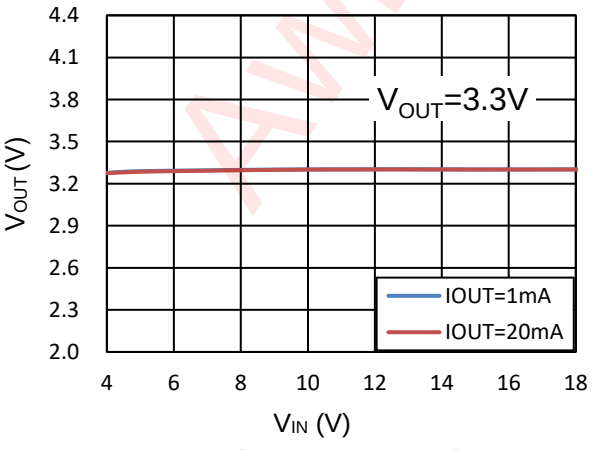
Output Voltage vs Output Current



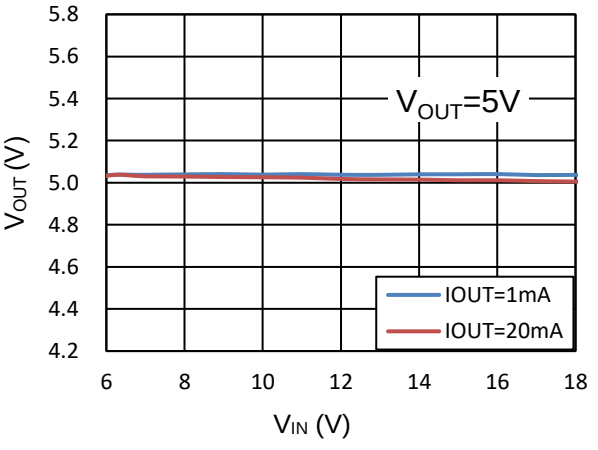
Output Voltage vs Output Current



Output Voltage vs Input Voltage



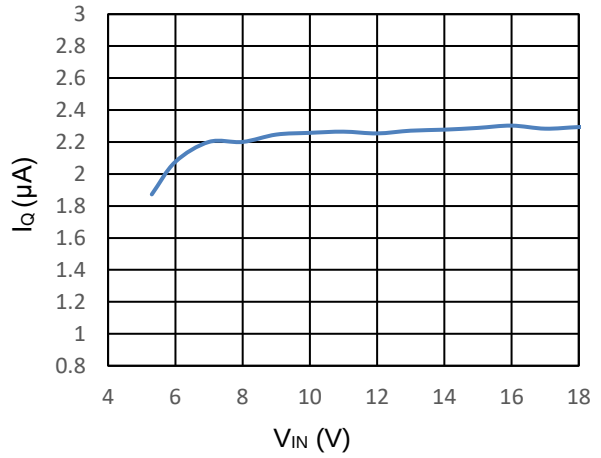
Output Voltage vs Input Voltage



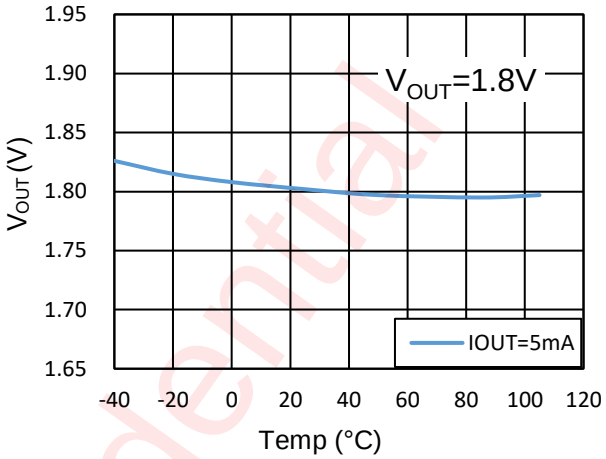
Output Voltage vs Input Voltage

Typical Characteristics (Continued)

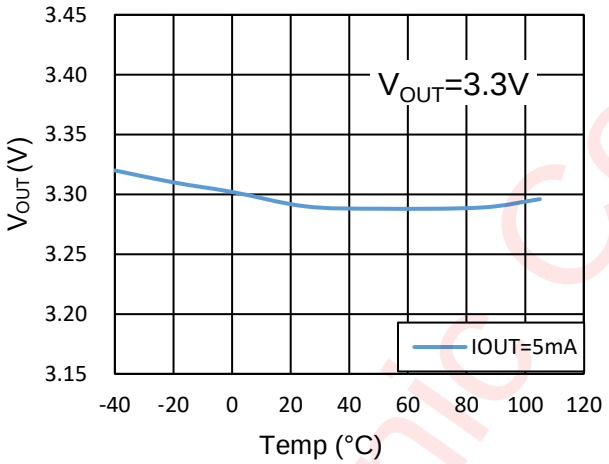
V_{IN}=V_{OUT}+2V, I_{OUT}=1mA, C_{IN}=C_{OUT}=1μF, T_J=25°C. In Typical Application Circuit, unless otherwise noted.



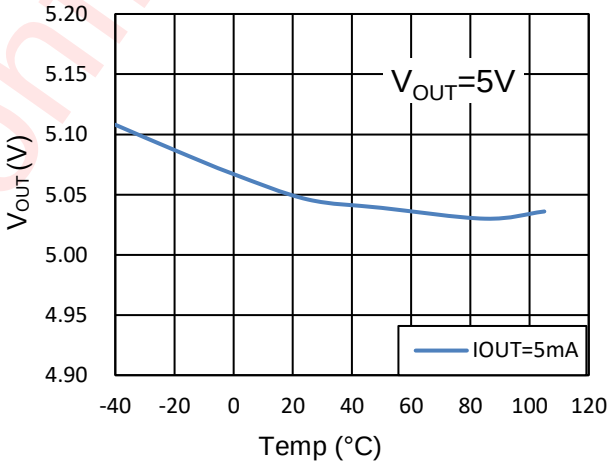
Quiescent Current vs Input Voltage



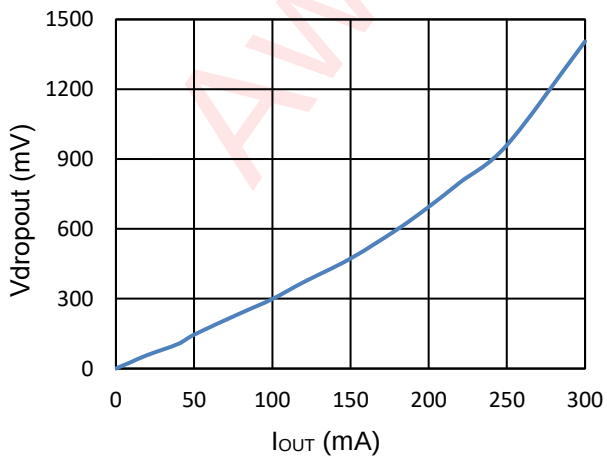
Output Voltage vs Temperature



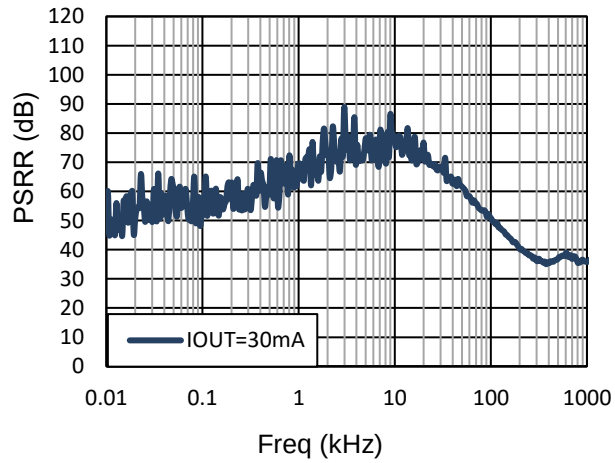
Output Voltage vs Temperature



Output Voltage vs Temperature



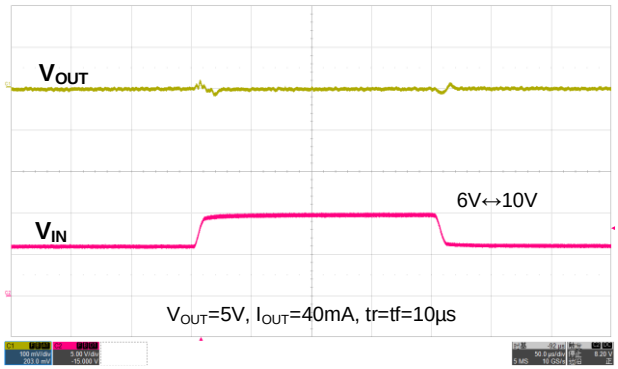
Dropout Voltage vs Output Current



PSRR vs Frequency

Typical Characteristics (Continued)

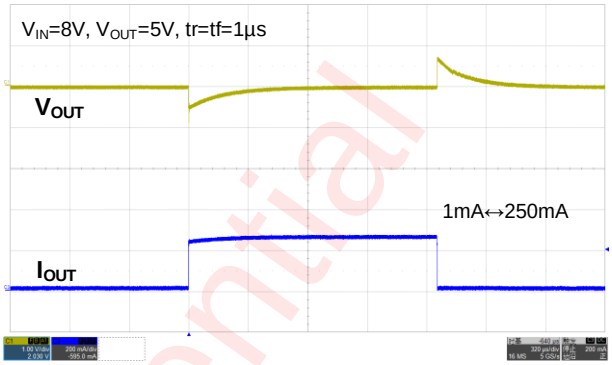
V_{IN}=V_{OUT}+2V, I_{OUT}=1mA, C_{IN}=C_{OUT}=1μF, T_J=25°C. In Typical Application Circuit, unless otherwise noted.



V_{OUT}: 100mV/div V_{IN}: 5V/div

Time(50μs/div)

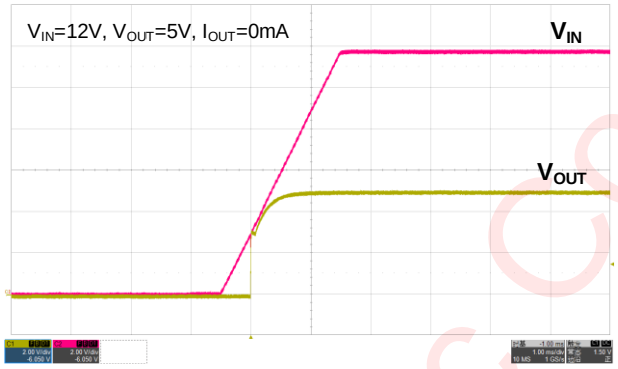
Input Transient Response



V_{OUT}: 1V/div I_{OUT}: 200mA/div

Time(320μs/div)

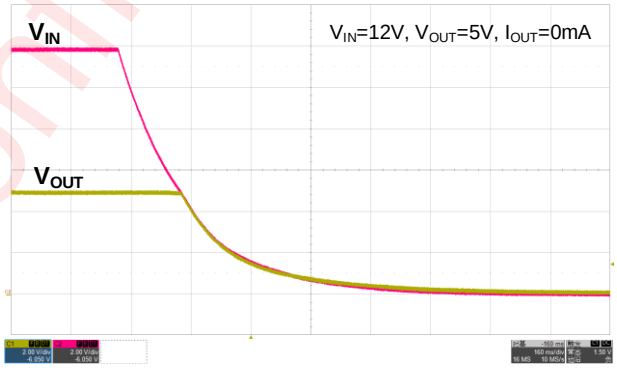
Load Transient Response



V_{OUT}: 2V/div V_{IN}: 5V/div

Time(1ms/div)

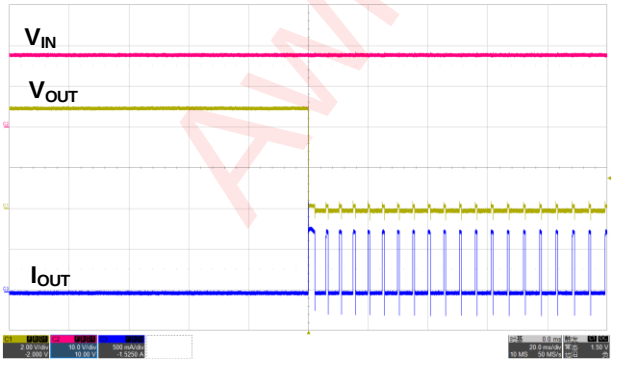
Turn On with V_{IN}



V_{OUT}: 2V/div V_{IN}: 2V/div

Time(160ms/div)

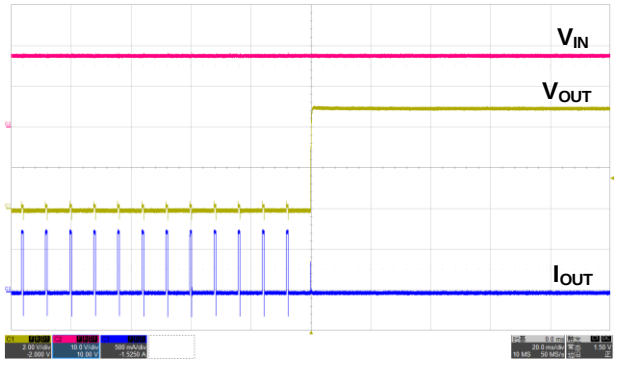
Turn Off with V_{IN}



V_{OUT}: 2V/div V_{IN}: 10V/div I_{OUT}: 500m/div

Time(20ms/div)

V_{OUT} Short to GND



V_{OUT}: 2V/div V_{IN}: 10V/div I_{OUT}: 500mA/div

Time(20ms/div)

V_{OUT} Short and Release

Detailed Functional Description

The AWP37200BXXX is available in fixed output voltages 1.8V, 3.3V and 5V. The linear regulator input supply must be well regulated and kept at a voltage level to not exceed the maximum input to output voltage differential allowed by the device. The minimum dropout voltage (V_{IN} – V_{OUT}) must be met with extra headroom when possible to keep the output well regulated. A 1μF or higher capacitor must be placed at the input to bypass noise. The output voltage tolerance is ±2%.

Output Current Limit

AWP37200BXXX integrates output current limit function, protecting IC from excessive current.

When the load is excessively heavy, AWP37200BXXX limits the current flowing through the IC to a typical 620mA current. This value is specially designed, so that IC is protected properly and the output capability of 300mA is not influenced either.

There is also internal short-circuit current limit that shuts down the device if the output current becomes too high.

Thermal Shutdown

AWP37200BXXX integrates thermal shutdown function, protect IC from excessively high temperature.

When the chip temperature exceeds 140°C, AWP37200BXXX detects it as an over-temperature event, triggering thermal shutdown, which will turn off the main function module, including power MOSFET. This inhibits increase of chip's temperature. IC would keep the protection-state on until the chip's temperature falls below to 120°C. At this moment, the over-temperature protection-state is released, IC resumes to work again. The hysteresis avoids IC's turning off and on frequently around the thermal shutdown threshold.

Application Information

Power Dissipation and Device Operation

The permissible power dissipation is dependent on the ambient temperature T_A and the junction-to-ambient thermal resistance $R_{\theta JA}$.

The absolute maximum allowable power dissipation for the device in a given package can be calculated using Equation below, where T_{J_MAX} = 125°C :

$$PD_{MAX\_ABS} = (T_{J\_MAX} – T_A) / R_{\theta JA}$$

The recommended maximum allowable power dissipation for the device in a given package can be calculated using Equation below, where T_{J_REC} = 125°C :

$$PD_{MAX\_REC} = (T_{J\_REC} – T_A) / R_{\theta JA}$$

The actual power being dissipated in the device can be represented by Equation below:

$$PD_{ACT} = (V_{IN} – V_{OUT}) \times I_{OUT}$$

These equations above establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device.

Capacitors Selection

IN pin: Input Capacitor C_{IN}

AWP37200BXXX advises to use a 1μF or more X5R or X7R ceramic capacitor at IN pin as shown in Typical Application Circuit.

OUT pin: Output Capacitor C_{OUT}

AWP37200BXXX advises to use a 1μF or more X5R or X7R ceramic capacitor at OUT pin as shown in Typical Application Circuit. The minimum effective capacitance of C_{OUT} that AWP37200BXXX can remain stable is 0.5μF. For ceramic capacitor, temperature, DC bias and package size will change the effective capacitance, so enough margin of C_{OUT} must be considered in design. Additionally, C_{OUT} with larger capacitance and lower ESR will help increase the high frequency PSRR and improve the load transient response.

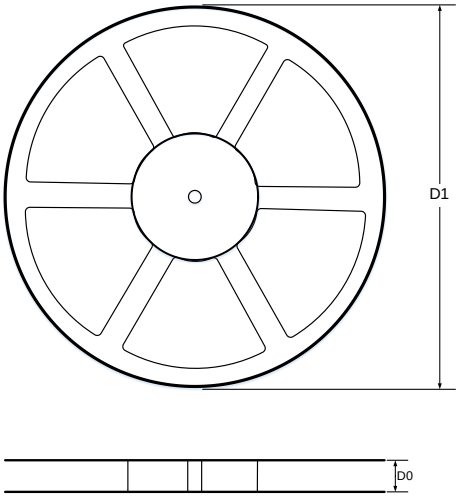
PCB Layout Consideration

The performance of a power source circuit using this device is highly dependent on a peripheral circuit. To obtain the optimal performance, a peripheral component or the device mounted on PCB should not exceed its rated voltage, rated current or rated power. When designing a peripheral circuit, guidelines below for PCB layout of AWP37200BXXX should be obeyed:

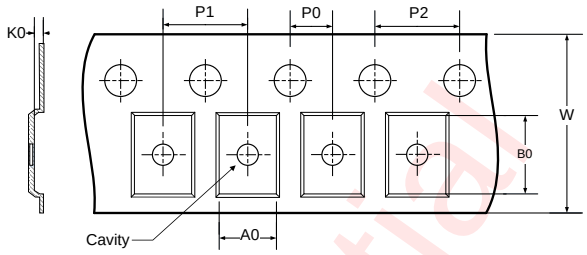
1. All peripheral components should be placed as close to the chip as possible. C_{IN} and C_{OUT} should be close to IN and OUT pins respectively. Avoid connecting device and chip pins with two different layers of copper, use the same layer of copper instead.
2. IN and OUT pin are the large current input and output of the chip, make IN, OUT, and meanwhile GND lines sufficient.
3. The connection lines between the planes of C_{IN} or C_{OUT} and respective chip pin should be as short and wide as possible, to reduce noise and EMI interference, or it may cause noise pickup or unstable operation.
4. The exposed plane of chip and GND pins must be connected to the large-area ground layer of PCB directly, meanwhile place sufficient vias below the exposed plane. Thus we can decrease the thermal resistor on the board to optimize heat-diffusion performance.

Tape And Reel Information

REEL DIMENSIONS

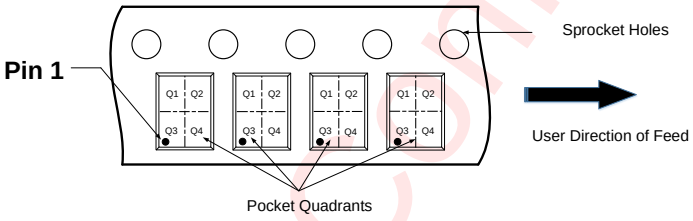


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



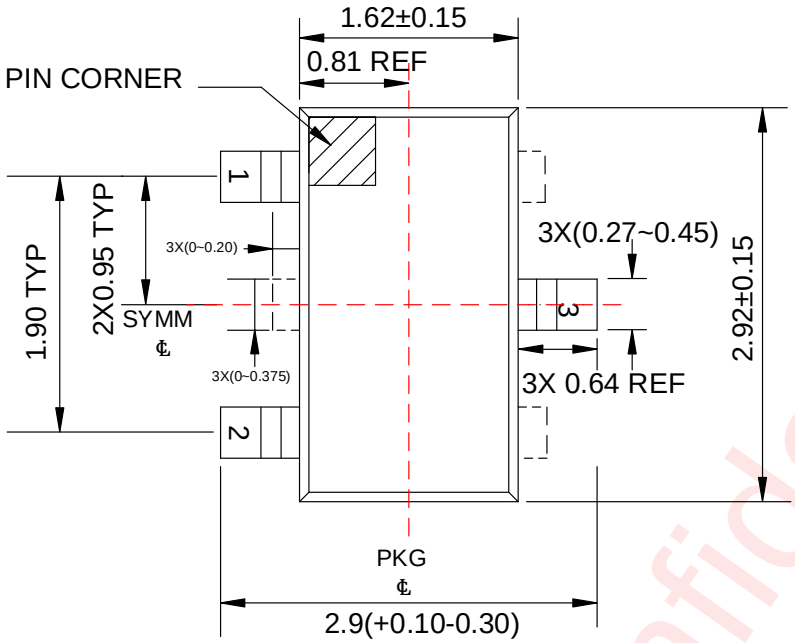
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

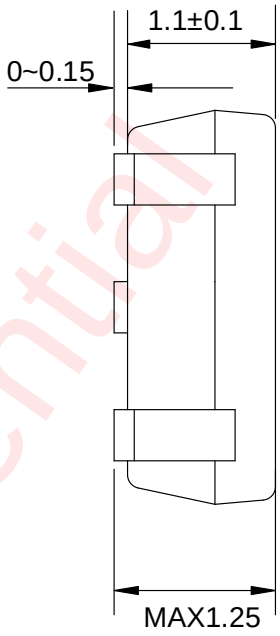
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	9	3.18	3.28	1.32	2	4	4	8	Q3

All dimensions are nominal

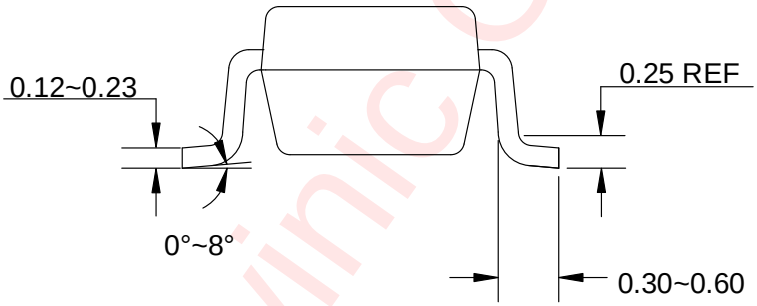
Package Description



Top View



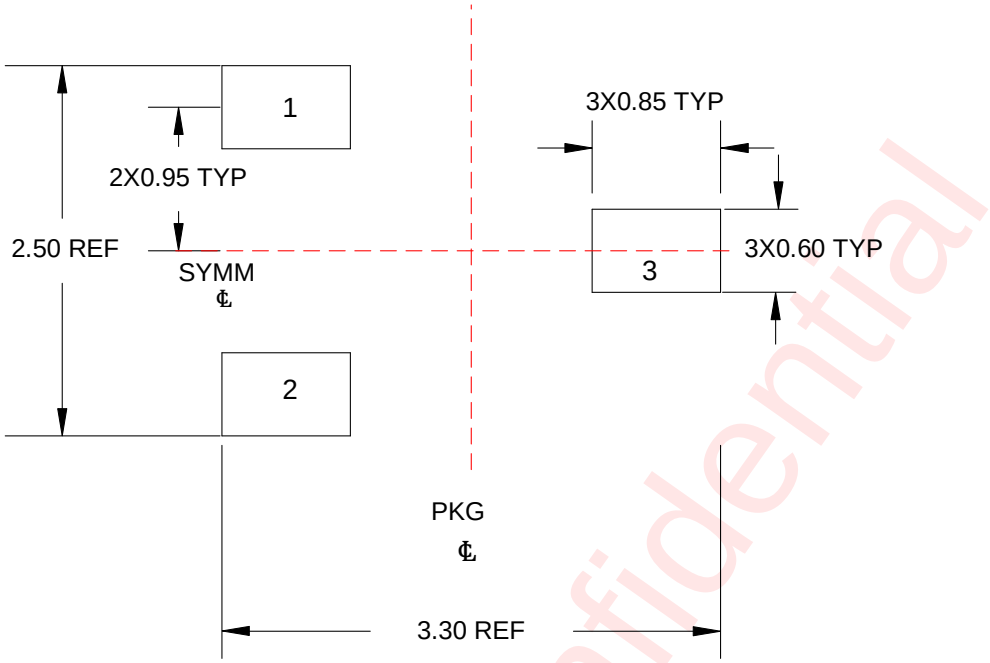
Side View

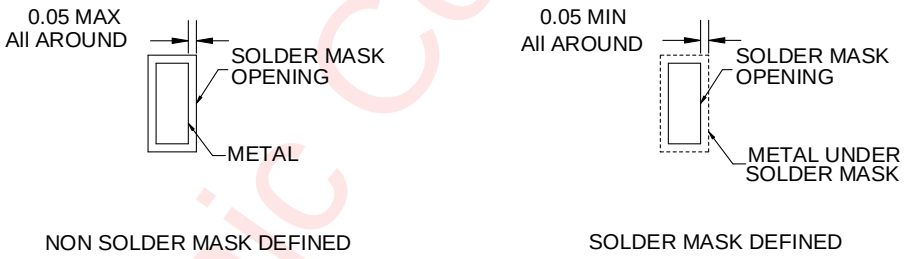


Side View

Unit: mm

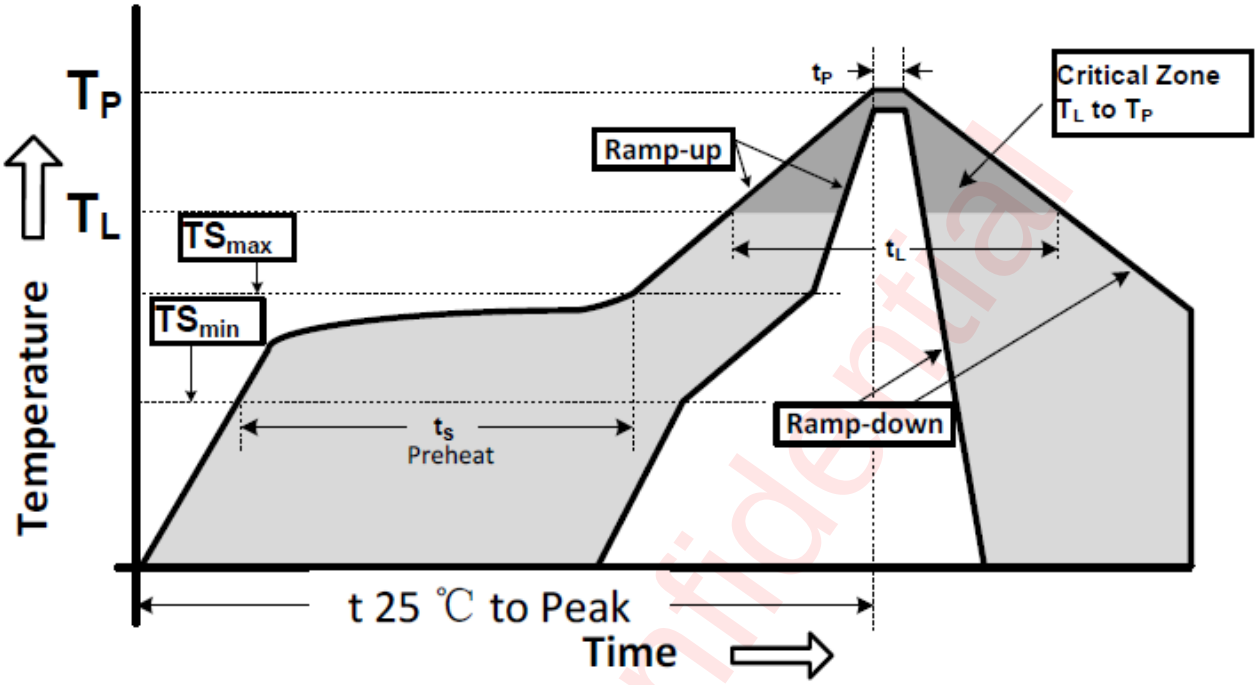
Land Pattern Data





Unit：mm

Reflow



Reflow Note	Spec
Ramp-up rate（TSmax to T_P）	3°C/second max.
Preheat temperature（TSmin to TSmax）	150°C to 200°C
Preheat time（t_s）	60 - 180 seconds
Time above T_L , 217°C（t_L）	60 - 150 seconds
Peak temperature（T_P）	260°C
Time within 5°C of peak temperature(t_P)	20 - 40 seconds
Ramp-down rate	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

Revision History

Version	Date	Change Record
V1.0	Oct. 2024	Officially released
V1.1	Dec. 2024	Modify the rated output current
V1.2	Nov. 2025	1.Add the value of θ_{JA}(P4) 2.Add the information of 1.8V and 3.3V.
V1.3	Dec. 2025	Update the Typical Characteristics(P6~P8)

Disclaimer

All trademarks are the property of their respective owners. Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.