36-Channel Intelligent 8-Bit RGB LED Driver

Features

- 36-channel RGB LED Driver
  - Individual 256-level PWM for dimming
- High-precision current sinks
  - Device-to-device error: ±7%
  - Channel-to-channel error: ±7%
- EMI and audible noise reduction
  - Spread spectrum function
- LED open/short detection per channel
- Auto power saving mode when all LEDs off > 32ms
- Over-temperature protection
- 400kHz I²C interface, four selectable addresses
- Power supply: 2.7V~5.5V
- QFN 5mmX5mmX0.75mm-44L package

Applications

Smart speaker

E-sports devices

Smart home appliance

General Description

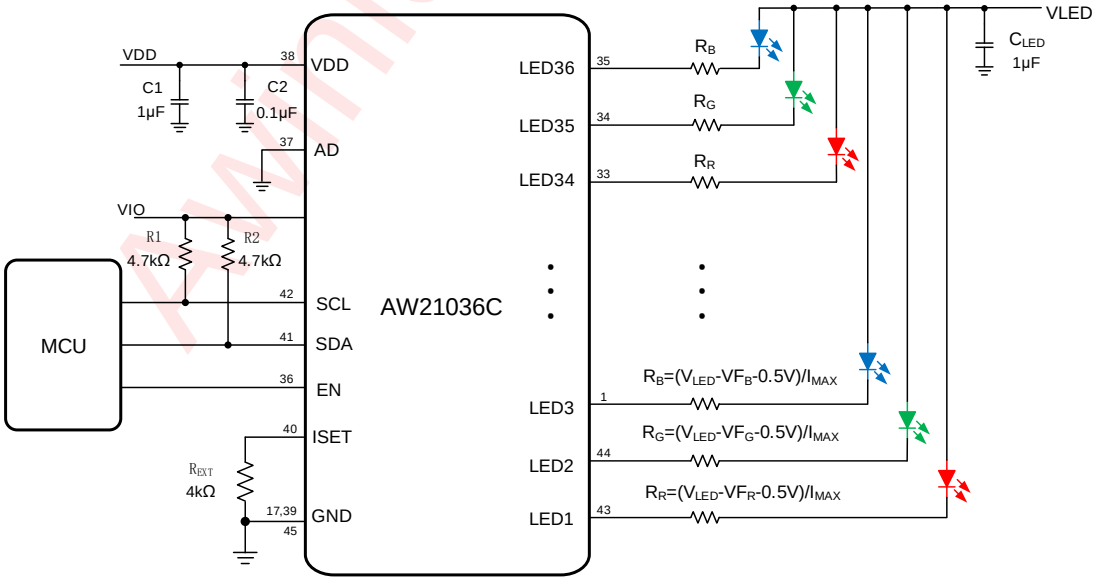
AW21036C is a 36-channel high precision constant current LED driver. Each channel has individual 8-bit PWM current for brightness control. The maximum global current of each channel is recommended to be 40mA configured via external resistor R_{EXT}.

Programmable spread spectrum technology are utilized to reduce EMI and audible noise caused by MLCC when LEDs turn on or off simultaneously.

AW21036C can be turned off with minimum current consumption by either pulling the EN pin low or setting bit GCR.CHIPEN=0.

AW21036C is available in QFN 5mmX5mmX 0.75mm-44L package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +85°C.

Typical Application Circuit

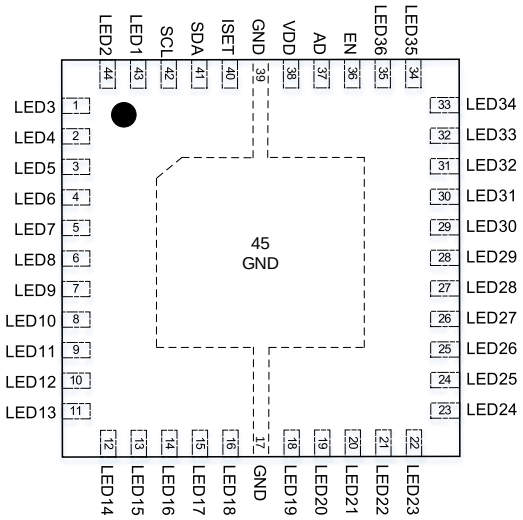


Note: The resistors(R_R,R_G,R_B) between LED and IC are only for thermal reduction. For more information, please refer to application information.

Figure 1 AW21036C Application Circuit

Pin Configuration And Top Mark

AW21036CQNR
(Top View)



AW21036CQNR
(Top View)

A1JD – AW21036CQNR
XXXX – Production Tracing Code

Figure 2 Pin Configuration and Marking

Pin Definition

No.	NAME	DESCRIPTION
1~16	LED3~LED18	Constant current sink, connect to LED's cathode.
17, 39	GND	Ground.
18~35	LED19~LED36	Constant current sink, connect to LED's cathode.
36	EN	Shutdown the chip when pulled low.
37	AD	I^2C address setting, connects to GND, VDD, SCL or SDA for different device address of I^2C. Internally pulled down to GND with a resistor of 400kΩ.
38	VDD	Power supply: 2.7V~5.5V
40	ISET	When R_{EXT}=4.0kΩ, global current of LED is 20mA.
41	SDA	Serial data I/O for I^2C interface.
42	SCL	Serial clock input for I^2C interface.
43, 44	LED1, LED2	Constant current sink, connect to LED's cathode.
45	GND	Ground.

Functional Block Diagram

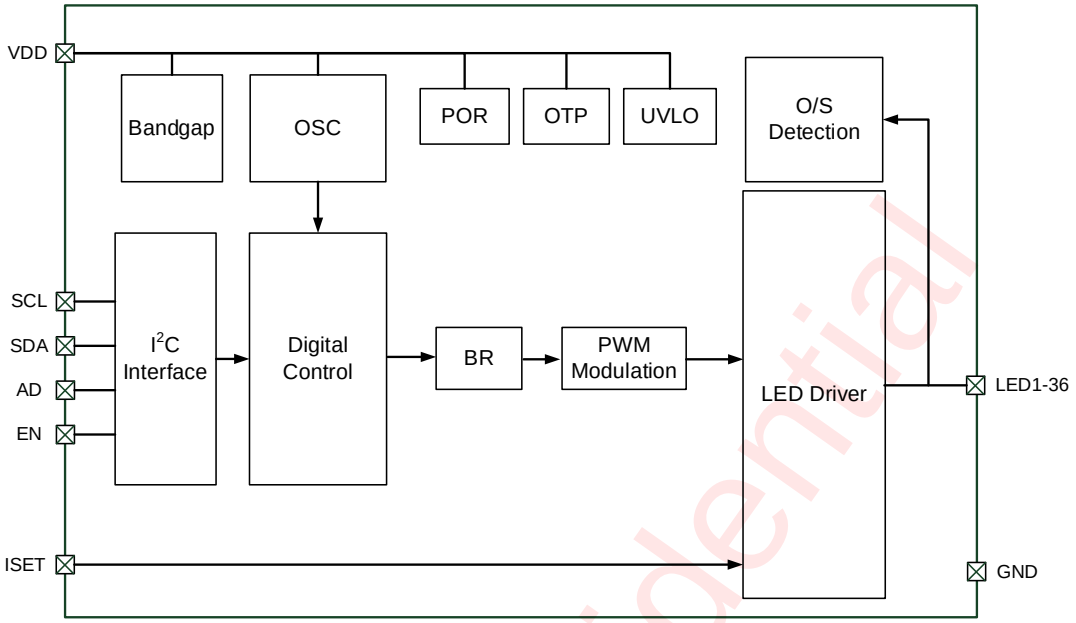
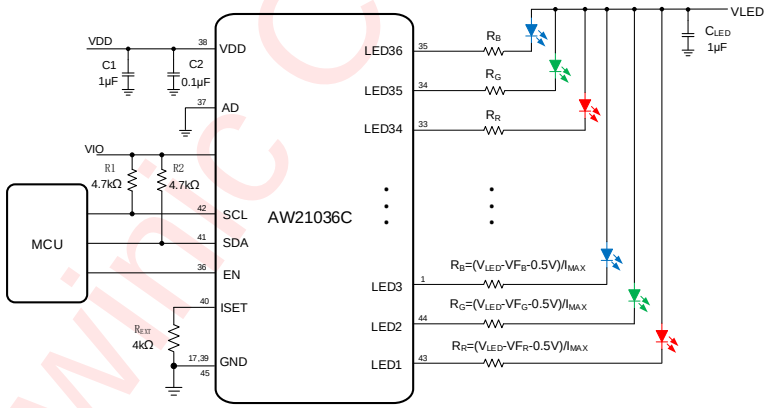


Figure 3 Functional Block Diagram

Typical Application Circuit



Note: The resistors(R_R,R_G,R_B) between LED and IC are only for thermal reduction. For more information, please refer to application information.

Figure 4 AW21036C Typical Application Circuit

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW21036CQNR	-40°C~85°C	QFN 5mmX5mmX0.75mm-44L	A1JD	MSL3	ROHS+HF	6000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage range VDD		-0.3V to 6V
Input voltage range	SCL, SDA, EN, AD	-0.3V to 6V
Output voltage range	LED1~LED36	-0.3V to 6V
Junction-to-ambient thermal resistance θ_{JA}		43.07°C/W
Operating free-air temperature range		-40°C to 85°C
Maximum operating junction temperature T_{JMAX}		160°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD (NOTE 2)		
HBM		±2kV
CDM		±1.5kV
Latch-Up		
Test condition: JEDEC EIA/JESD78E		+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ANSI/ESDA/JEDEC JS-001-2017. CDM test method: JEDEC EIA/JESD22-C101F.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating free-air temperature range	-40		85	°C
VDD	Input voltage	2.7		5.5	V
LED1~LED36	Voltage on LEDx	0		5.5	V
C_1, C_{LED}	Input capacitance	1		22	μF
C_2	Input capacitance	0.1		1	μF
R_1, R_2	External resistor for I^2C	1	4.7	10	kΩ
R_{EXT}	External resistor for setting sink current	2	4	20	kΩ

Electrical Characteristics

T_A=25°C, R_{EXT}=4kΩ, VDD=3.6V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Power supply voltage and current						
VDD	Power supply voltage		2.7		5.5	V
I_{STB_VDD}	Standby current of VDD	EN=GND		3	10	μA
	Power-save mode current consumption	V_{EN}=3.6V, GCR.APSE=1, All LEDs off >32ms		3	10	μA
I_{ACT_VDD}	Quiescent current in active mode	V_{EN}=VDD, GCR.CHIPEN=1,		2	4	mA
		V_{EN}=VDD, GCR.CHIPEN=1, CS_MS=0xFF, CS_DSX=0xFF		10	12	mA
$I_{LEAKAGE}$	Output leakage current	V_{EN}=0V, VLEDX=5.5V		0.1	1	μA
I_{MAX}	Maximum global current of LEDX	CS_MS =0xFF, CS_DSX=0xFF BRX =0xFF	18.6	20.0	21.4	mA
I_{MATCH}	Output current match accuracy	CS_MS =0xFF, CS_DSX=0xFF BRX =0xFF	-7		+7	%
$V_{DROPOUT}$	Dropout voltage when the LED current has dropped 10%	ILEDX=20mA		120	250	mV
F_{OSC}	OSC clock frequency		14.88	16	17.12	MHz
T_{SD}	Thermal shutdown threshold			150		°C
	Thermal shutdown hysteresis			20		°C
AD, EN						
V_{IL}	Input low level	AD, EN			0.4	V
V_{IH}	Input high level	AD, EN	1.2			V
R_{ADPD}	Internal pull down resistance	AD, VDD=3.6V		400k		Ω
R_{ENPD}	Internal pull down resistance	EN, VDD=3.6V		400k		Ω
I²C Interface						
V_{OL}	Output low level	SDA, I_{OL} = 5 mA			0.1	V
V_{IH}	Input high level	SCL, SDA	1.2			V
V_{IL}	Input low level	SCL, SDA			0.4	V

I²C Interface Timing

PARAMETER		MIN	TYP	MAX	UNIT
F_{SCL}	Interface Clock frequency	-		400	kHz
$T_{HD:STA}$	(Repeat-start) Start condition hold time	0.6		-	μs
T_{LOW}	Low level width of SCL	1.3		-	μs
T_{HIGH}	High level width of SCL	0.6		-	μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time	0.6		-	μs
$T_{HD:DAT}$	Data hold time	0		-	μs
$T_{SU:DAT}$	Data setup time	0.1		-	μs
T_R	Rising time of SDA and SCL	-		0.3	μs
T_F	Falling time of SDA and SCL	-		0.3	μs
$T_{SU:STO}$	Stop condition setup time	0.6		-	μs
T_{BUF}	Time between start and stop condition	1.3		-	μs

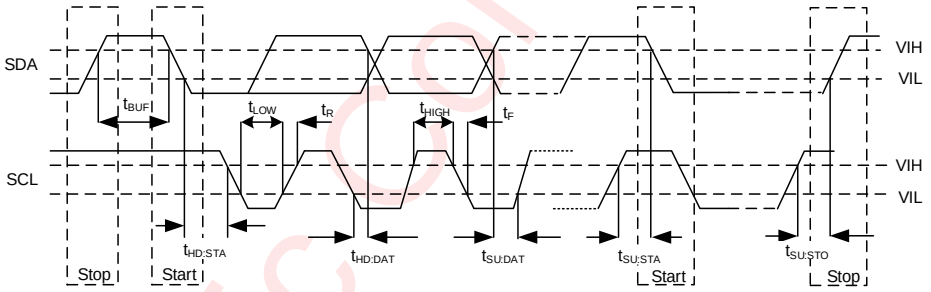


Figure 5 I²C Interface Timing

Detailed Functional Description

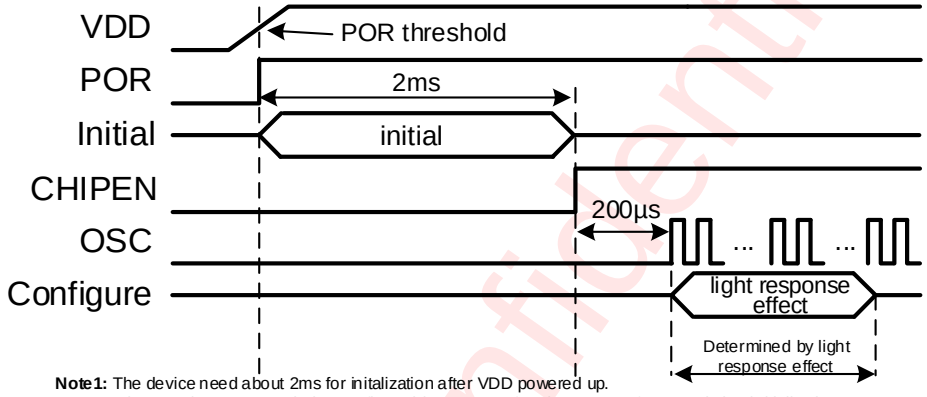
Operation Mode And Reset

Power On Reset

Upon initial power-up, the AW21036C is reset by internal power-on-reset, and all register are reset to default value, and LED driver is shut down.

Once the supply voltage VDD drops below the threshold voltage V_{POR_VDD} (2.0V), the power-on-reset will be activated to reset the device again. By reading the bit PORST of the register UVCR (address 79h), whether the device has been reset can be determined.

Below is the recommended operation timing:



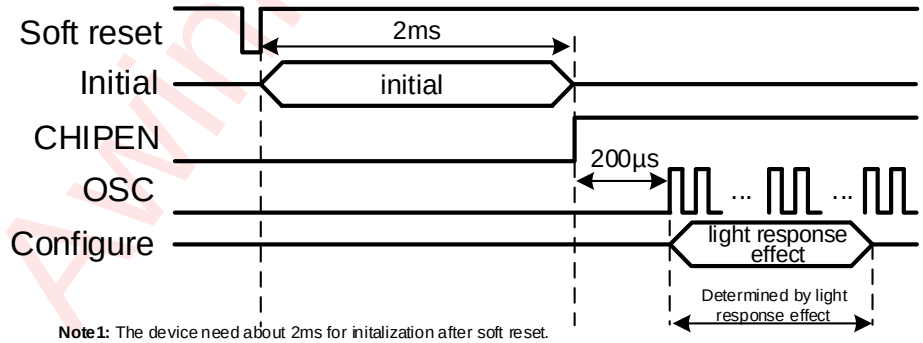
Note1: The device need about 2ms for initalization after VDD powered up.
Note2: It is strongly recommended to configure bit CHIPEN of register GCR after completing initialization.
Note3: The light response effect can be set after OSC stable that needs 200us after CHIPEN=1.

Figure 6 Power Up Timing

Software Reset

By writing 00H to register RESET (address 7Fh), the software reset is triggered. After software reset, all registers will be reset to the default value and enter into standby mode.

After the software reset command is input through I²C or power on reset, it needs to wait at least 2ms before any other I²C command can be accepted.



Note1: The device need about 2ms for initalization after soft reset.
Note2: It is strongly recommended to configure bit CHIPEN of register GCR after completing initialization.
Note3: The light response effect can be set after OSC stable that needs 200us after CHIPEN=1.

Figure 7 Software Reset Timing

Standby Mode

The AW21036C enters into standby mode after VDD powered up. In standby mode all analog blocks except POR are powered down. I²C interface is accessible and all registers can be configured.

Active Mode

When EN is in high level, and the bit CHIPEN of the register GCR (address 00h) is set to “1”, the AW21036C enters into the active mode.

Auto Power-Save Mode

The bit APSE of the register GCR (address 00h) is set to “1”, the auto power-save mode is enabled. When all LEDs are off and the value of all register BR0~BR35 are 0x00 for more than 32ms, AW21036C automatically enters into standby mode for power saving. Once writing a non-zero value into any register among BR0~BR35, the device exits power-save mode immediately.

In addition, the auto power-save mode is disabled under autonomous breathing mode.

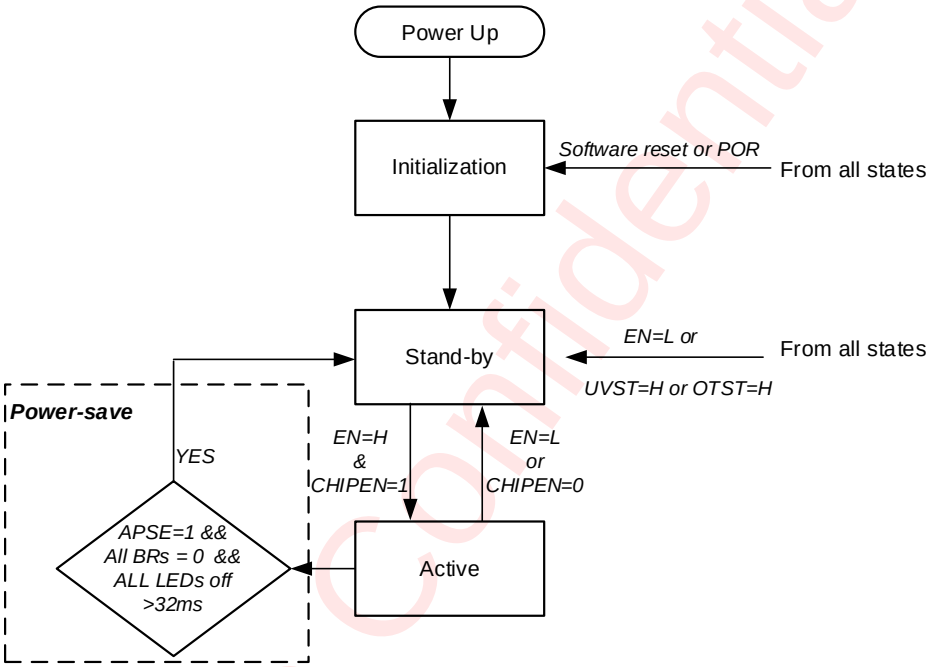


Figure 8 AW21036C Operating Mode Transition

I²C Interface

The AW21036C supports the I²C protocol. The maximum frequency supported by the I²C is 400kHz. The pull-up resistor for the SDA and SCL can be selected from 1kΩ to 10kΩ. Usually, 4.7kΩ is recommended for 400kHz I²C. The voltage from 1.8V to 3.3V is allowed for the I²C interface. Additionally, the I²C device supports continuous read and write operations.

Device Address

The I²C device address is 7-bit (A7~A1), followed by a R/W bit A0 (Read=1/Write=0). Set A0 to “0” for writing and “1” for reading. The values of bit A1 and bit A2 are depended on the connection of pin AD, there are 4 options: VDD, GND, SCL and SDA. The A7 to A3 is “01101” constantly. The device also supports using a broadcast slave address of 1Ch to access registers. All slave addresses as followed.

AD PIN	A7: A3	A2:A1	A0	Device Address	Broadcast Address
GND	01101	00	0/1	34h	1Ch
VDD		01		35h	
SCL		10		36h	
SDA		11		37h	

I²C Start/Stop

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

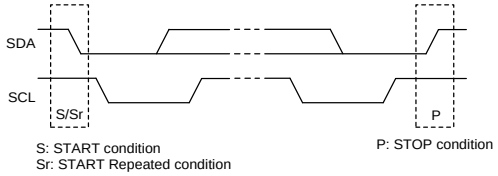


Figure 9 I²C Start/Stop Condition Timing

Data Validation

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

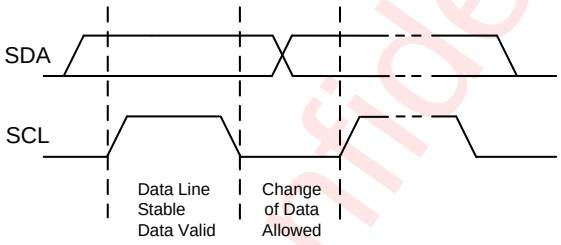


Figure 10 Data Validation Diagram

ACK (Acknowledgement)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is sent and I²C stop is not sent by master, slave device sends the next data. If ACK is not sent by master, slave device stops to send data and waits for I²C stop.

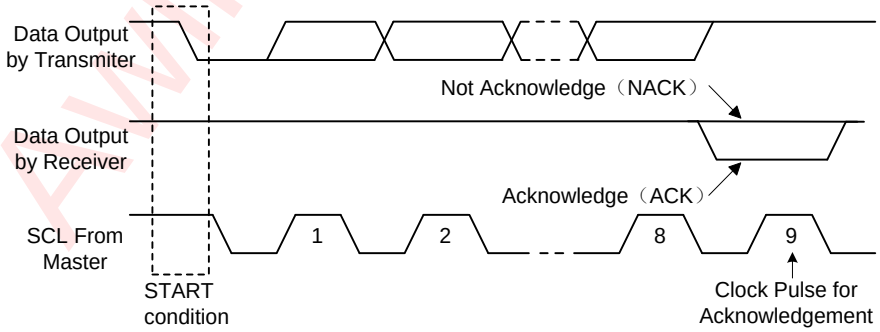


Figure 11 I²C ACK Timing

Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction.

New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The “START” signal is generated by lowering the SDA signal while the SCL signal is high.
b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).
c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends control register address (8-bit).
e) Slave sends acknowledge signal.
f) Master sends data byte to be written to the addressed register.
g) Slave sends acknowledge signal.
h) If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step f and g).
i) Master generates STOP condition to indicate write cycle end.

Figure 12 I²C Write Byte Cycle

Read Cycle

In a read cycle, the following steps should be followed:

a) Master device generates START condition.
b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).
c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends control register address (8-bit).
e) Slave sends acknowledge signal.
f) Master generates STOP condition followed with START condition or REPEAT START condition.
g) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).
h) Slave device sends acknowledge signal if the slave address is correct.
i) Slave sends data byte from addressed register.
j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.
k) If the master device generates STOP condition, the read cycle is ended.

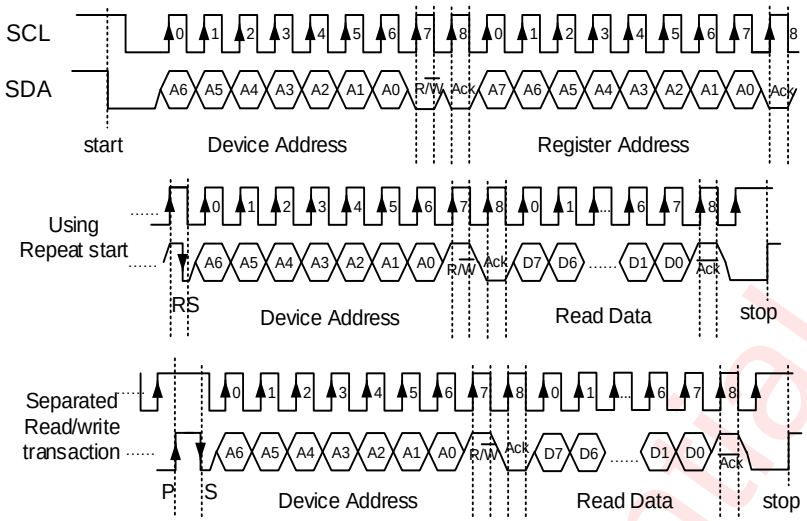


Figure 13 I²C Read Byte Cycle

Under Voltage Lock Out (UVLO)

When bit UVDIS of the register UVCR (address 79h) is set to “0”, the device monitors the voltage of VDD. If the voltage drops below threshold (2.4V typically), the bit UVST of the register UVCR (address 79h) will be set to “1”. After read-out, the register UVCR will be clear.

If both bit UVDIS and bit UVPD of the register UVCR (address 79h) is set to “0”, UVLO protection function is enabled. Once the event of under voltage occurs, the bit CHIPEN of the register GCR (address 00h) will be cleared to “0”, and then the device will enter into standby mode. If the voltage of VDD rises above the UVLO threshold and then write “1” to bit CHIPEN, the device will enter into active mode again.

By default, control bits UVDIS, UVPD are all “0”. Both UVLO monitor and protection are enabled.

Over Temperature Protection (OTP)

When bit OTDIS of the register OTCR (address 77h) is set to “0”, the over-temperature detection is enabled. Once the temperature of this device reaches 150°C, the over-temperature condition is detected, and the bit OTST of the register OTCR (address 77h) will be set to “1”. The OTST will be cleared to “0” after reading the register OTCR.

If both bit OTDIS and bit OTPD of the register OTCR (address 77h) is set to “0”, the Over-Temperature Protection (OTP) function is enabled. Once the event of over-temperature occurs, the bit CHIPEN of the register GCR (address 00h) will be cleared to “0”, and then the device will enter into standby mode. When the temperature returns below 130°C, the device will enter into active mode again after writing “1” to bit CHIPEN.

By default, control bits OTDIS and OTPD are all “0”, both OT monitor and OT protection are enabled.

LED Open/Short Detection

AW21036C supports LED open/short detection. Writing “111” into OS_EN[2:0] to enable LED open/short detection. When bit OSDM[1:0] of the register OSDCR(address 71h) is set to “11” , open detection mode is enabled, and the detection results can be read out via the registers OSST0~4 (address 72h~76h). Similarly, when set bit OSDM [1:0] of the register OSDCR (address 71h) to “10”, short detection mode is enabled, and the results also can be read out via the registers OSST0~4.

Writing 0x20 into CS_MS (address 6Eh) to enter open/short detection mode. We recommend the register BRx being set to “0xFF” of each LED when the open/short function is enabled.

Current Setting

The average output current of LED_n (n=1, 2, …, 36) can be expressed by the following formula,

$$I_{OUT(n)} = K \times \frac{V_{REXT}}{R_{EXT}} \times \frac{BR_n}{256} \qquad \text{n=1, 2, 3, …, 36}$$

Where V_{REXT}=0.4V, K=200, R_{EXT} is the value of external resistor, BR_n is 8bit individual PWM modulated current parameter.

The average output current is determined by the global current(controlled by R_{EXT}) and PWM duty cycle(controlled by BR). For example, R_{EXT}=4kΩ, BR=0xFF. The global current is 20mA, the average output current is slightly less than 20mA because the maximum PWM duty cycle(=255/256) can't reach 100%.

PWM Modulation

PWM Frequency

The PWM frequency is decided by bits CLKFRQ[2:0] in register GCR (address 00h). Following table shows the relationship of PWM frequency and the CLKFRQ[2:0]. To avoid the MLCC audible noise, it's recommended to use the PWM frequency lower than 500Hz or higher than 20kHz.

CLKFRQ[2:0]	000	001	010	011	100	101	110	111
PWM Freq. [Hz]	62k	32k	4k	2k	1k	500	244	122

Spread Spectrum

PWM is a troublesome for some application which is concerned about EMI. AW21036C has spread spectrum function to optimize the EMI performance. If bit SSE in register SSCR (address 78h) is set to "1", spread spectrum function is enabled. By setting the bit SSR in register SSCR, four spread spectrum range 5%/15%/25%/35% can be selected. The total electromagnetic emitting energy can spread into a wider range of frequency band that significantly degrades the peak energy of EMI.

Register Configuration

Register List

ADDR	NAME	W/R	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
00H	**GCR**	**W/R**	APSE	CLKFRQ			-			CHIPEN	00H
01H ~ 24H	**BR0 ~ BR35**	**W/R**	BR0~BR35								00H
49H	**UPDATE**	**W**	UPDATE								00H
4AH ~ 6DH	**CS_DSx**	**W/R**	CS_DS0~CS_DS35								00H
6EH	**CS_MS**	**W/R**	CS_MS								00H
71H	**OSDCR**	**W/R**	-				OTH	STH	OSDM		00H
72H	**OSST0**	**R**	OSST [7:0]								00H
73H	**OSST1**	**R**	OSST [15:8]								00H
74H	**OSST2**	**R**	OSST [23:16]								00H
75H	**OSST3**	**R**	OSST [31:24]								00H
76H	**OSST4**	**R**	-				OSST [35:32]				00H
77H	**OTCR**	**W/R**	TROF		TRST	OTST	OTPD	OTDIS	TRTH		00H
78H	**SSCR**	**W/R**	OS_EN			SSE	SSR		CLT		00H
79H	**UVCR**	**W/R**	REXT_ST		UVST	PORST	OCPTH	OCPD	UVPD	UVDIS	00H
7CH	**GCR4**	**-**	-	-	-	-	-	SRR	SRF		00H
7EH	**VER**	**R**	VERSION								A8H
7FH	**RESET**	**W/R**	RESET/ID								18H

Register Detailed Description

GCR: Global Control Register(Address 00H)

Bit	Symbol	R/W	Description	Default
7	APSE	RW	Auto power-saving mode enable 0: Disable 1: Enable	0
6:4	CLKFRQ	RW	OSC frequency selection 000: 16MHz 001: 8MHz 010: 1MHz 011: 512kHz 100: 256kHz 101: 125kHz 110: 62.5kHz 111: 31.25kHz	000
3:1	RESERVED	R	Reserved	0

0	CHIPEN	RW	Chip enable 0: Disable (default) 1: Enable	0

BR: BR Register(Address 01H~24H)

Bit	Symbol	R/W	Description	Default
7:0	BR	RW	Individual 8bit BR parameter for LED1~36. After configuring the BR registers, should write 0x00 to register UPDATE to update the data.	0x00

UPDATE: Update Register(Address 49H)

Bit	Symbol	R/W	Description	Default
7:0	UPDATE	W	Write 0x00 to update BR register.	0x00

CS_DSx: CS_DS Register(Address 4AH~6DH)

Bit	Symbol	R/W	Description	Default
7:0	CS_DS	RW	Current Source Channel Switch, set to 0xFF to enable.	0x00

CS_MS: CS_MS Register(Address 6EH)

Bit	Symbol	R/W	Description	Default
7:0	CS_MS	RW	Current Source Main Switch, set to 0xFF to enable. Writing 0x20 to enter open/short detection mode.	0x00

OSDCR: Open Short Detect Control Register(Address 71H)

Bit	Symbol	R/W	Description	Default
7:4	RESERVED	R	Reserved	0000
3	OTH	RW	Open threshold 0: 0.1V 1: 0.2V	0
2	STH	RW	Short threshold 0: VDD-1V 1: VDD-0.5V	0
1:0	OSDM	RW	Open short detect mode 0x: Detect disable 10: Short detect mode 11: Open detect mode	00

OSST0~3: Open/Short Status Register (Address 72H~75H)

Bit	Symbol	R/W	Description	Default
7:0	OSST	R	Open/short status of LED1~LED32 0: No open/short event detected 1: Open/short event detected	0x00

OSST4: Open/Short Status Register (Address 76H)

Bit	Symbol	R/W	Description	Default
7:4	RESERVED	R	Reserved	0000
3:0	OSST	R	Open/short status of LED33~LED36 0: No open/short detected 1: Open/short detected	0000

OTCR: Over Temperature Control Register (Address 77H)

Bit	Symbol	R/W	Description	Default
7:6	TROF	RW	Thermal roll off percentage of I_{OUT} 00: 100% 01: 75% 10: 55% 11: 30%	00
5	TRST	R	Thermal roll off status 0: None roll off 1: Roll off	0
4	OTST	R	Over-temperature status 0: None over-temperature 1: Over-temperature	0
3	OTPD	RW	Over-temperature(OT) protect disable 0: OT protect enable, when OT event occurs, device will clear GCR.CHIPEN to 0. 1: OT protect disable	0
2	OTDIS	RW	Over-temperature detect disable 0: OT detect enable, when OT event occurs, OTCR.OTST will be set. 1: OT detect disable	0
1:0	TRTH	RW	Thermal roll off threshold 00: 140°C 01: 120°C 10: 100°C 11: 90°C	00

SSCR: Spread Spectrum Control Register (Address 78H)

Bit	Symbol	R/W	Description	Default
7:5	OS_EN	RW	Writing '111' to enable LED open/short detection	000
4	SSE	RW	Spread spectrum enable 0: Disable 1: Enable	0
3:2	SSR	RW	Spread spectrum range 00: ±5% 01: ±15% 10: ±25% 11: ±35%	00
1:0	CLT	RW	Spread spectrum cycle time 00: 1980μs (default) 01: 1200μs 10: 820μs 11: 660μs	00

UVCR: UVLO Control Register (Address 79H)

Bit	Symbol	R/W	Description	Default
7:6	REXT_ST	R	R_{EXT} status 00: Normal 10: R_{EXT} is open 01: R_{EXT} is short or OCP 11: Not defined	00
5	UVST	R	UVLO status 0: No UVLO detected 1: UVLO detected	0
4	PORST	R	Power-up reset status 0: No power-on reset 1: Power-on reset (cleared after read out)	0
3	OCPTH	RW	OCP Threshold 0: 85mA 1: 55mA	0
2	OCPD	RW	OCP disable 0: Enable OCP 1: Disable OCP	0
1	UVPD	RW	UVLO protect disable 0: UVLO protect enable, when under-voltage event occurs, device will clear GCR.CHIPEN to 0. 1: UVLO protect disable	0
0	UVDIS	RW	UVLO detect disable 0: UVLO detect enable, when under-voltage event occurs, UVCR.UVST will be set. 1: UVLO detect disable	0

GCR2: Global Control Register 2(Address 7AH)

Bit	Symbol	R/W	Description	Default
7:1	RESERVED	R	Reserved	0000 000
0	RGBMD	RW	RGB configure mode enable 0: Disable 1: Enable, every 3 LEDs share a common brightness.	0

GCR4: Global Control Register 4(Address 7CH)

Bit	Symbol	R/W	Description	Default
7:3	RESERVED	R	Reserved	0000 0
2	SRR	RW	Slew rate control for LED output rising time 0: 1ns 1: 6ns	0
1:0	SRF	RW	Slew rate control for LED output falling time 00: 1ns 01: 3ns 10: 6ns 11:10ns	00

VER: Version Register (Address 7Eh)

Bit	Symbol	R/W	Description	Default
7:0	VER	R	Chip version	0xA8

RESET: Software Reset Register (Address 7FH)

Bit	Symbol	R/W	Description	Default
7:0	RESET	RW	Write 00H to the register will reset all registers to their default value. The chip ID 0x18 will be read out from the register.	0x18

Application Information

REXT

The selection of R_{EXT} determined the maximum LED1~LED36 current I_{MAX} as described in below formula (1).

$$I_{MAX} = K \times \frac{V_{REXT}}{R_{EXT}} \quad (1)$$

Where V_{REXT} = 0.4V, K = 200, the recommended minimum value of R_{EXT} is 2kΩ.

When R_{EXT} = 2kΩ, I_{MAX} = 40mA.

When R_{EXT} = 4kΩ, I_{MAX} = 20mA.

RR, RG, RB

The resistance(R_X) used for thermal reduction can be calculated according to the following formula:

$$R_X = \frac{VLED - VF_X - V_{DROPOUT}}{I_{MAX}} \quad (2)$$

VLED: LED power supply voltage.

VF_X: LED forward voltage.

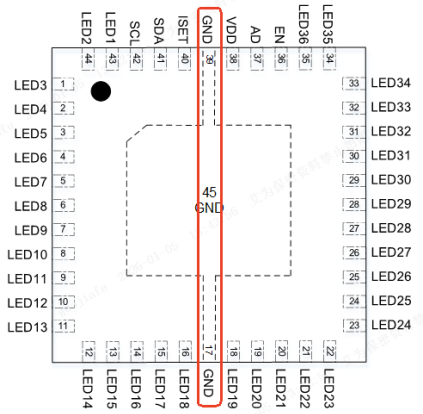
$V_{DROPOUT}$: Voltage on LEDx, recommended values is 0.5V.

I_{MAX}: Global current.

PCB Layout Consideration

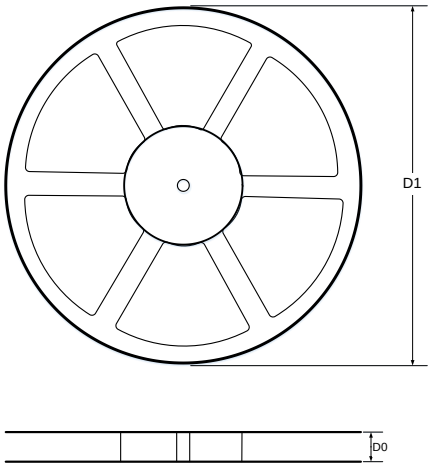
AW21036C is a 36-channel LEDs driver programmed via I²C compatible interface. When all LEDs are operating, the device power dissipation is large. To obtain the good thermal performance and avoid thermal shutdown, PCB layout should be considered carefully. Here are some guidelines:

1. The C_1, C_2, C_{LED} should be placed as close to the chip as possible.
2. The R_{EXT} should be placed as close to the chip as possible.
3. The Thermal PAD must be well connecting to the GND of the PCB, and add as many thermal vias as possible beneath the thermal PAD on the PCB for the heat conductivity of the device and PCB.
4. PIN17 and PIN39 are connected on lead frame of package. It is recommended that solder mask opening on the GND trace inside AW21036 to facilitate sufficient connection between IC and the PCB during soldering.

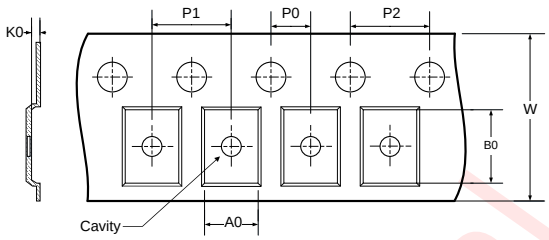


Tape And Reel Information

REEL DIMENSIONS

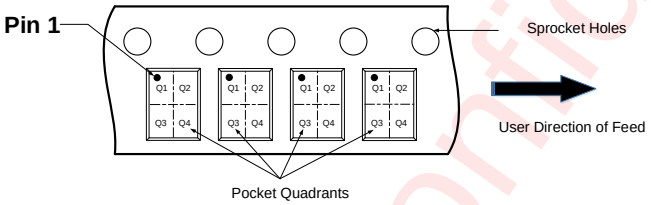


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

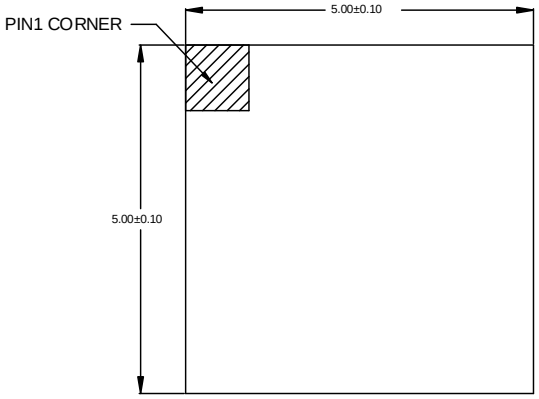


DIMENSIONS AND PIN1 ORIENTATION

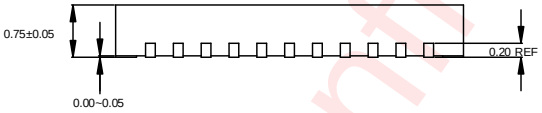
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	5.3	5.3	1.1	2	8	4	12	Q1

All dimensions are nominal

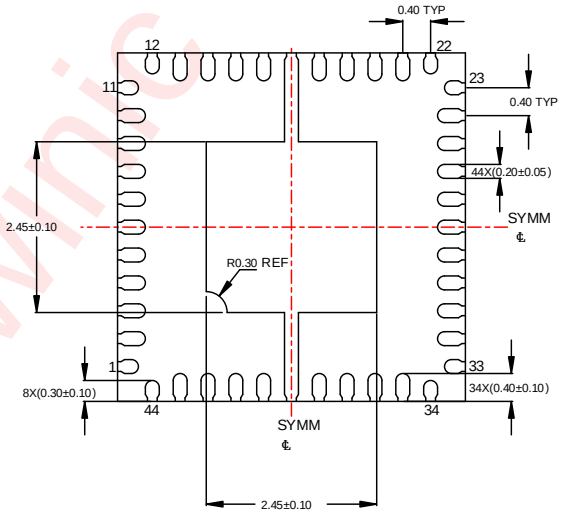
Package Description



Top View



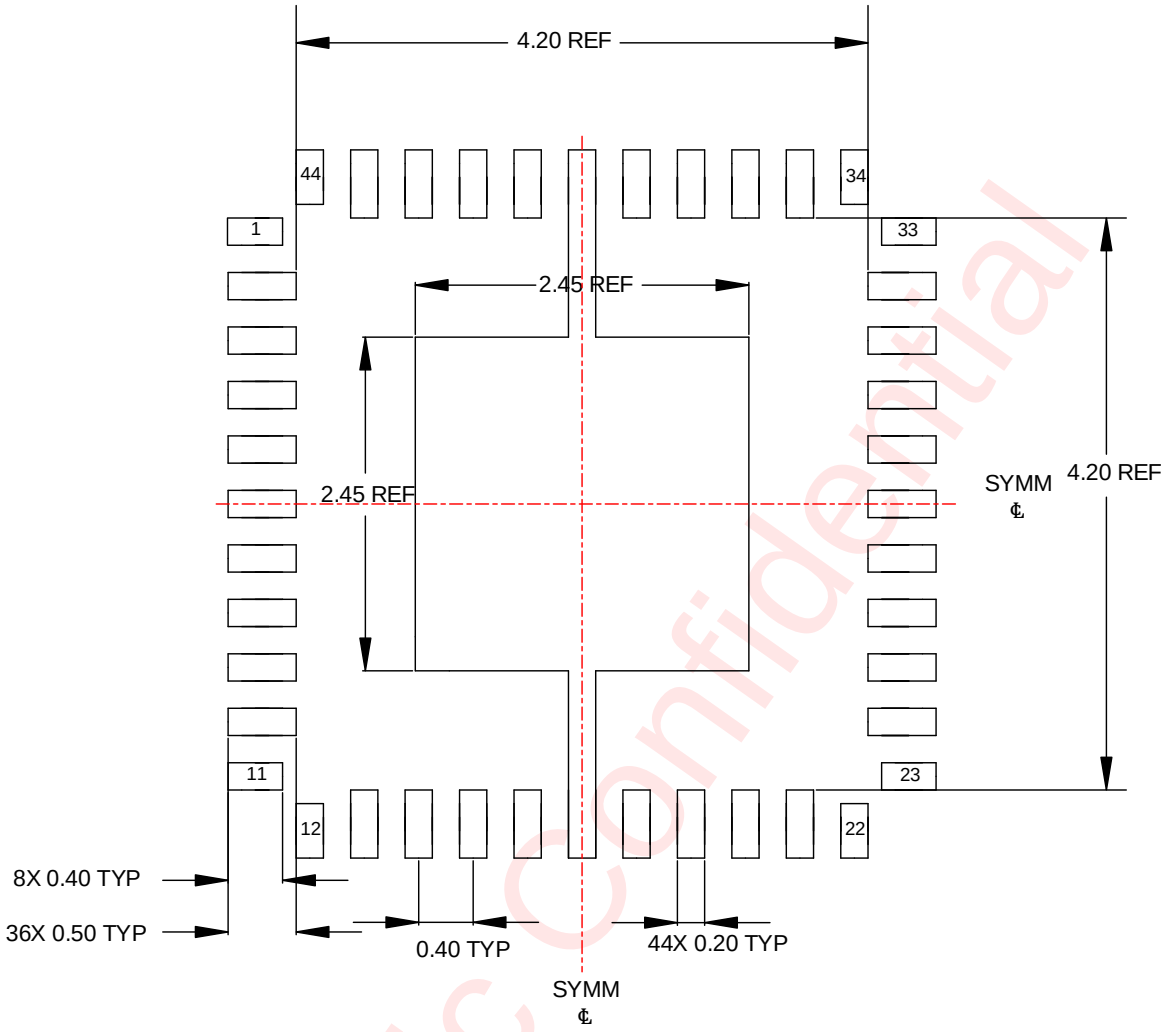
Side View

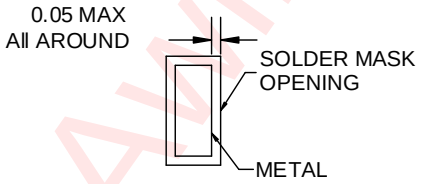


Bottom View

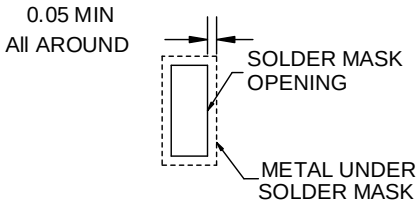
Unit: mm

Land Pattern Data





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Dec.2025	Officially released

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