

380nA,Rail-to-Rail I/O,5.5V Operational Amplifier

Features

- Wide Supply Voltage Range:1.4V ~ 5.5V
- Low Input Offset Voltage: $\pm 1.5\text{mV}(\text{MAX})$
- Offset Voltage Temperature Drift: $1.4\ \mu\text{V}/^\circ\text{C}$
- Slew Rate: 1.5V/ms
- Low Input Bias Current: $\pm 1\text{pA}$
- Low Quiescent Current: 380nA/CH
- No Phase Reversal
- Rail-to-Rail Input and Output
- Bandwidth: 8KHz
- Sink and Source Current Capability: 12mA
- Operating Temperature Range: -40°C to 125°C

Applications

- Wearable Devices
- Smoke Alarm
- Motion Detector with PIR Sensor
- Gas Detectors

General Description

The AWS79552 is a ultra-low power (380nA), low-voltage (1.4V to 5.5V) operational amplifiers with rail-to-rail input and output swing capabilities, which makes it ideal to low power consumption applications.

The AWS79552 is unity-gain stable, and feature a 8kHz gain-bandwidth product, which is designed to provide optimal performance in low-frequency systems.

The AWS79552 provides an appropriate solution for space-constrained applications such as battery powered devices, wearable electronics, and personal electronics where minimum PCB footprint is required.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AWS79552DNR	DFN2×2-8L	2mm × 2mm

Typical Application Circuit

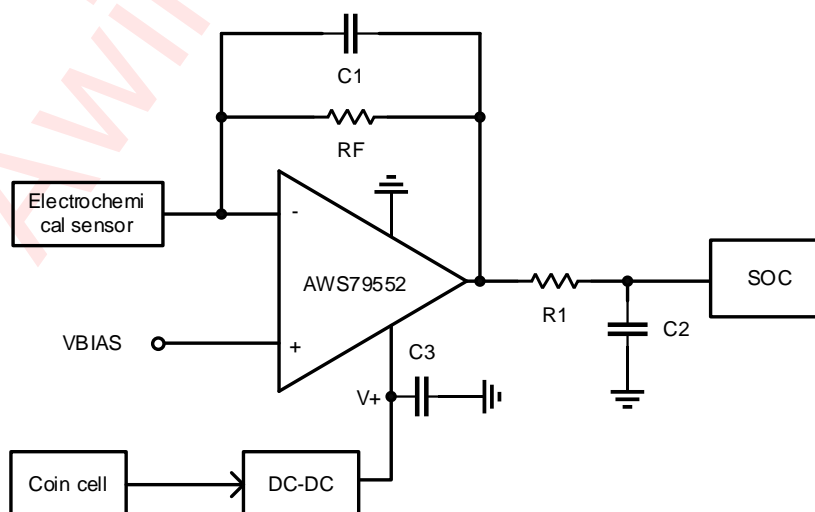


Figure 1 Typical Application of AWS79552

Pin Configuration And Top Mark

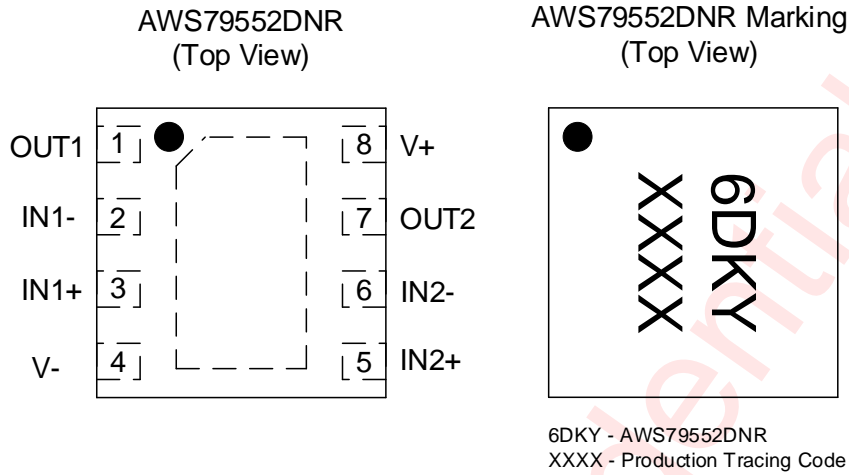


Figure 2 Pin Configuration of AWS79552

Pin Definition

PIN		DESCRIPTION
NAME	DFN2*2-8L	
OUT1	1	Channel 1 output
IN1-	2	Channel 1 inverting input
IN1+	3	Channel 1 noninverting input
V-	4	Negative (low) supply or ground (for single-supply operation)
IN2+	5	Channel 2 noninverting input
IN2-	6	Channel 2 inverting input
OUT2	7	Channel 2 output
V+	8	Positive (high) supply

Functional Block Diagram

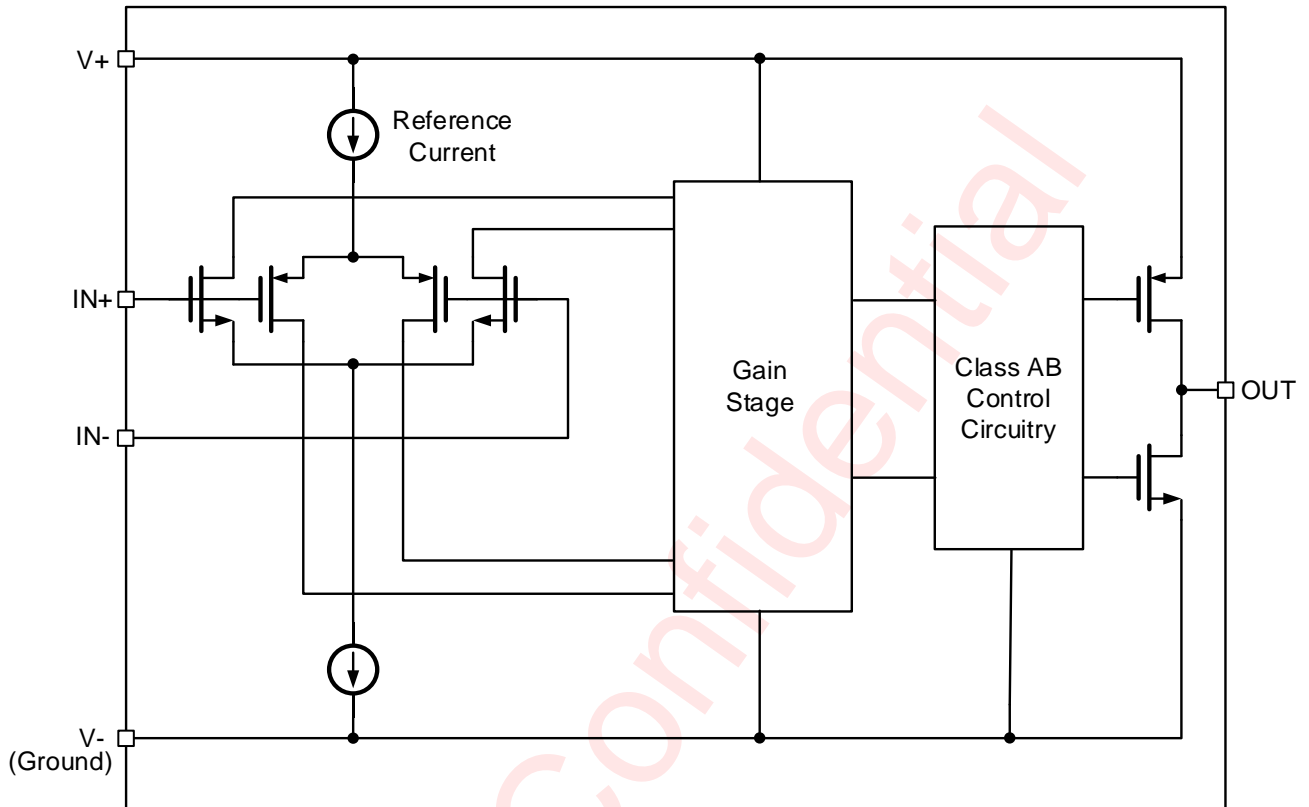


Figure 3 Functional Block Diagram

Typical Application Circuits

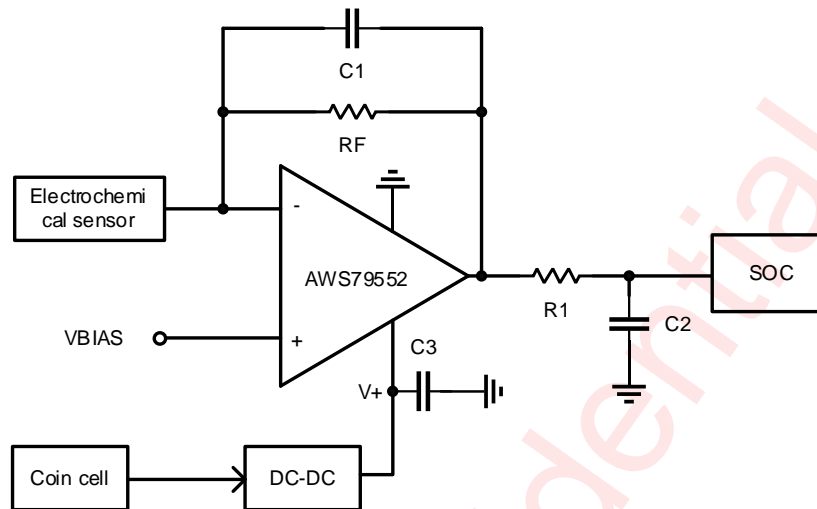


Figure 4 AWS79552 Application Circuit

- **Notice for typical application circuits:**

1. Bypass capacitors C₁/C₂ are used to reduce the coupled noise by providing a low-impedance path to ground. So low-ESR, 0.1μF ceramic bypass capacitors are necessary between each supply pin and ground, placed close to the device, but far away from input traces. If negative supply is connected to GND, then negative supply to GND can be disconnected to bypass ceramic.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWS79552DNR	-40°C ~ 125°C	DFN 2X2-8L	6DKY	MSL1	ROHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings (NOTE1)

PARAMETERS		RANGE
Supply voltage, $V_S = (V+) - (V-)$		-0.3V to 6.0V
Signal input pins	Common-mode voltage (NOTE 2)	(V-) - 0.3V to (V+) + 0.3V
	Differential voltage (NOTE 2)	(V-) to (V+)
	Current (NOTE 2)	-10mA to 10mA
Output short-circuit (NOTE 3)		Continuous
Operating free-air temperature range T_A		-40°C to 125°C
Maximum operating junction temperature T_{JMAX}		150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should be within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Input pins are diode-clamped to each power supply. Input signals that may extend more than 0.5V beyond the supply rails must be current limited to 10mA or less.

NOTE3: A heat sink may be required to keep the junction temperature below the absolute maximum.

ESD Rating and Latch Up

PARAMETERS	VALUE	UNIT
HBM (Human Body Model) (NOTE 4)	±2.5	kV
CDM (NOTE 5)	±1.0	kV
Latch-Up (NOTE 6)	+IT: 200 -IT: -200	mA

NOTE4: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2024

NOTE5: Test method: ESDA/JEDEC JS-002-2025

NOTE6: Test method: JESD78F.02

Electrical Characteristics

Unless otherwise noted, $V_S = (V_+) - (V_-) = 1.8V$ to $5.5V$ ($\pm 0.9V$ to $\pm 2.75V$), $R_L = 10M\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, typical values are at $V_S = 5V$ and $T_A = 25^\circ C$.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	$V_S = 5V$	-1.5	0.025	1.5	mV
dV_{OS}/dT	Input offset voltage drift	$T_A = -40^\circ C$ to $125^\circ C$		1.4		$\mu V/^\circ C$
PSRR	Power-supply rejection ratio	$V_S = 1.8V$ to $5.5V$, $V_{CM} = 0.5V$	90	105		dB
INPUT BIAS CURRENT						
I_B	Input bias current	$V_{CM} = V_S/2$		± 1		pA
I_{OS}	Input offset current	$V_{CM} = V_S/2$		± 1		pA
NOISE						
E_N	Input voltage noise (peak-to-peak)	$f = 0.1Hz$ to $10Hz$, $V_S = 5.5V$		5.2		μV_{PP}
e_N	Input voltage noise density	$f = 100Hz$, $V_S = 5V$		270		nV/\sqrt{Hz}
		$f = 1kHz$, $V_S = 5V$		290		
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	No phase reversal, rail-to-rail input	(V-)		(V+)	V
CMRR	Common-mode rejection ratio	$(V_-) + 0.1V < V_{CM} < (V_+) - 0.9V$, $V_S = 3.3V$	90	105		dB
		$(V_-) + 0.1V < V_{CM} < (V_+) - 0.1V$, $V_S = 3.3V$	65	80		
POWER SUPPLY						
V_S	Specified voltage range		1.4		5.5	V
I_Q	Quiescent current per channel	$V_S = 5.5V$, $I_O = 0A$	300	380	600	nA
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	$V_S = 5.5V$, $R_L = 100k\Omega$, $(V_-) + 0.3V < V_O < (V_+) - 0.3V$	115	135		dB
		$V_S = 5.5V$, $R_L = 10M\Omega$, $(V_-) + 0.3V < V_O < (V_+) - 0.3V$	120	160		dB
FREQUENCY RESPONSE CHARACTERISTICS						
GBP	Gain-bandwidth product	$V_S = 5V$, $G = +1$		8		KHz
ϕ_m	Phase margin	$V_S = 5V$, $G = +1$		56		$^\circ$

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
SR	Slew rate	$V_S = 5V, G = +1, SR+$		1.5		V/ms
		$V_S = 5V, G = +1, SR-$		2.1		V/ms
OUTPUT CHARACTERISTICS						
V_{OP}	Voltage output swing from positive supply rail	$V_S = 5.5V, R_L = 100k\Omega$		3	5.5	mV
V_{ON}	Voltage output swing from negative supply rail	$V_S = 5.5V, R_L = 100k\Omega$		3.4	6	mV
ISC	Short-circuit current per channel	$V_S = 5.0V, ISC+$		12.5		mA
		$V_S = 5.0V, ISC-$		13.9		
		$V_S = 1.4V, ISC+$		0.43		
		$V_S = 1.4V, ISC-$		0.64		

Typical Characteristics

At $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{V}$, $V_- = -2.75\text{V}$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, $R_L = 100\text{k}\Omega$ connected to $V_S/2$ unless otherwise noted.

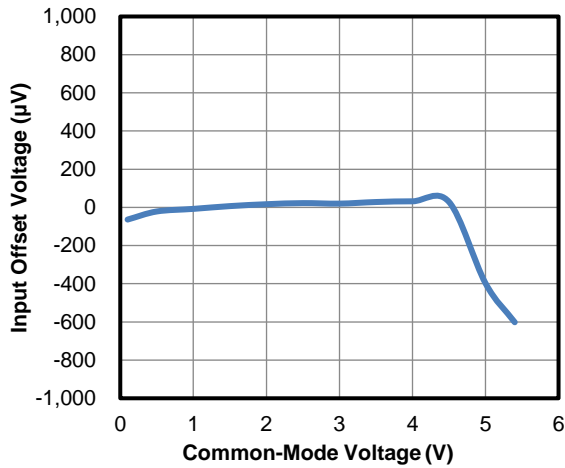


Figure 5 Input Offset Voltage vs. V_{CM}

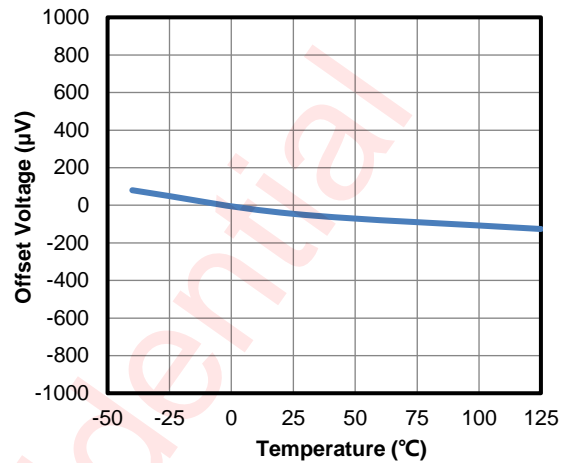


Figure 6 Input Offset Voltage vs. Temperature

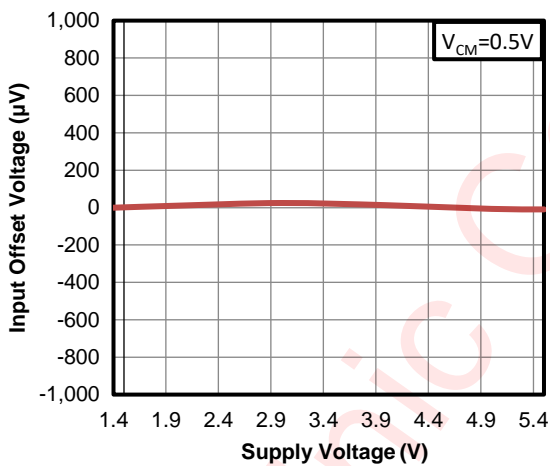


Figure 7 Offset Voltage vs. Supply Voltage

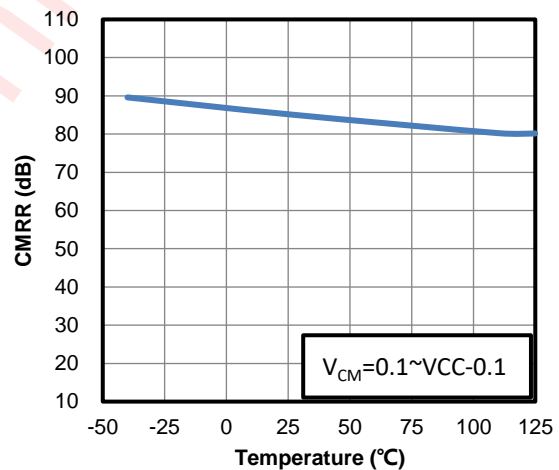


Figure 8 CMRR vs. Temperature

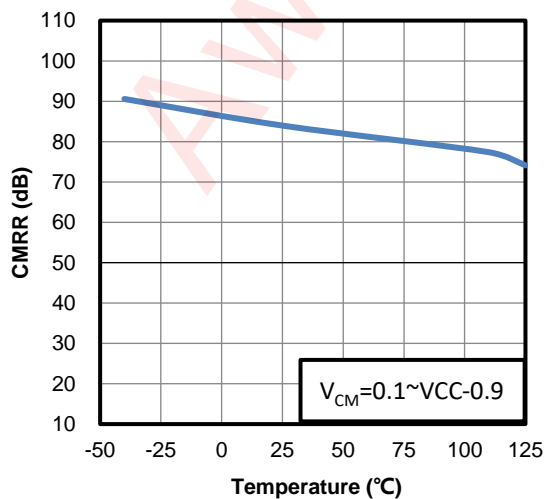


Figure 9 CMRR vs. Temperature

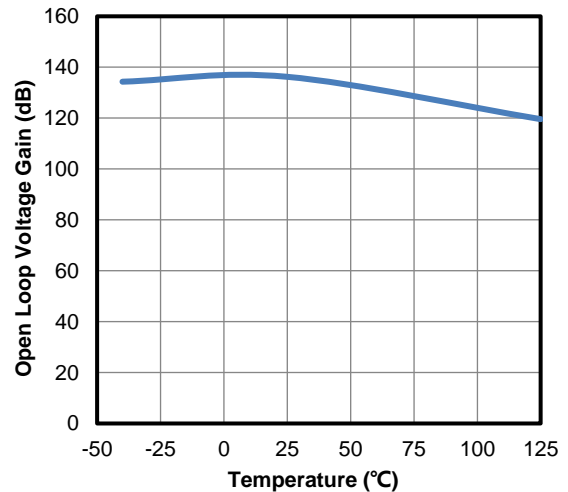


Figure 10 Open Loop Voltage Gain vs. Temperature

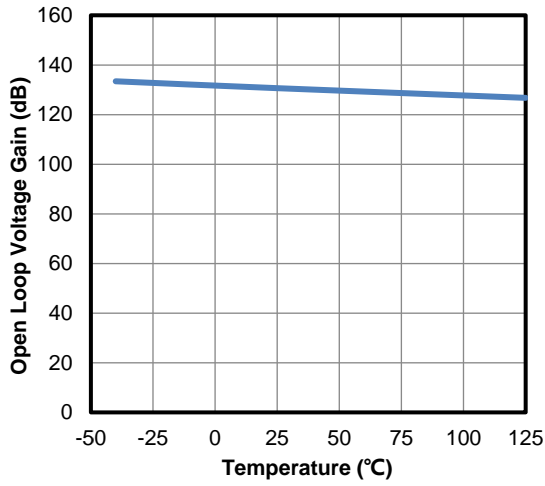


Figure 11 Open Loop Gain vs. Temperature

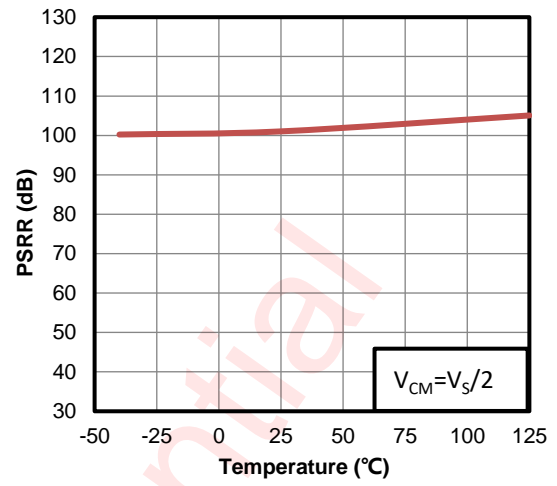


Figure 12 PSRR vs. Temperature

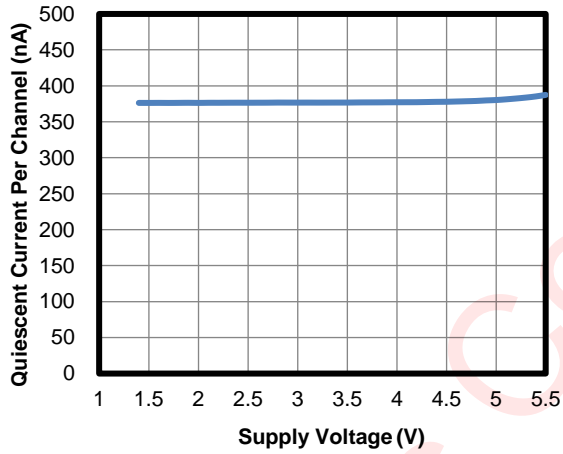


Figure 13 IQ vs. Supply Voltage

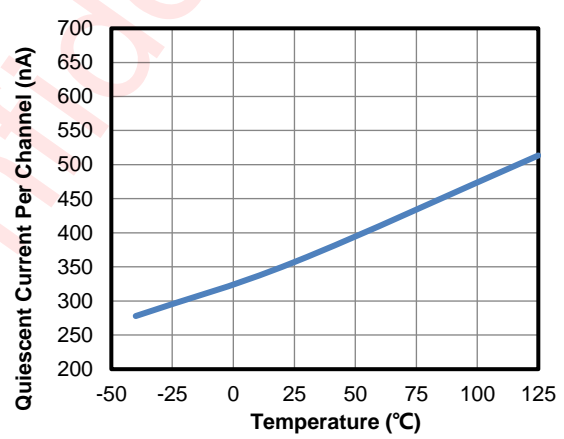


Figure 14 IQ vs. Temperature

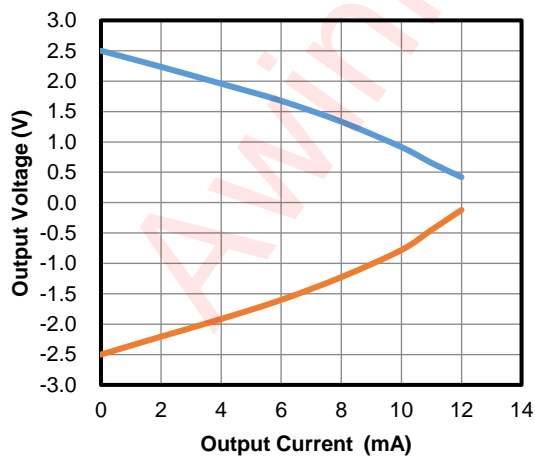


Figure 15 Output Voltage vs. Output Current

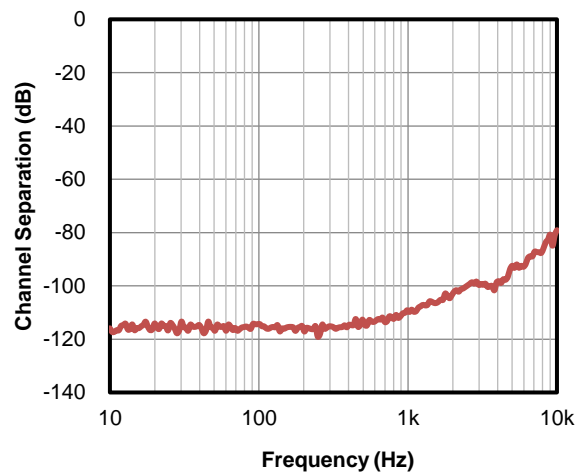


Figure 16 Channel Separation vs. Frequency

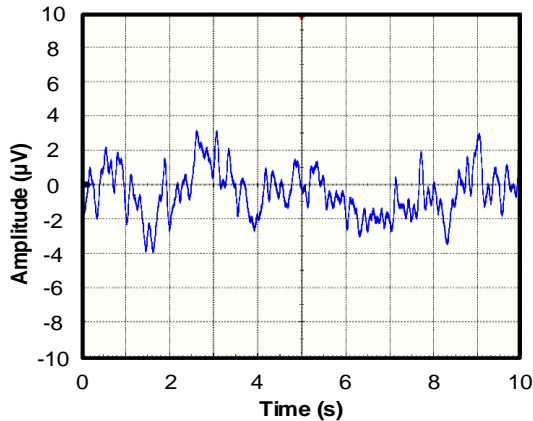


Figure 17 0.1-Hz to 10-Hz Integrated Voltage Noise

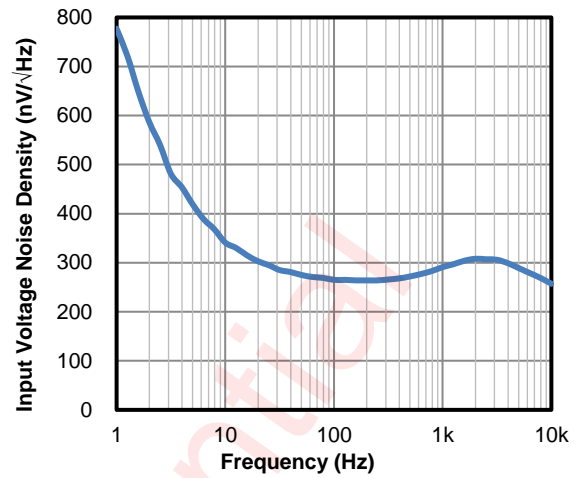


Figure 18 Voltage Noise Density vs. Frequency

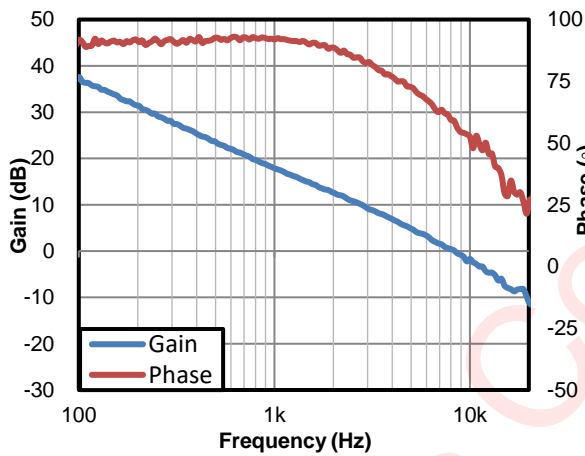


Figure 19 AoL and Phase vs. Frequency

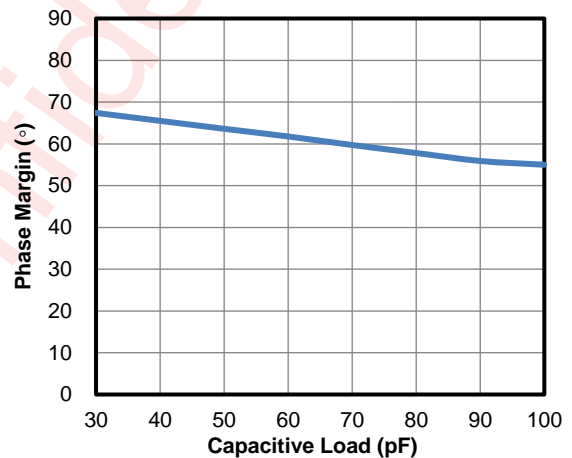


Figure 20 Phase Margin vs. Capacitive Load

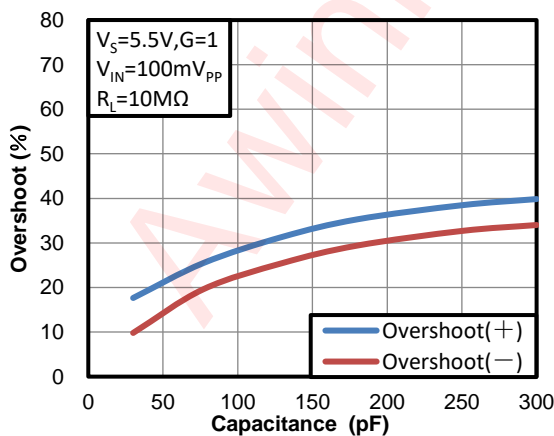


Figure 21 Small Signal Overshoot vs. CL

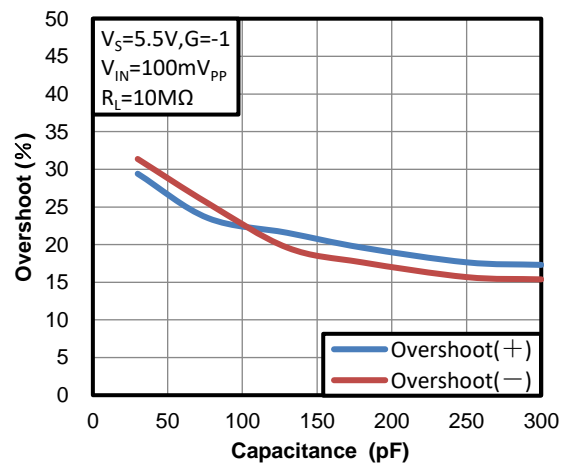


Figure 22 Small Signal Overshoot vs. CL

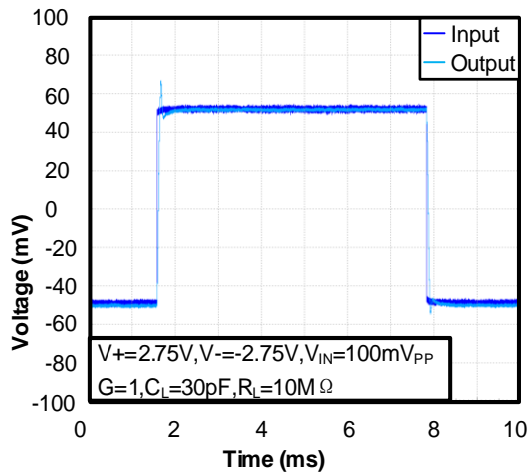


Figure 23 Small Signal Step Response

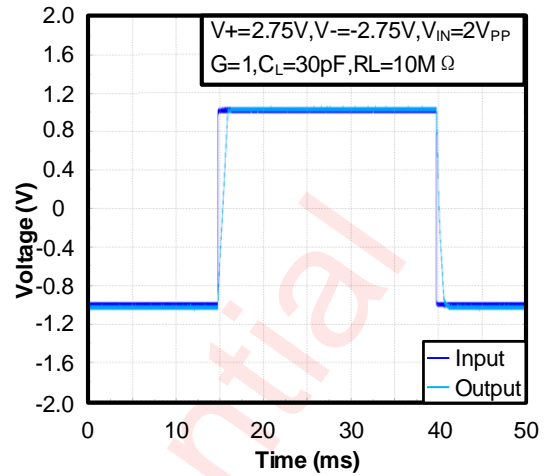


Figure 24 Large Signal Step Response

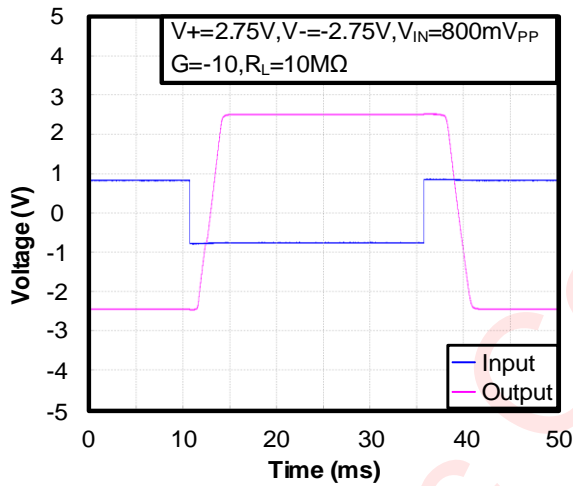


Figure 25 Overload Recovery

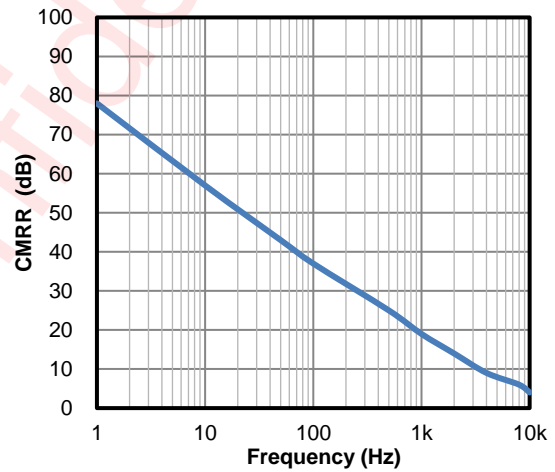


Figure 26 CMRR vs. Frequency

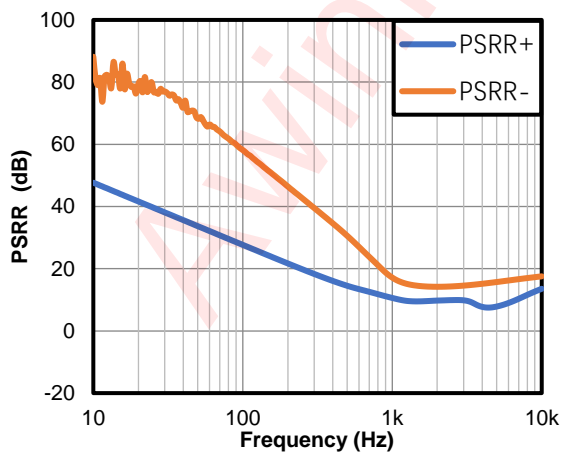


Figure 27 PSRR vs. Frequency

Detailed Functional Description

The AWS79552 is a ultra-low power, low-voltage, CMOS operational amplifier with rail-to-rail input and output swing capabilities, while drawing 380nA per channel (typical) quiescent current. The device can be unity-gain stable with power supply voltages from 1.4V to 5.5V, which makes it ideal for a wide range of general-purpose applications.

Rail-to-Rail Input

When the input voltage is close to $V+$, op-amps with a differential input pair composed of P-channel MOSFETs do not provide a normal output, because a current source enters the linear region and gain is reduced. Similarly, op-amps with a differential input pair composed of N-channel MOSFETs do not provide a normal output when the input voltage is close to $V-$. The input voltage range of the AWS79552 can be as high as $(V+)$ or as low as $(V-)$ within the full supply voltage range of 1.8V ($\pm 0.9V$) to 5.5V ($\pm 2.75V$). This performance is achieved by using an N-channel input differential pair in parallel with a P-channel differential pair. When input voltage is close to the positive rail, typically $(V+) - 0.6V$ to $(V+)$, the N-channel pair is active, whereas the P-channel pair is active for inputs from $(V-)$ to approximately $(V+) - 0.6V$. Both of the input pairs are on when the input voltage is between typically $(V+) - 0.7V$ to $(V+) - 0.4V$, which is usually called the transition region. Within this transition region, PSRR, CMRR, offset voltage, and THD can degrade compared to device operation outside this region. Furthermore, the transition region can range from $(V+) - 0.9V$ to $(V+) - 0.5V$ on the low end, and up to $(V+) - 0.6V$ to $(V+) - 0.2V$ on the high end with process variations.

Rail-to-Rail Output

A class-AB output stage with common-source transistors achieves full rail-to-rail output swing capability. Different load conditions change the ability of the amplifier to swing close to the rails. The AWS79552 output stage can drive up to a 100k Ω load and still swing to within 3mV of the supply rails. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.3V beyond either supply, otherwise current will flow through these diodes.

The rail-to-rail output stage of the amplifier can be modeled as a current source when driving the load toward $V+$, and as a current sink when driving the load toward $V-$. The limit of this current source/sink varies with supply voltage. The maximum output current is a function of total supply voltage. The output current capability increases as the supply voltage to the amplifier increases. Attention must be paid to keep the junction temperature of the op-amp below 150°C when the output is in continuous short-circuit.

Phase Reversal Protection

Many op amps exhibit a phase reversal when the input is driven beyond its specified input common-mode range, causing the output to reverse into the opposite rail. This condition is most often encountered in noninverting circuits. The AWS79552 has internal phase-reversal protection, therefore, input signals beyond the rails do not cause phase reversal. This performance is shown in Figure 28.

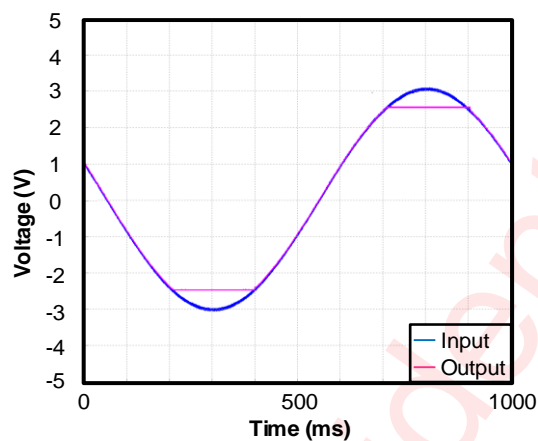


Figure 28 No Phase Reversal

PCB Layout Consideration

For the optimal performance of the device, good PCB layout practices are needed, here are some guidelines:

1. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground. So low-ESR, 0.1 μF ceramic bypass capacitors are necessary between each supply pin and ground, placed close to the device, but far away from input traces.
2. R_i is a balance resistor equals to $R_G \parallel R_F$ to reduce the influence of the input bias current on R_G and R_F , which can be shorted when unnecessary.
3. Separate grounding for analog and digital portions of circuitry for better noise suppression. Devote one or more layers on multilayer PCBs to ground planes, which help distribute heat and reduces EMI noise.
4. Run the input traces far away from the V_s supply or output traces to reduce the parasitic coupling. If not, cross these sensitive traces at a 90 degree instead of being parallel with the noisy trace.
5. The input traces are the most sensitive part of the circuit, so keep the length of input traces as short as possible. Place the external resistors and capacitors as close to device as possible, especially the R_F and R_G should be close to the inverting input to minimize the parasitic capacitance.
6. In differential applications, the trace of the inverting input and the non-inverting input should be symmetrical including the same layer, same length, same width and same line spacing.
7. Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process.

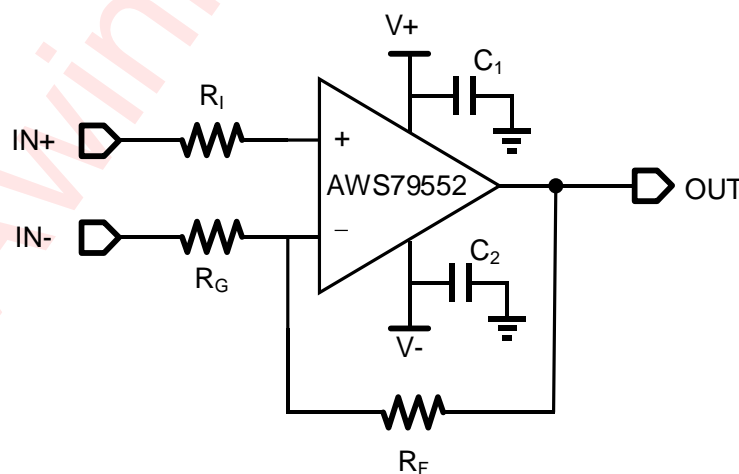


Figure 29 AWS79552 Schematic Example

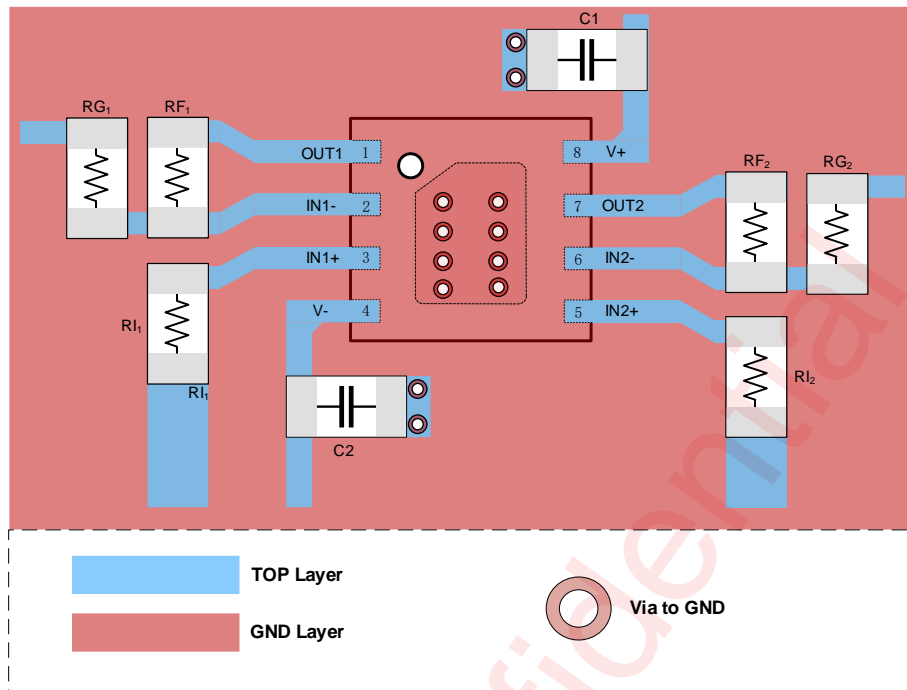


Figure 30 AWS79552 Layout Example

PCB Surface Leakage Current

In high precision applications where input bias current is critically concerned, the leakage current on PCB surface caused by dust or humidity may badly reduce the output accuracy. In this case, a multi-layer PCB is recommended for routing the input traces under the PCB surface. In addition, the usage of a guard ring can significantly reduce the leakage current to sensitive node. A conductive ring surrounding the inputs should be connected to a low impedance node with the same voltage as the inputs, so this ring will absorb the leakage current from high voltage nodes around the inputs.

For non-inverting gain application, connect the IN+ to the input with traces not touching the PCB surface, for example, routing in second layer in Figure 31. Then surround the IN+ pin with a guard ring which is connected to IN-, thus biasing the guard ring with the same voltage of the common mode input voltage.

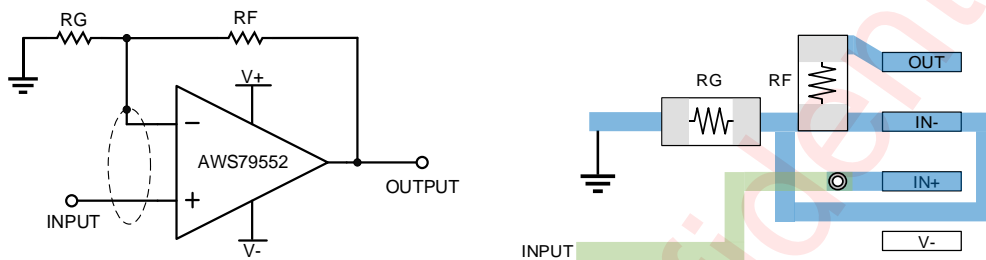


Figure 31 Non-inverting Gain Application Schematic and Layout Example

Similarly, for inverting gain application, connect the IN- to the input with traces not touching the PCB surface, for example, striding over with the input resistor in Figure 32. Then surround the IN- pin with a guard ring which is connected to IN+, thus biasing the guard ring with the reference voltage of AWS79552.

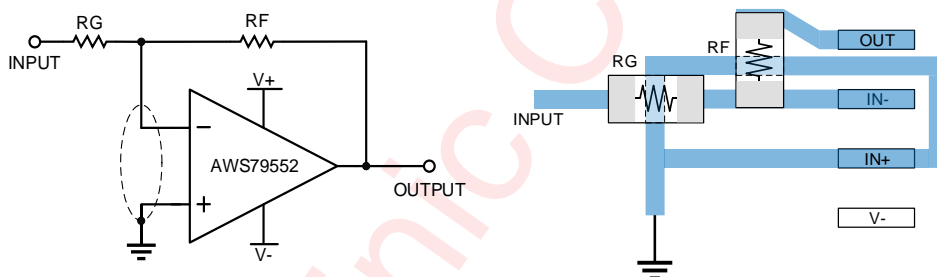
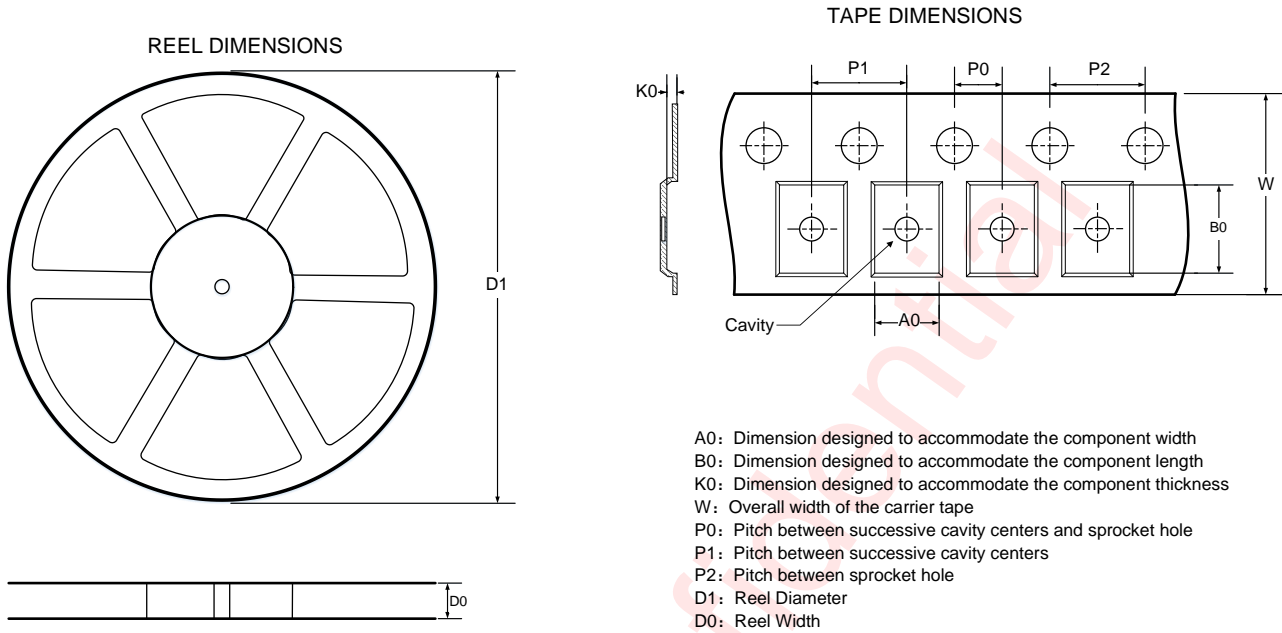
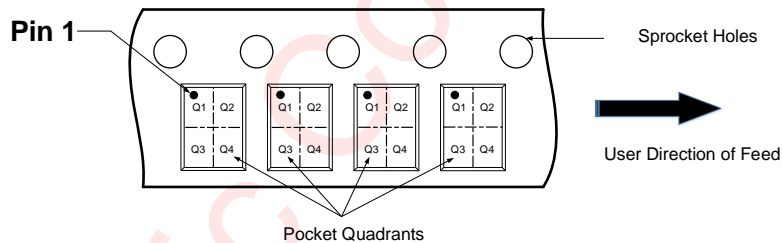


Figure 32 Inverting Gain Application Schematic and Layout Example

Tape And Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



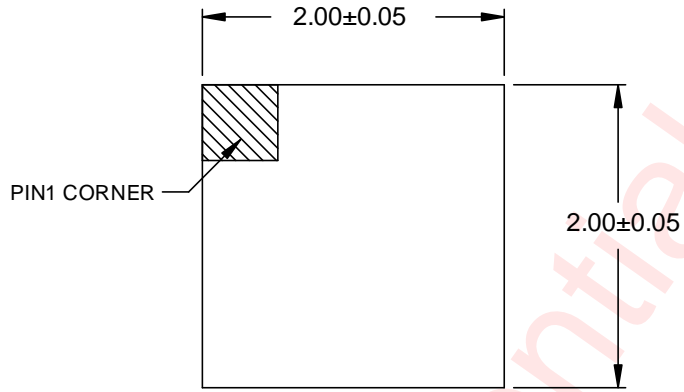
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

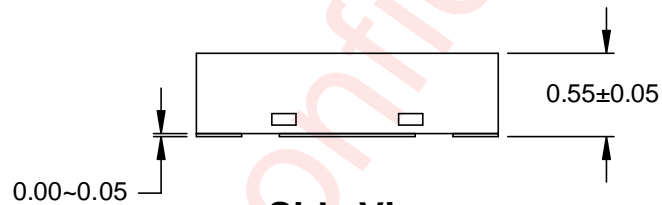
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178.00	8.40	2.20	2.20	0.75	2.00	4.00	4.00	8.00	Q1

All dimensions are nominal

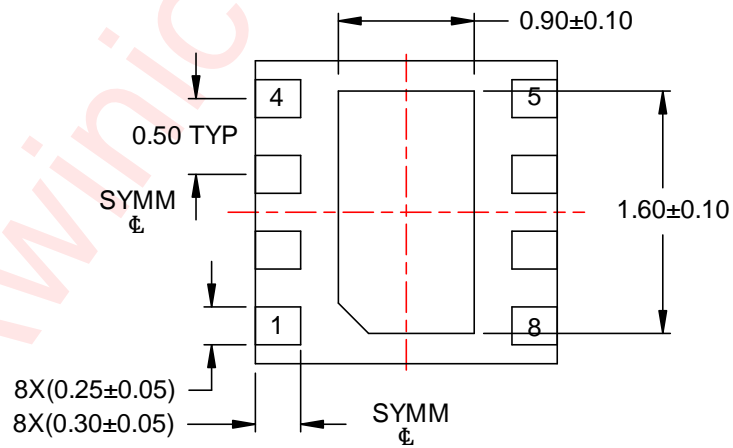
Package Description



Top View



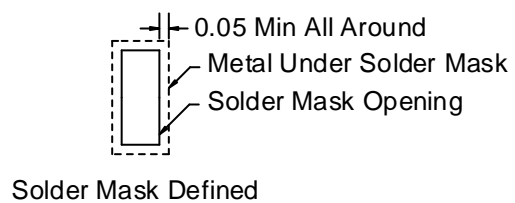
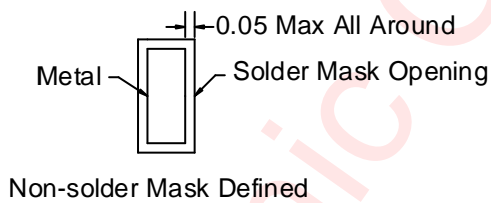
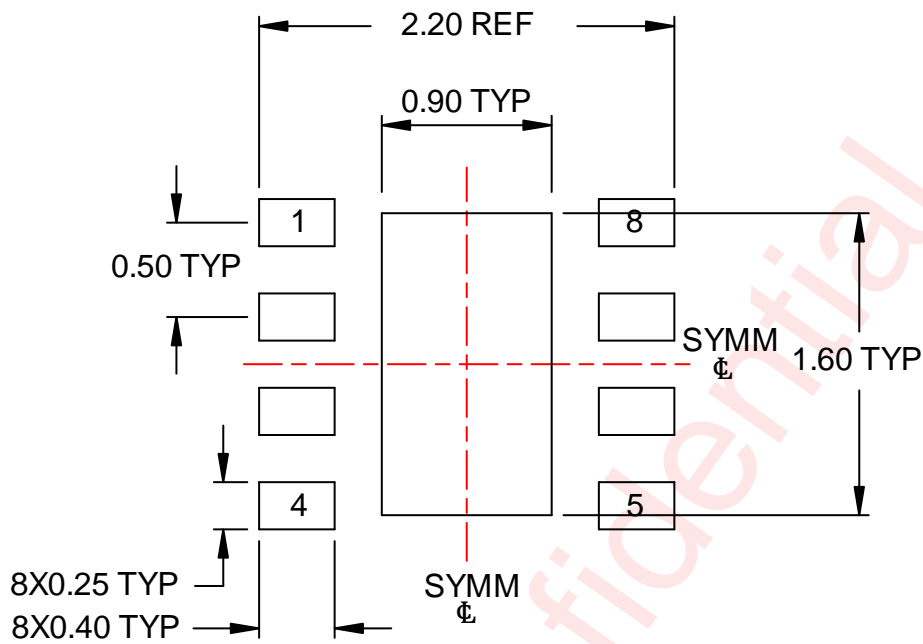
Side View



Bottom View

Unit:mm

Land Pattern Data



Unit: mm

Revision History

Version	Date	Change Record
V1.0	Dec. 2025	Official released

Awinic Confidential

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