10-bit DAC Bi-Directional VCM Auto-Focus Driver

Features

- Power Supply
  - 2.3V to 3.6V power supply
  - Support Power On Reset(POR)
  - Support Power Down(PD) mode
- Support Automatic Static Address Recognition Up to 2 Chips
- Built-In Digital-to-Analog Convertor
  - 10-bit resolution DAC
  - bi-directional
- Adjustable Output Current
  - Default current ±100mA/±130mA
  - The current range can be configured by register
- Fast Settling Function
  - Support LSC(Linear Slope Control) /VRC(VCM Ringing Control) mode
- 2-Wire I²C Serial Interface
  - 1.2V/1.8V interface available
  - Support I2C Frequency Up to 3.4MHz
- Package Dimension
  - Small 0.4mm pitch WLCSP 0.59mm x 0.99mm x 0.265mm -6B

General Description

The AW86016S is a bi-directional voice coil motor driver chip, which contains a 10-bit DAC. The operating voltage is from 2.3V to 3.6V. While the maximum output current is totally adjustable by register setting.

The AW86016S is controlled through the I²C serial interface, and its operating frequency can reach up to 3.4MHz. The device address of the chip is default 0x18(7-bit 0x0C).

The AW86016S contains Linear Slope Control mode and VCM Ringing Control mode etc., which allow programmable configuration of output current waveform to minimize mechanical vibration for fast settling, and can be suitable for different types of voice coil motors.

The AW86016S contains power on reset circuit and power down function. The reset circuit ensures that the digital circuit works well when supply power up. The supply current consumption less than 1μA in Power Down mode.

The AW86016S can be used for auto focus applications in mobile cameras, digital still cameras, camcorders and action cameras etc.

Applications

- Mobile camera
- Digital still camera
- Camcorder
- Security camera
- Web camera
- Nano actuator

Pin Configuration And Top Mark

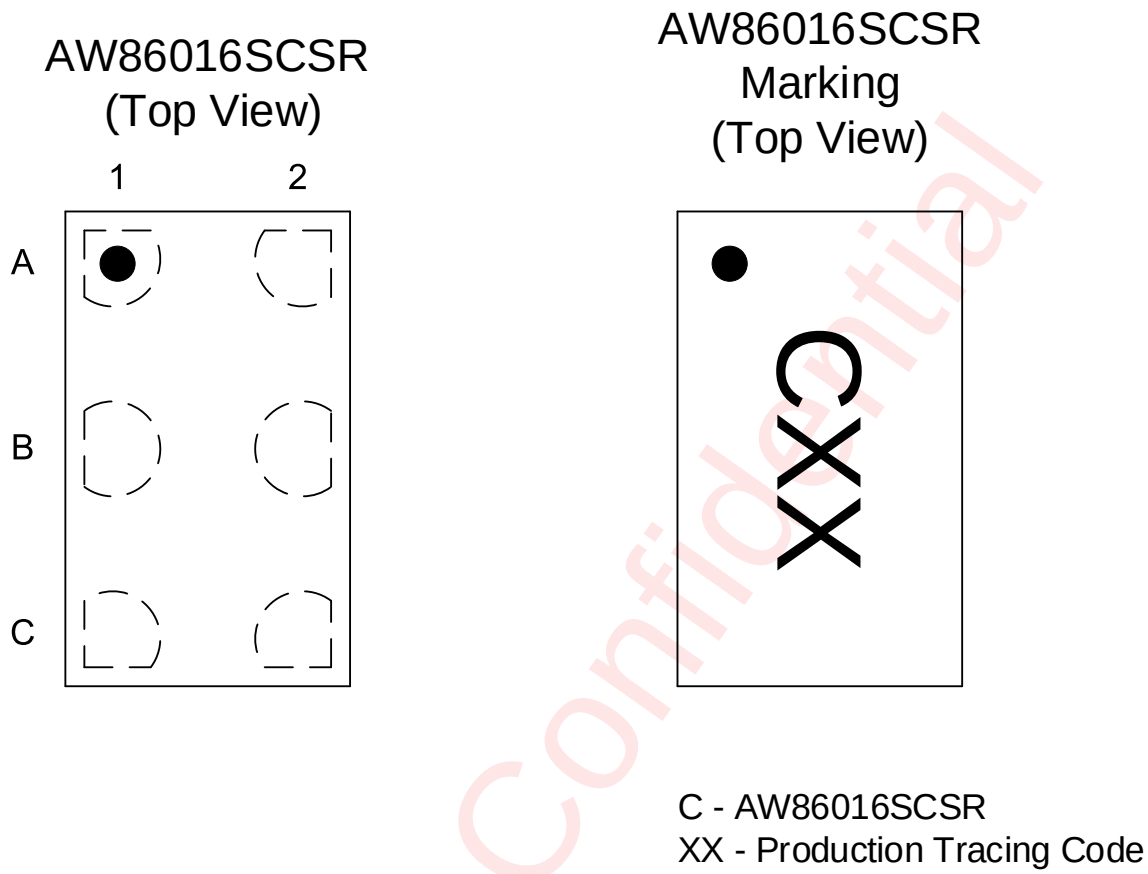


Figure 1 AW86016SCSR Pin Configuration and Top Mark

Pin Definition

No.	Name	I/O	Description
A1	GND	-	Ground
A2	VDD	-	Supply Voltage
B1	OUTN	out	H bridge negative output
B2	OUTP	out	H bridge positive output
C1	SDA	inout	I²C interface data input/output
C2	SCL	in	I²C interface clock input

Functional Block Diagram

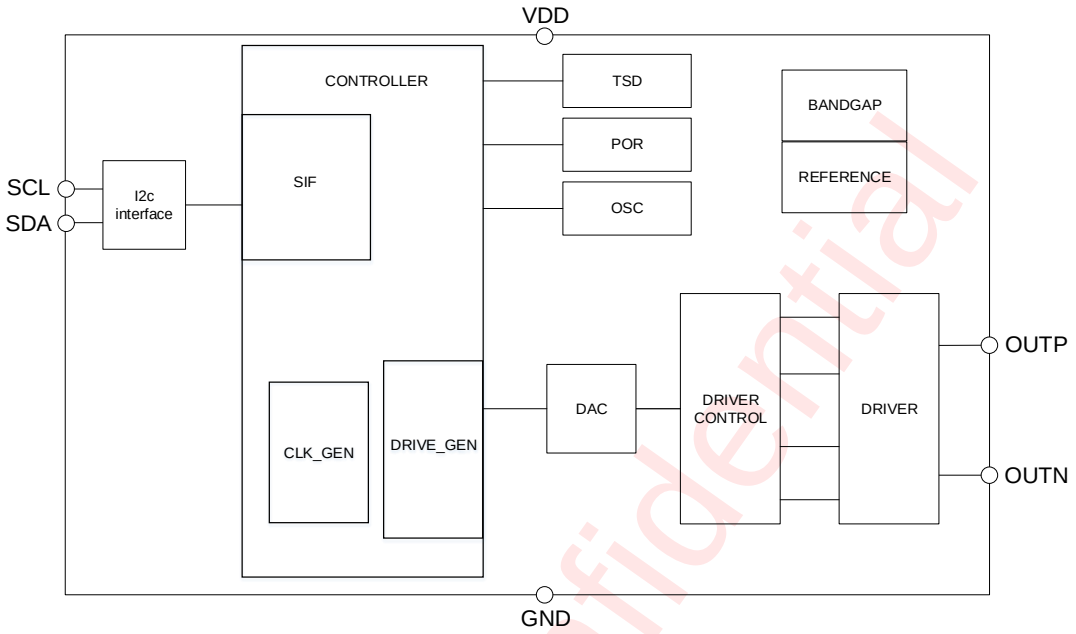


Figure 2 AW86016S Functional Block Diagram

Typical Application Circuits

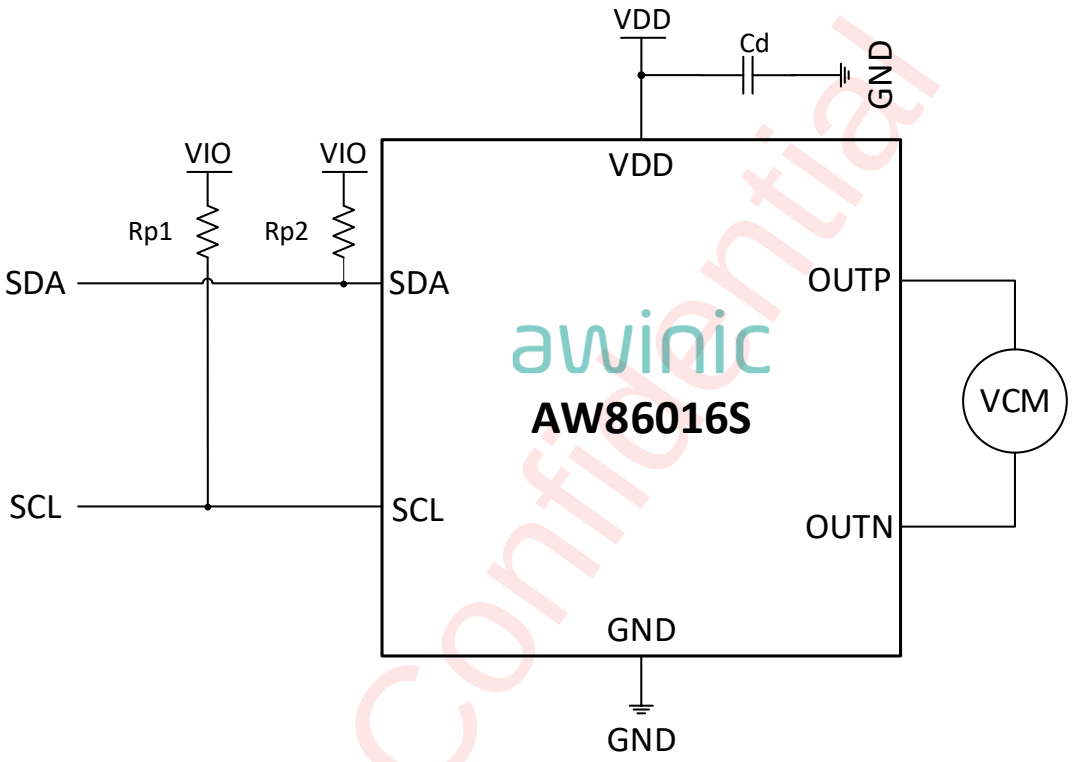


Figure 3 Mid-Typical Application Circuit of AW86016S

Notice for Typical Application Circuits:

1. Power supply decoupling capacitor (Cd) should be placed as close as possible to the VDD and GND.
2. Pull-up Resistors (Rp) are necessary for IIC communication. Recommend pull-up resistor (Rp) value is 470Ω@f_{SCL}=3.4MHz, 1kΩ@f_{SCL}=1000kHz or 4.7kΩ@f_{SCL}=400kHz.
3. Recommend decoupling capacitor (Cd) value is at least 1μF

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW86016SCSR	-40°C~85°C	WLCSP 0.59mm x 0.99mm x 0.265mm -6B	C	MSL1	RoHS+HF	4500 units/ Tape and Reel

Self-Adapting Identification Mechanism

The device can self-adaptively adjust the I²C address according to the hardware connection. As the connection method shown in the following figure, if the device address of Slave A is 0x18(8-bit), then the device address of Slave B is 0x38(8-bit).

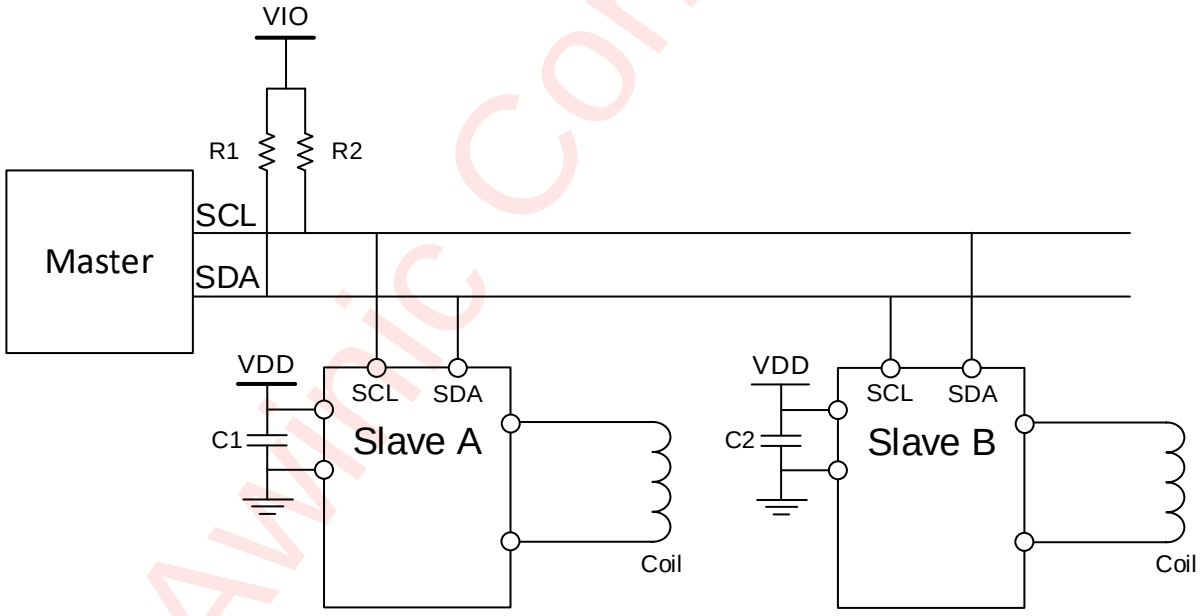


Figure 4 Hardware Connection of Self-Adapting Identification

Absolute Maximum Ratings(NOTE 1)

Parameters	Range
Supply voltage range V_{DD}	-0.3V to 4.2V
Control input voltage range V_{IN}	-0.3V to V_{DD}+0.3V
Operating free-air temperature range T_{OPR}	-40°C to 85°C
Maximum operating junction temperature T_{JMAX}	150°C
Storage temperature range T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	240°C
ESD(NOTE 2)	
Test standard(HBM):ESDA/JEDEC JS-001-2017	±2000V
Test standard(CDM):ESDA/JEDEC JS-002-2018	±1500V
Latch-up	
Test standard:JESD78E	+IT:200mA -IT:-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2:The human body model is a 100pF capacitor discharged through a 1.5KΩ resistor into each pin.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Power supply voltage	2.3		3.6	V
V_{IN}	Control input voltage	0		V_{DD}	V
f_{SCL}	Serial clock frequency		400	3400	kHz

Electrical Characteristics

V_{DD}=2.8V, V_{IO}=1.2V, T_A=25°C for typical values (unless otherwise noted)

Parameter		Test condition	Min	Typ	Max	Unit
Overall						
V_{DD}	Power supply voltage	On pin VDD	2.3	2.8	3.6	V
T_{TURNON}	Supply Turn On Time		0.05		3	ms
$T_{RESTART}$	Re-start Time		1			ms
T_{DELAY}	Turn On Delay		2			ms
I_{QZ}	Quiescent current	DAC=0x200	0.15	0.23	0.3	mA
I_Q	Quiescent current	DAC≠0x200	0.25	0.35	0.45	mA
I_{PD}	Power Down current	V_{DD}=2.8V	-1	0.3	1	μA
t_{SET}(NOTE 2)	Setup waiting time			400		μs
Logic input / output（SCL/SDA）						
I_S	Input current		-1	0	1	μA
V_{IL}	Logic input low level	SCL/SDA			0.36	V
V_{IH}	Logic input high level	SCL/SDA	0.84			V
V_{OL}	SDA low level output voltage	SDA, IOL=12mA			0.3	V
Driver						
I_{MAX0}(NOTE 3)	Maximum output current (IMAX=0)	IOUT=±100mA	±97	±100	±103	mA
I_{MAX1}(NOTE 3)	Maximum output current (IMAX=1)	IOUT=±(100+30)mA	±125	±130	±135	mA
I_{SD}	Shutdown current		-1	0	1	μA
Resolution	DAC resolution			10		Bits
R_{TOTAL}(NOTE 3)	Total output resistance	IOUT=100mA		2.5		Ω
Pos(NOTE3, 4,5) INL	Positive Integral Non-Linearity		-4		4	LSB
Pos(NOTE3, 4,5) DNL	Positive Differential Non-Linearity		-1		1	LSB

Parameter			Test condition	Min	Typ	Max	Unit
Neg(NOTE3, 4,6)	INL	Negative Integral Non-Linearity		-4		4	LSB
	DNL	Negative Differential Non-Linearity		-1		1	LSB

NOTE3: Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device

NOTE4: Maximum output current can be changed by register setting.

NOTE5: Postive Code is DAC[9:0] = 520~1016.

NOTE6: Negative Code is DAC[9:0] = 8~504.

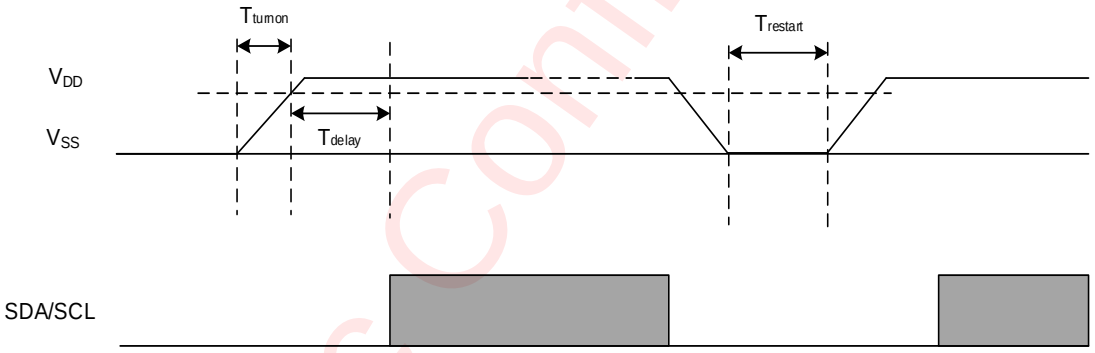


Figure 5 VDD Supply And I2C Interface Timing

Detailed Functional Description

POWER UP SEQUENCE

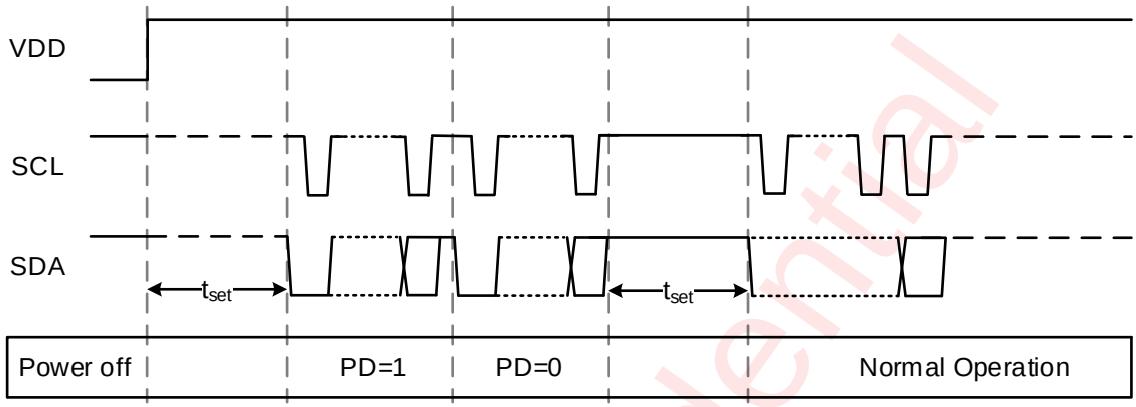


Figure 6 Power Up Sequence

T_{set}: After VDD(Min) is reached, user must wait for a while before I2C work.

The power on sequence of this device is illustrated in the above figure.

FAST SETTLING FUNCTION

The device supports linear slope series control mode (LSC) and voice coil motor ringing series control mode (VRC), which allows programmable configuration of output current waveform to minimize mechanical vibration for fast settling function, and can be suitable for different types of voice coil motors. A status monitor is available in register STATUS[0] – BUSY, it will automatic trigger to "1" when a control mode is executing, and I²C instruction will not respond during the "BUSY" status.

LSC SCHEME

In linear slope control (LSC) mode, the output current increase or decrease to the target in several same steps, the whole output current waveform appears as a first-order linear function.

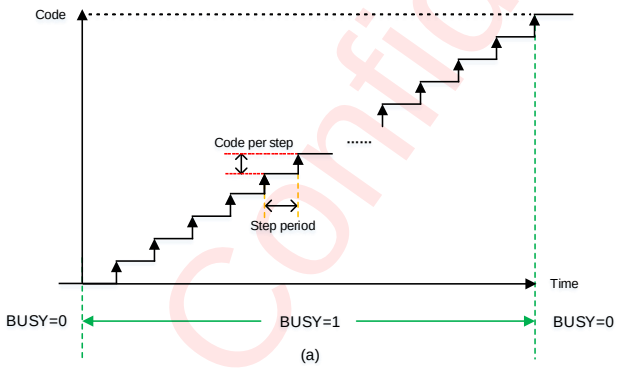


Figure 7 LSC Scheme

VRC SCHEME

Voice coil motor ringing control (VRC) mode is a smart solution for reducing mechanical ringing and achieving very fast settling time, therefore it reduces autofocus response time and enhances image quality. VRC mode incorporates a wide band of tolerance around the vibration period of the VCM to compensate for manufacturing variability in the mechanical vibration period (T_{vib}) of VCM. The device offers different VRC modes which are trade-off operation time and tolerance. Customer can select the appropriate VRC mode to fit different specifications of voice coil motors.

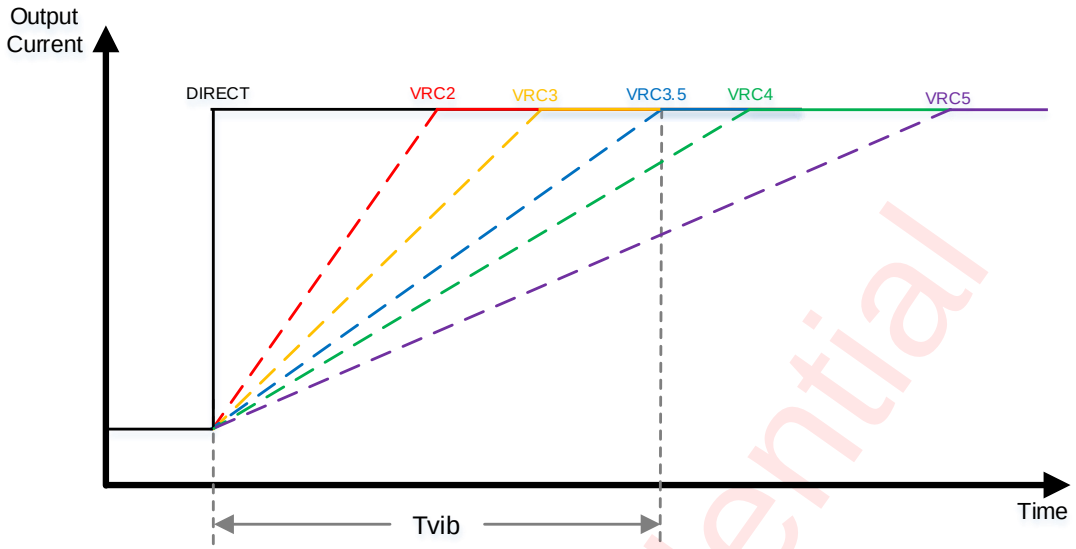


Figure 8 Control Mode Setting Time

Control Mode	Operation Time(NOTE 7)	Frequency Tolerance(NOTE 8)
DIRECT	-	-
VRC2	T_{vib} x 0.48	±9%
VRC3	T_{vib} x 0.72	±19%
VRC3.5	T_{vib} x 1.0	±31%
VCR4	T_{vib} x 1.20	±37%
VCR5	T_{vib} x 1.64	±43%

NOTE7: T_{vib} means the mechanical vibration period of voice coil motors.

NOTE8: Tolerance can be changed by mechanical characteristics of different voice coil motors.

I²C INTERFACE

This device supports the I²C serial bus and data transmission protocol in Fast-mode(Fm) at 400kHz ,fast-mode plus(Fm+) at 1MHz and Hs-mode at 3.4MHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 470~10kΩ and the typical value is 4.7kΩ. This device can support different high level (1.1V~3.6V) of this I²C interface.

DEVICE ADDRESS

The default device address of the chip is 0x18(7-bit 0x0C), and which can be changed by the factory.

DATA VALIDATION

When SCL is high level, SDA level must be stable. SDA can be changed only when SCL is low level.

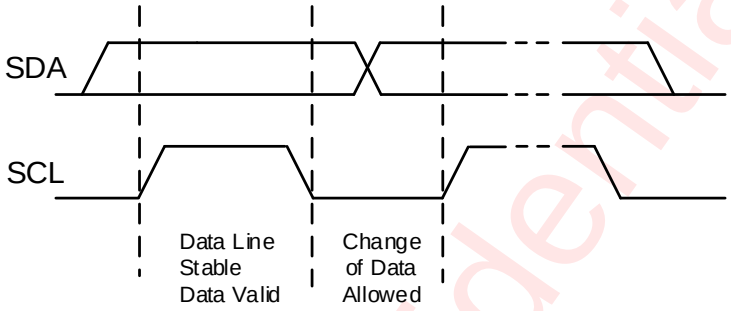


Figure 9 Data Validation Diagram

I²C START/STOP

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

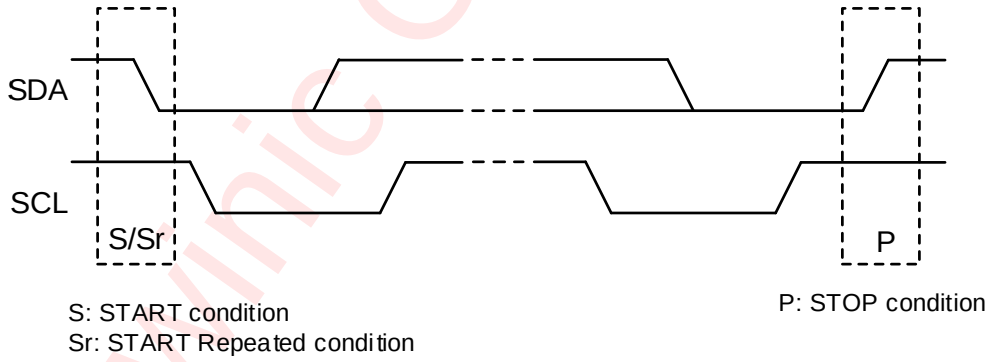


Figure 10 I²C Start/Stop Condition Timing

ACKNOWLEDGE(ACK)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

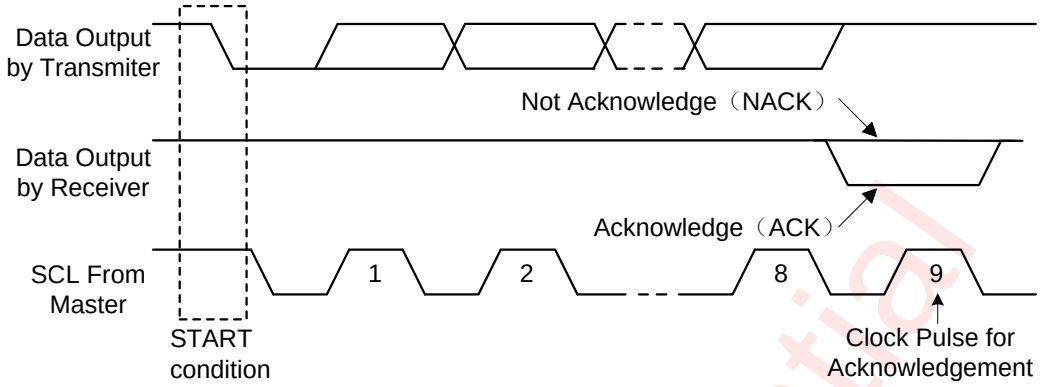


Figure 11 I²C ACK Timing

WRITE PROCESS

Writing process refers to the master device write data into the slave device. In this process, the transfer direction of the data is always unchanged from the master device to the slave device. All acknowledgment bits are transferred by the slave device, in particular, the device as the slave device, the transmission process in accordance with the following steps, as shown in the following figure.

1. Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.
2. Master device transmits the 7-bits device address of the slave device, and followed by the "read / write" flag ($R/\overline{W}$ = 0);
3. The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;
4. The master device transmits the 8-bits register address to which the first data byte will written;
5. The slave device asserts an acknowledgment (ACK) bit to confirm the register address is correct;
6. Master sends 8-bits of data to register which needs to be written;
7. The slave device asserts an acknowledgment bit (ACK) to confirm whether the data is sent successfully;
8. If the master device needs to continue transmitting data by sending another pair of data bytes, just need to repeat the sequence from step 6~7. In the latter case, the targeted register address will have been auto-incremented by the device.

9. The master device generates the STOP state to end the data transmission.

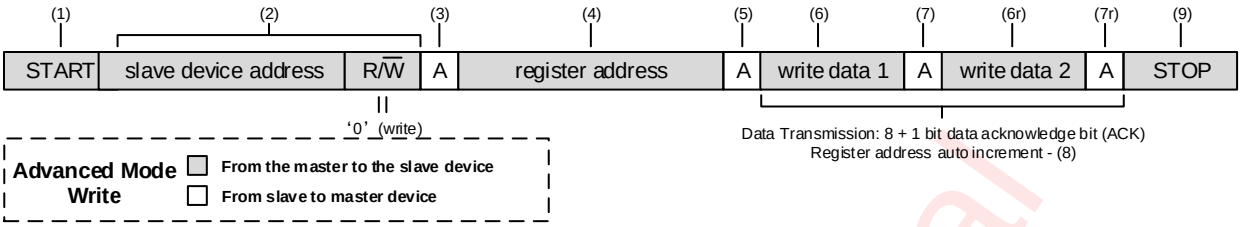


Figure 12 Writing process

READ PROCESS

Reading process refers to the slave device reading data back to the master device. In this process, the direction of data transmission will change. Before and after the change, the master device sends START state and slave address twice, and sends the opposite "read/write" flag. As the slave device, the transmission process carried out by following steps listed in the following figure.

1. Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.
2. Master device transmits the 7-bits device address of the slave device, and followed by a "read / write" flag ($R/\overline{W} = 0$);
3. The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;
4. The master device transmits the register address to make sure where the first data byte will read;
5. The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;
6. The master device restarts the data transfer process by continuously generating STOP state and START state or a separate Repeated START;
7. Master sends 7-bits address of the slave device and followed by a read / write flag ($R/\overline{W} = 1$) again;
8. The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;
9. Master transmits 8-bits of data to register which needs to be read;
10. The slave device sends an acknowledgment bit (ACK) to confirm whether the data is sent

successfully, but no need for an acknowledgment bit (NOACK) in the last data transmission process;

11. The device automatically increment register address once after sent each acknowledgment bit (ACK);

12. The master device generates the STOP state to end the data transmission.

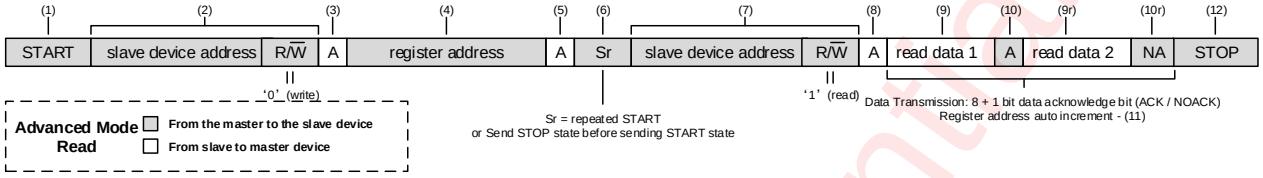


Figure 13 Reading process

I²C TIMING FEATURE

Parameter			Fm		Fm+		Hs-mode		Unit
No.	Symbol	Name	Min	Max	Min	Max	Min	Max	
1	f_{SCL}	SCL Clock frequency		400		1000		3400	KHz
2	t_{LOW}	SCL Low level Duration	1.30		0.50		0.16		μs
3	t_{HIGH}	SCL High level Duration	0.70		0.26		0.06		μs
4	t_{RISE}	SCL, SDA rise time		0.30		0.12		0.04	μs
5	t_{FALL}	SCL, SDA fall time		0.30		0.12		0.04	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.60		0.26		0.16		μs
7	$t_{HD:STA}$	(repeat-start) start condition hold time	0.60		0.26		0.16		μs
8	$t_{SU:STO}$	Stop condition setup time	0.60		0.26		0.16		μs
9	t_{BUF}	Time between start and stop condition	1.30		0.50		0.16		μs
10	$t_{SU:DAT}$	SDA setup time	0.10		0.10		0.10		μs
11	$t_{HD:DAT}$	SDA hold time	0		0		0		μs

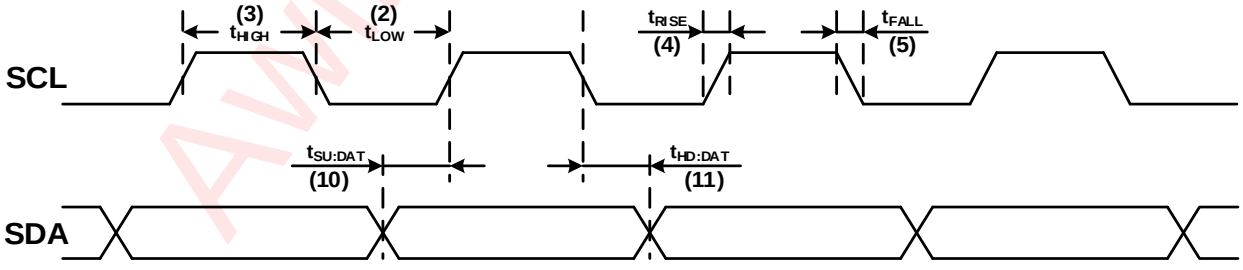


Figure 14 SCL and SDA timing relationships in the data transmission process

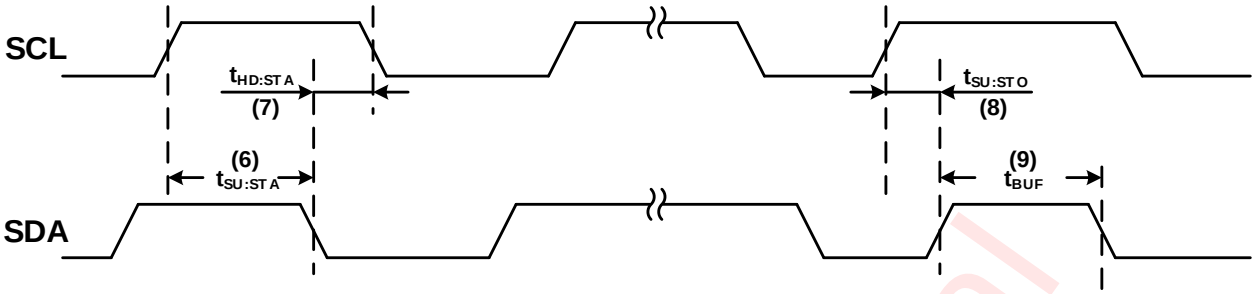


Figure 15 The timing relationship between START and STOP state

REGISTER LIST

Addr	Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	IC_INFO	RO							CHIP_ID		0x03
0x01	IC_VER	RO						IC_VER			0x01
0x02	CONTROL	RW							RING	SPD	0x00
0x03	CODE_H	RW							CODE_H		0x02
0x04	CODE_L	RW	CODE_L								0x00
0x05	STATUS	RO							EF_DONE	BUSY	0x00
0x06	ALG_MODE	RW	VRC_MODE							DIV_H	0x00
0x07	DIV	RW	DIV_L					VRCT			0x60
0x10	IMAX	RW						SEL_IMAX		IMAX_30	0x08

RO: Read Only

RW: Read and Write available

SET UP METHOD

Here gives some examples of set up sequence, more details please refer to “Register Detailed Description”.

Control Mode	Operate Seq.	Device Addr.	Register Addr.	Register Data	Description
Power Down	1	0x18	0x02	0x01	Enter Power Down Mode
Direct	1	0x18	0x02	0x00	Set RING to 1’b0
	2	0x18	0x06	0x00	Set Direct Mode
	3	0x18	0x03,0x04	CODE[9:0]	VCM Drive
VRC3	1	0x18	0x02	0x02	Set RING to 1’b1
	2	0x18	0x06	0x40	Set VRC3 Mode & Period Divider
	3	0x18	0x07	DIV_L & VRCT[6:0]	Set Period Divider & Time Step
	4	0x18	0x03,0x04	CODE[9:0]	VCM Drive

REGISTER DETAILED DESCRIPTION

IC_INFO: Address(0x00)				
Bit	Symbol	R/W	Description	Default
7:3	Reserved	RW	Not used	0
2:0	CHIP_ID	RO	CHIP_ID	0x3

IC_VER: Address(0x01)				
Bit	Symbol	R/W	Description	Default
7:4	Reserved	RO	Not used	0
3:0	IC_VER	RO	IC Version Fixed in ANALOG_TOP	0x1

CONTROL: Address(0x02)				
Bit	Symbol	R/W	Description	Default
7:2	Reserved	RW	Not used	0
1	RING	RW	Ringing Control Enable RING VRC_MODE[1:0] MODE 0 00 Direct 0 01 Reserved 0 10 LSC(LSC1) 0 11 VRC3.5 1 00 VRC2 1 01 VRC3 1 10 VRC4 1 11 VRC5	0x0
0	SPD	RW	Soft Reset (PD Mode) 0: Work(Realease Soft Shutdown) 1: Soft Shutdown, go into PD Mode	0x0

CODE_H: Address(0x03)				
Bit	Symbol	R/W	Description	Default
7:2	Reserved	RW	Not used	0
1:0	CODE_H	RW	10bit DAC Code bit8~bit9 bit9 Mid Mount Mode Direction Control 0: Negative direction 1: Positive direction	0x2

CODE_L: Address(0x04)				
Bit	Symbol	R/W	Description	Default
7:0	CODE_L	RW	10bit DAC Code bit0~bit7 (trig byte) Negative output current = -(512 - CODE[8:0]) x (100mA / 512) [mA] Positive output current = CODE[8:0] x (100mA / 512) [mA] OUTN & OUTP(DAC output) is updated when address 0x04 is written.	0x00

STATUS: Address(0x05)				
Bit	Symbol	R/W	Description	Default
7:2	Reserved	RO	Not used	0
1	EF_DONE	RO	Efuse Initial Load Done Signal 0: efsue data unprepared 1: efuse initial load data done	0x0
0	BUSY	RO	Indicate the chip is busying generate wave BUSY bit should be ”L” when ”CODE_H and CODE_L” registers are written. During ringing control operation, the BUSY bit is ”H” and the I2C write commands to registers except SPD bit of 0x02 are ignored.	0x0

ALG_MODE: Address(0x06)				
Bit	Symbol	R/W	Description	Default
7:6	VRC_MODE	RW	VCM Ringing Control(VRC) Mode Selection RING VRC_MODE[1:0] MODE 0 00 Direct 0 01 Reserved 0 10 LSC1 0 11 VRC3.5 1 00 VRC2 1 01 VRC3 1 10 VRC4 1 11 VRC5	0x0
5:1	Reserved	RO	Not used	0
0	DIV_H	RW	Time Step Scaling Factor (Period Divider) bit2 3'b0 00: Tvib x 2 3'b0 01: Tvib x 1 (default) 3'b0 10: Tvib x 0.5 3'b0 11: Tvib x 0.25 3'b1 00: Tvib x 8 3'b1 01: Tvib x 4 else : Tvib x 1 (reserved default)	0x0

DIV: Address(0x07)				
Bit	Symbol	R/W	Description	Default
7:6	DIV_L	RW	Time Step Scaling Factor (Period Divider) bit0~bit1 3'b0 00: Tvib x 2 3'b0 01: Tvib x 1 (default) 3'b0 10: Tvib x 0.5 3'b0 11: Tvib x 0.25 3'b1 00: Tvib x 8 3'b1 01: Tvib x 4 else : Tvib x 1 (reserved default)	0
5:0	VRCT	RW	Mid Mount Mode Time Step Setting VRC Setting Time = Tvib = (6.3ms + VRCT[5:0] x 0.1ms) x DIV[2:0] (1.575ms~100.8ms) LSC Step Time = (252us + VRCT[5:0] x 4 us) x DIV[2:0] (63us~4032us)	0x0

IMAX: Address(0x10)				
Bit	Symbol	R/W	Description	Default
7:4	Reserved	RW	Not used	0
3:1	SEL_IMAX	RW	Slection of Driver Max Sink Current (Reg Control) 3'b000: 80mA 3'b001: 120mA 3'b1xx: 100mA(default)	0x04
0	IMAX	RW	Maximum Output Current 0: Imax+0mA(default) 1: Imax+30mA	0x0

PCB Layout Consideration

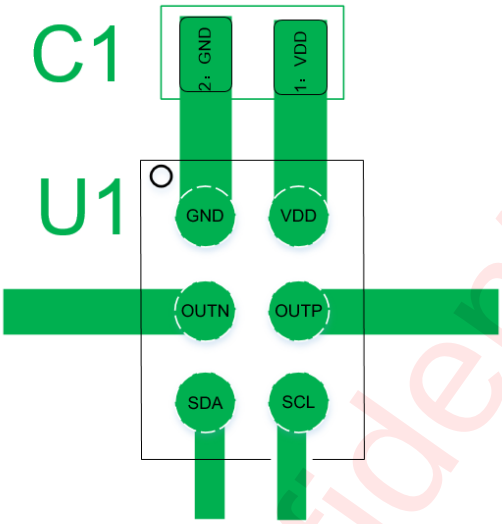


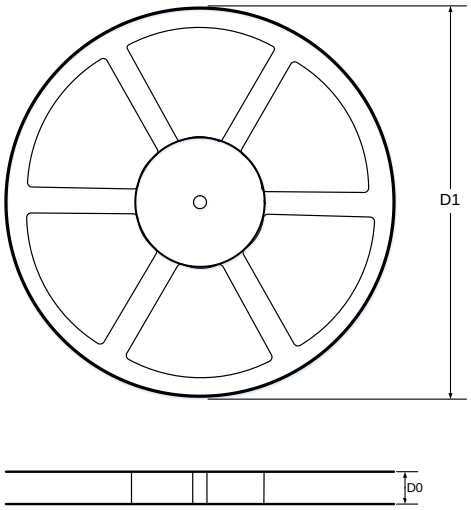
Figure 16 AW86016S PCB Layout Placement

To obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

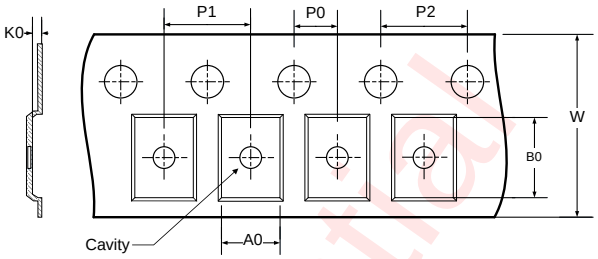
1. The decoupling capacitor Cd should be placed close to the chip VDD and GND on the same layer as the chip to ensure the best filtering effect.
2. I^2C bus should be surrounded by GND as mush as possible.
3. VDD,OUTN,OUTP should be routed as thick as possible after exiting from the pad to meet the overcurrent capability; VDD,OUTN,OUTP must be routed to meet at least 250mA of current.

Tape And Reel Information

REEL DIMENSIONS

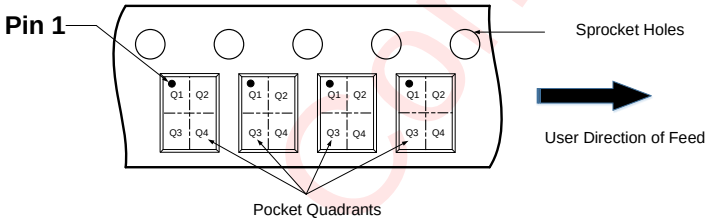


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



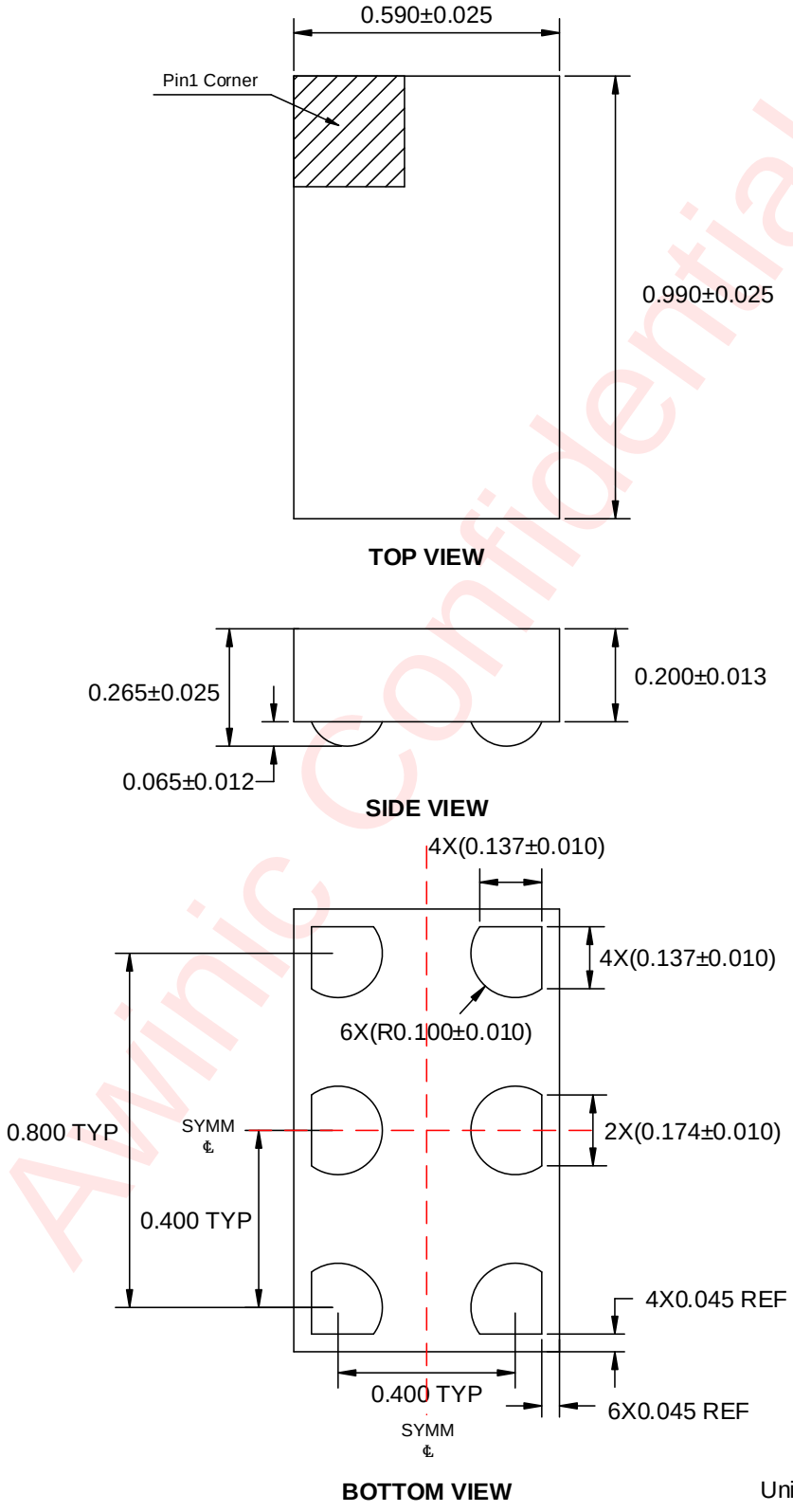
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178.0	8.40	0.70	1.11	0.37	2.00	4.00	4.00	8.00	Q1

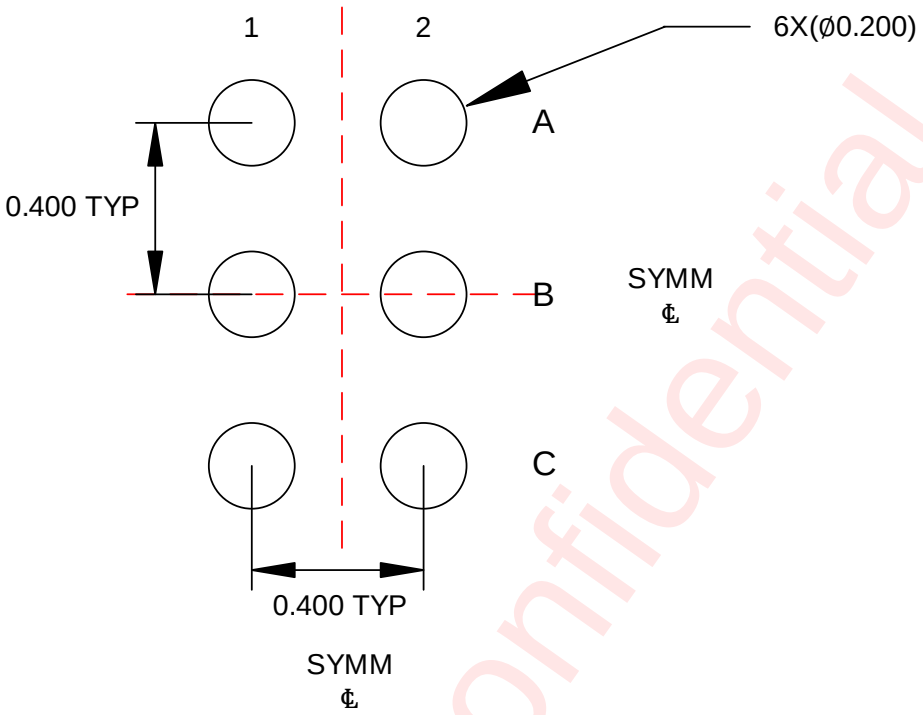
All dimensions are nominal

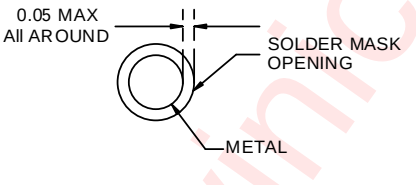
Package Description



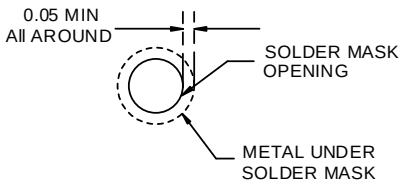
Unit: mm

Land Pattern Data





NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Dec. 2025	Officially released
V1.1	Jan. 2026	1. Add configurable current level descriptions 2. increase I2C communication speed to 3.4Mbps

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