SI4559ADY-T1-E3-VB Datasheet

N- and P-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY				
	V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ.)
N-Channel	60	0.026 at V_{GS} = 10 V	5.3	6 nC
		0.029 at V_{GS} = 4.5 V	4.7	
P-Channel	- 60	0.055 at V_{GS} = - 10 V	- 4.9	8 nC
		0.060 at V_{GS} = - 4.5 V	- 4.5	

FEATURES

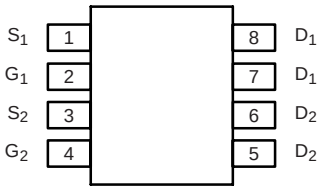
- **Halogen-free According to IEC 61249-2-21 Available**
- Trench Power MOSFET
- 100 % R_g and UIS Tested

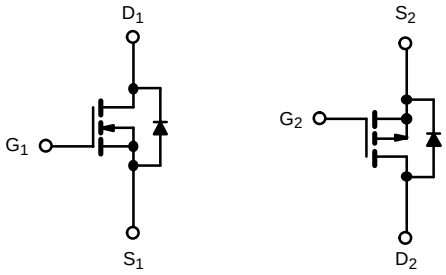
Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

APPLICATIONS

- CCFL Inverter

SO-8





N-Channel MOSFET P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted					
Parameter		**Symbol**	**N-Channel**	**P-Channel**	**Unit**
Drain-Source Voltage		V_{DS}	60	- 60	V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	5.3	- 4.9	A
	T_C = 70 °C		4.3	- 4.2	
	T_A = 25 °C		4.3[b, c]	- 4.0[b, c]	
	T_A = 70 °C		3.4[b, c]	- 3.4[b, c]	
Pulsed Drain Current (10 µs Pulse Width)		I_{DM}	20	- 25	
Source Drain Current Diode Current	T_C = 25 °C	I_S	2.6	- 2.8	
	T_A = 25 °C		1.7[b, c]	- 1.7[b, c]	
Pulsed Source-Drain Current		I_{SM}	20	- 25	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	11	15	
Single Pulse Avalanche Energy		E_{AS}	6.1	11	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	3.1	3.4	W
	T_C = 70 °C		2	2.2	
	T_A = 25 °C		2[b, c]	2[b, c]	
	T_A = 70 °C		1.3[b, c]	1.3[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS							
Parameter		**Symbol**	**N-Channel**		**P-Channel**		**Unit**
			Typ.	**Max.**	**Typ.**	**Max.**	
Maximum Junction-to-Ambient[b, d]	t ≤ 10 s	R_{thJA}	55	62.5	53	62.5	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	33	40	30	37	

Notes:
a. Based on T_C = 25 °C.
b. Surface Mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. Maximum under Steady State conditions is 110 °C/W for N-Channel and P-Channel.

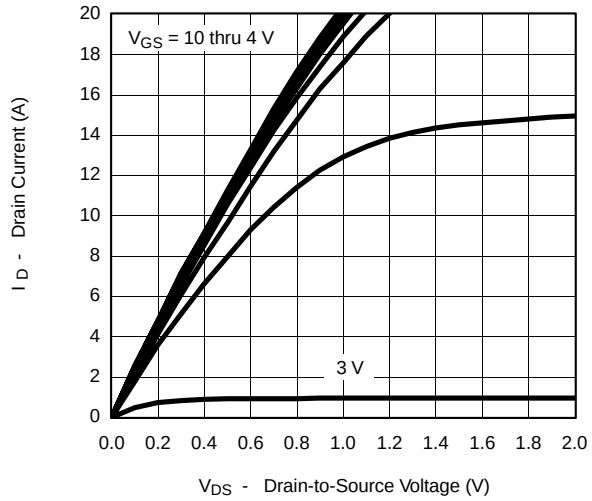
SPECIFICATIONS T_J = 25 °C, unless otherwise noted							
Parameter	**Symbol**	**Test Conditions**		**Min.**	**Typ.[a]**	**Max.**	**Unit**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	N-Ch	60			V
		V_{GS} = 0 V, I_D = - 250 µA	P-Ch	- 60			
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA	N-Ch		55		mV
		I_D = - 250 µA	P-Ch		- 50		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 µA	N-Ch		- 6		
		I_D = - 250 µA	P-Ch		4		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1		3	V
		V_{DS} = V_{GS}, I_D = - 250 µA	P-Ch	- 1		- 3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	N-Ch			100	nA
			P-Ch			- 100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	N-Ch			1	µA
		V_{DS} = - 60 V, V_{GS} = 0 V	P-Ch			- 1	
		V_{DS} = 60 V, V_{GS} = 0 V, T_J = 55 °C	N-Ch			10	
		V_{DS} = - 60 V, V_{GS} = 0 V, T_J = 55 °C	P-Ch			- 10	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	N-Ch	20			A
		$V_{DS} \leq$ - 5 V, V_{GS} = - 10 V	P-Ch	- 25			
Drain-Source On-State Resistance[b]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 4.3 A	N-Ch		0.026		Ω
		V_{GS} = - 10 V, I_D = - 3.1 A	P-Ch		0.055		
		V_{GS} = 4.5 V, I_D = 3.9 A	N-Ch		0.029		
		V_{GS} = - 4.5 V, I_D = - 0.2 A	P-Ch		0.060		
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 4.3 A	N-Ch		15		S
		V_{DS} = - 15 V, I_D = - 3.1 A	P-Ch		8.5		
Dynamic[a]							
Input Capacitance	C_{iss}	N-Channel V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz P-Channel V_{DS} = - 15 V, V_{GS} = 0 V, f = 1 MHz	N-Ch		665		pF
			P-Ch		650		
Output Capacitance	C_{oss}		N-Ch		75		
			P-Ch		95		
Reverse Transfer Capacitance	C_{rss}		N-Ch		40		
			P-Ch		60		
Total Gate Charge	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 4.3 A	N-Ch		13	20	nC
		V_{DS} = - 30 V, V_{GS} = - 10 V, I_D = - 3.1 A	P-Ch		14.5	22	
		N-Channel V_{DS} = 30 V, V_{GS} = 4.5 V, I_D = 4.3 A P-Channel V_{DS} = - 30 V, V_{GS} = - 4.5 V, I_D = - 3.1 A	N-Ch		6	9	
			P-Ch		8	12	
Gate-Source Charge	Q_{gs}		N-Ch		2.3		
			P-Ch		2.2		
Gate-Drain Charge	Q_{gd}		N-Ch		2.6		
			P-Ch		3.7		
Gate Resistance	R_g	f = 1 MHz	N-Ch		2	3	Ω
			P-Ch		14	20	

SPECIFICATIONS T_J = 25 °C, unless otherwise noted							
Parameter	**Symbol**	**Test Conditions**		**Min.**	**Typ.[a]**	**Max.**	**Unit**
Dynamic[a]							
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 30 V, R_L = 8.8 Ω $I_D \cong$ 3.4 A, V_{GEN} = 4.5 V, R_g = 1 Ω	N-Ch		15	25	ns
			P-Ch		30	45	
Rise Time	t_r		N-Ch		65	100	
			P-Ch		70	105	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel V_{DD} = - 30 V, R_L = 12.5 Ω $I_D \cong$ - 2.4 A, V_{GEN} = - 4.5 V, R_g = 1 Ω	N-Ch		15	25	
			P-Ch		40	60	
Fall Time	t_f		N-Ch		10	15	
			P-Ch		30	45	
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 30 V, R_L = 8.8 Ω $I_D \cong$ 3.4 A, V_{GEN} = 10 V, R_g = 1 Ω	N-Ch		10	15	
			P-Ch		10	15	
Rise Time	t_r		N-Ch		15	25	
			P-Ch		13	20	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel V_{DD} = - 30 V, R_L = 12.5 Ω $I_D \cong$ - 2.4 A, V_{GEN} = - 10 V, R_g = 1 Ω	N-Ch		20	30	
			P-Ch		35	55	
Fall Time	t_f		N-Ch		10	15	
			P-Ch		30	45	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C	N-Ch			2.6	A
			P-Ch			- 2.8	
Pulse Diode Forward Current[a]	I_{SM}		N-Ch			20	
			P-Ch			- 25	
Body Diode Voltage	V_{SD}	I_S = 1.7 A	N-Ch		0.8	1.2	V
		I_S = - 2 A	P-Ch		- 0.8	- 1.2	
Body Diode Reverse Recovery Time	t_{rr}	N-Channel I_F = 1.7 A, dI/dt = 100 A/µs, T_J = 25 °C P-Channel I_F = - 2 A, dI/dt = - 100 A/µs, T_J = 25 °C	N-Ch		30	60	ns
			P-Ch		30	50	
Body Diode Reverse Recovery Charge	Q_{rr}		N-Ch		32	50	nC
			P-Ch		35	60	
Reverse Recovery Fall Time	t_a		N-Ch		25		ns
			P-Ch		16		
Reverse Recovery Rise Time	t_b		N-Ch		5		
			P-Ch		14		

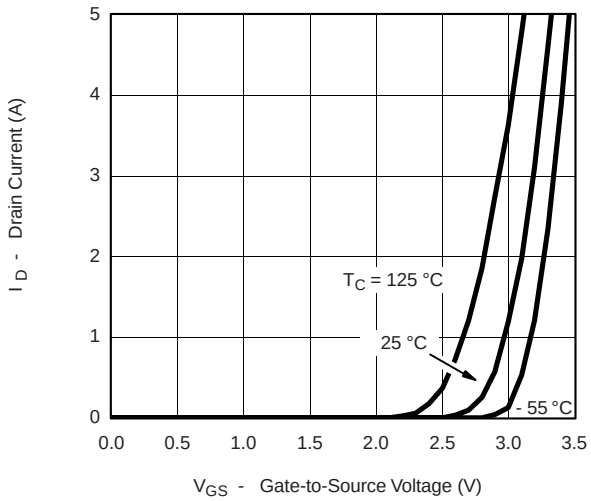
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

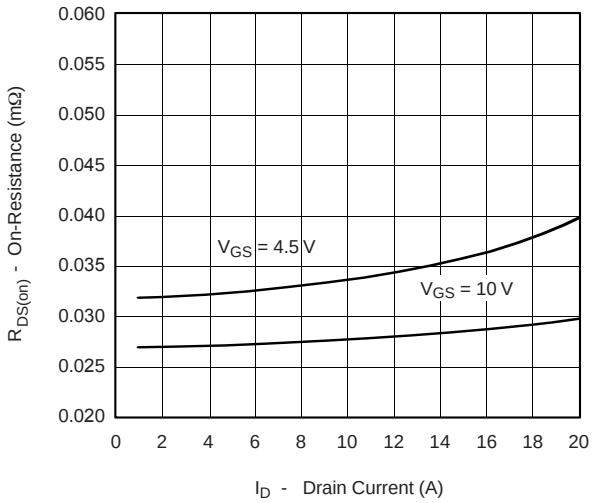
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



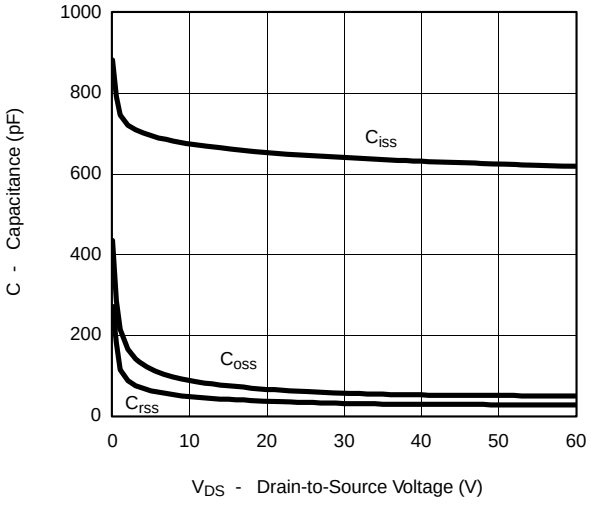
Output Characteristics



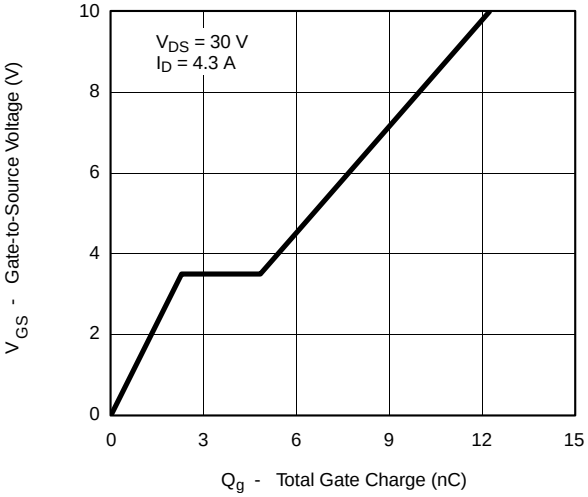
Transfer Characteristics



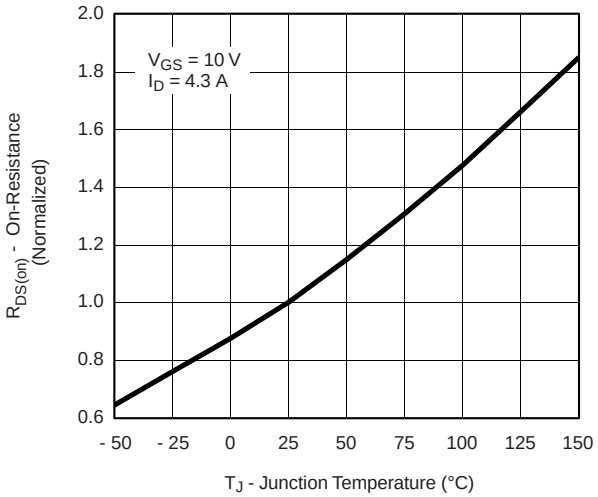
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

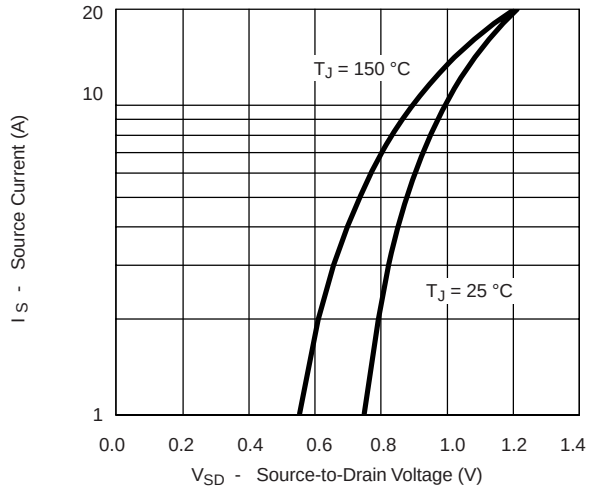


Gate Charge

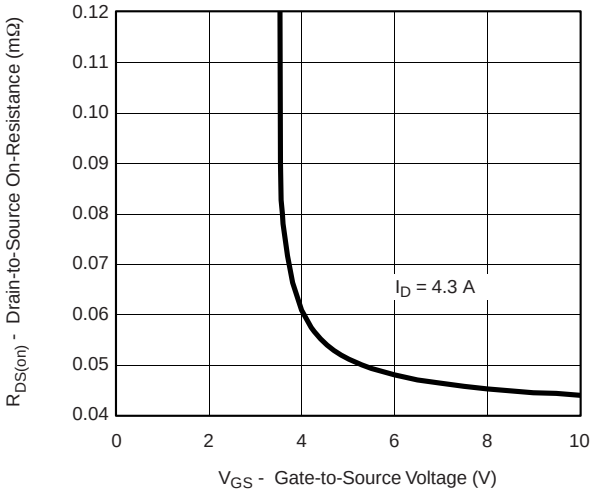


On-Resistance vs. Junction Temperature

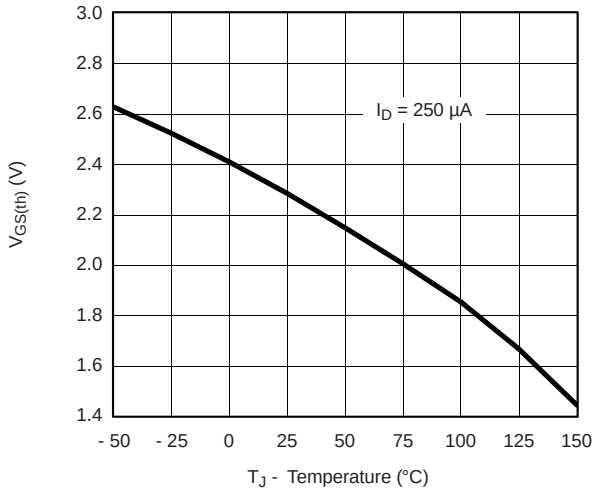
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



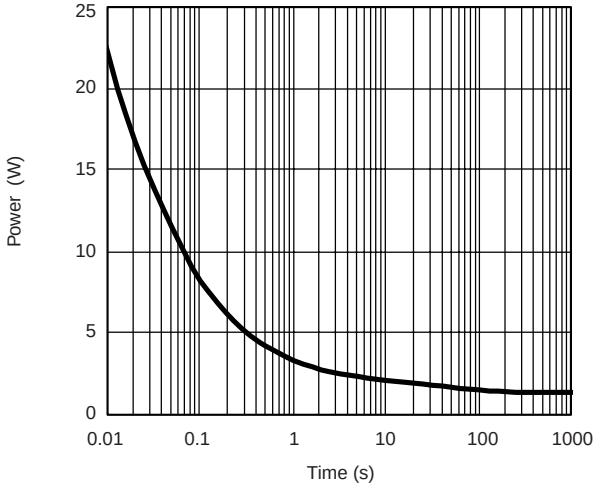
Source-Drain Diode Forward Voltage



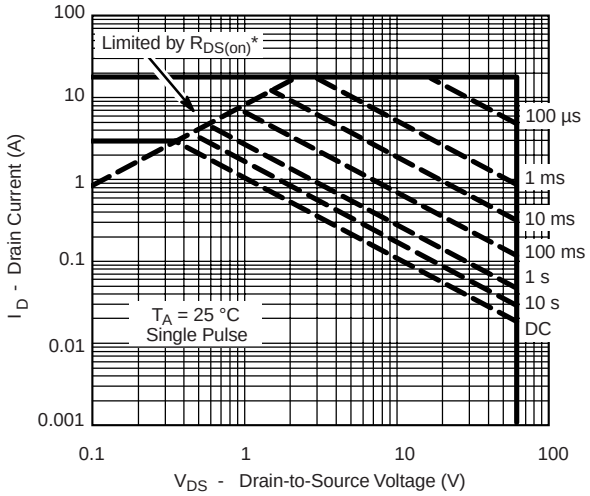
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



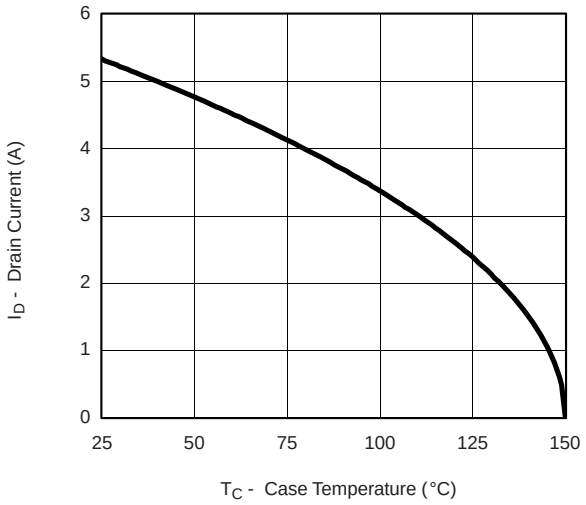
Single Pulse Power, Junction-to-Ambient



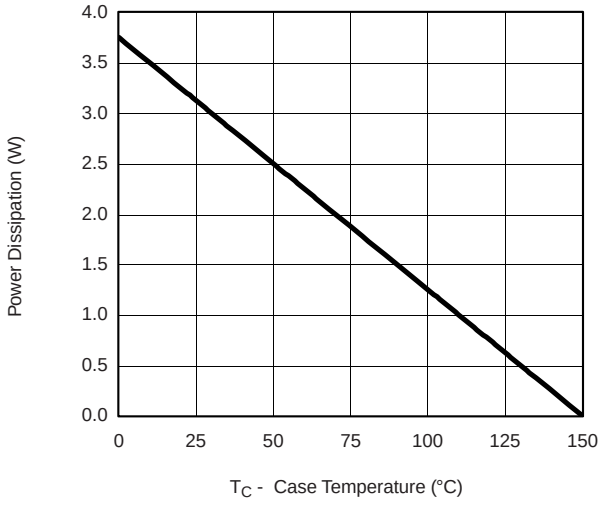
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

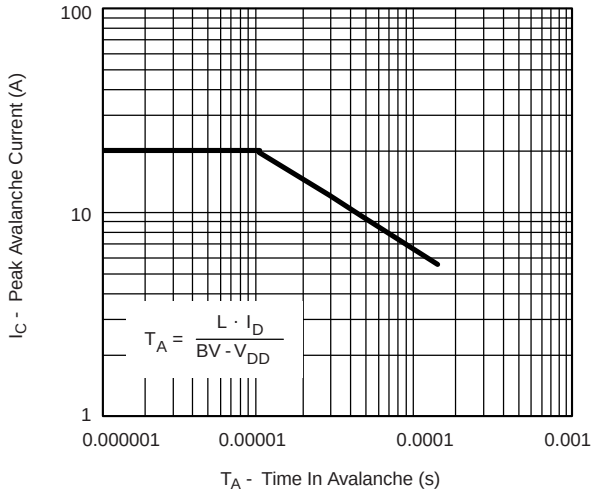
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



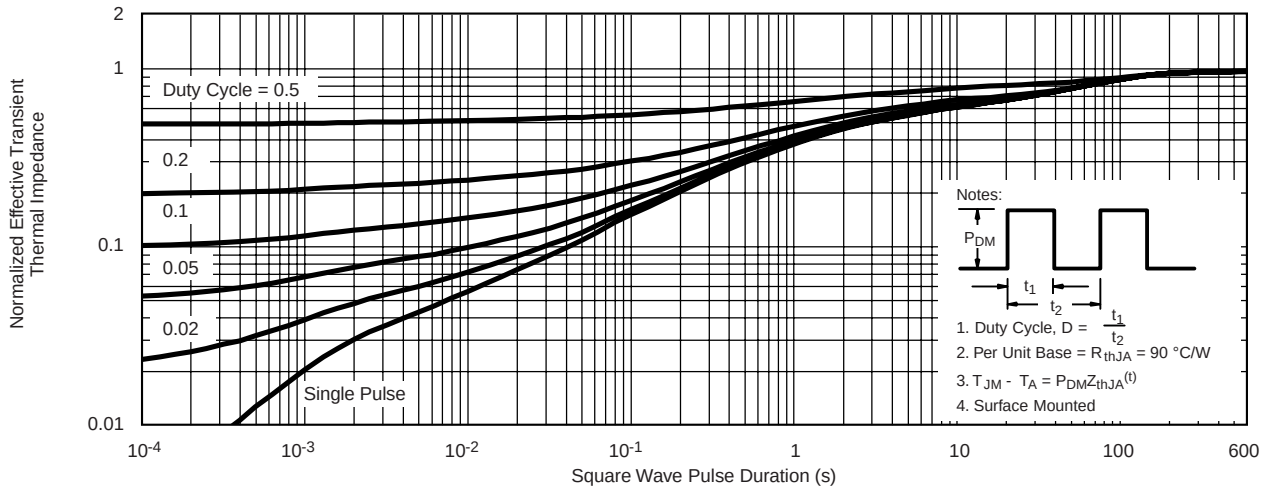
Power Derating



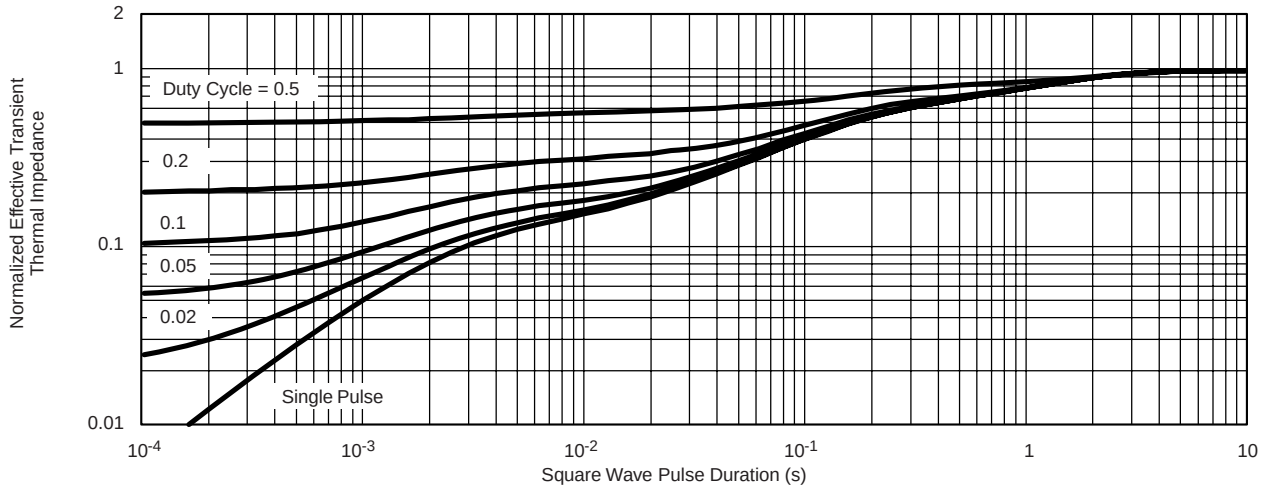
Single Pulse Avalanche Capability

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

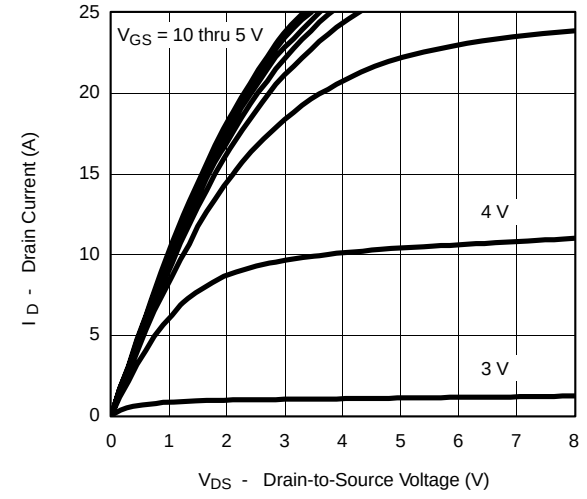


Normalized Thermal Transient Impedance, Junction-to-Ambient

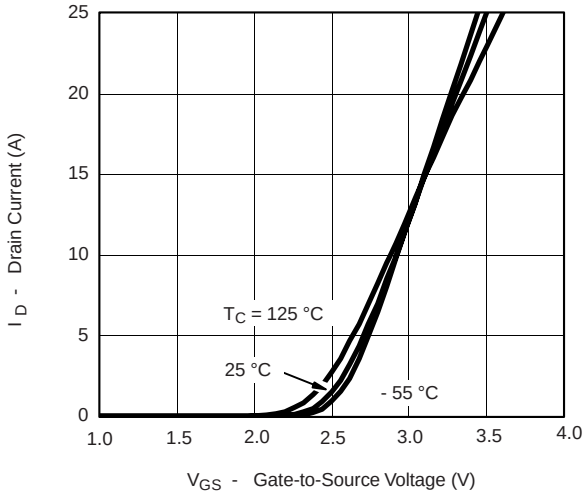


Normalized Thermal Transient Impedance, Junction-to-Case

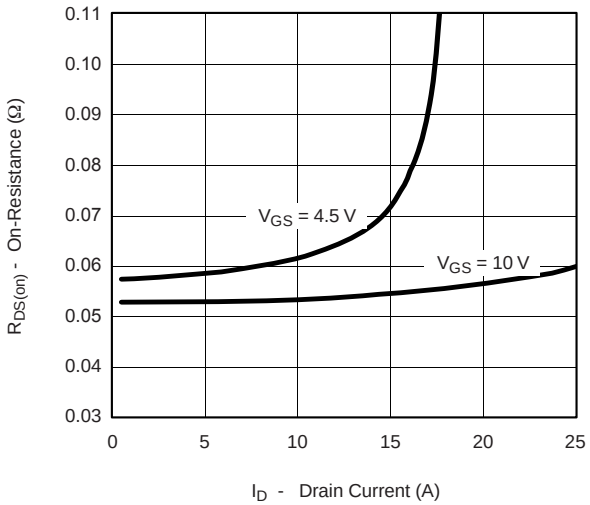
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



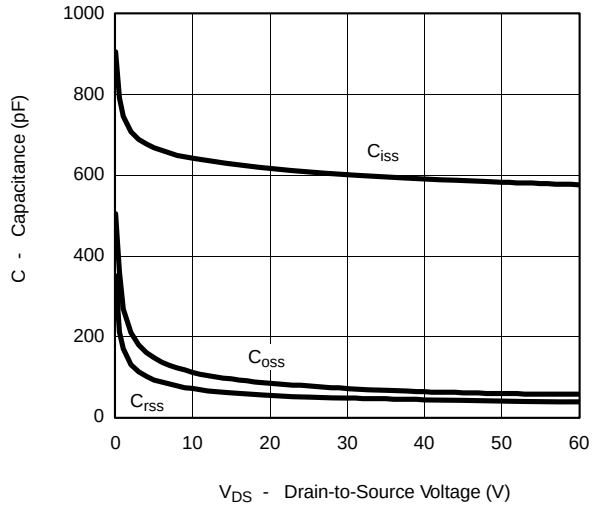
Output Characteristics



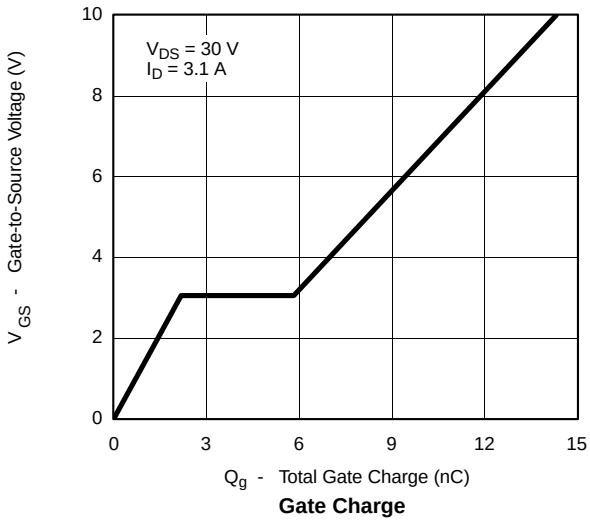
Transfer Characteristics



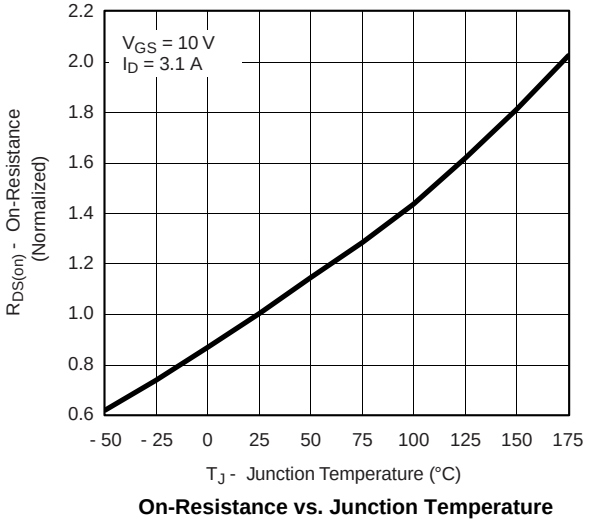
On-Resistance vs. Drain Current



Capacitance

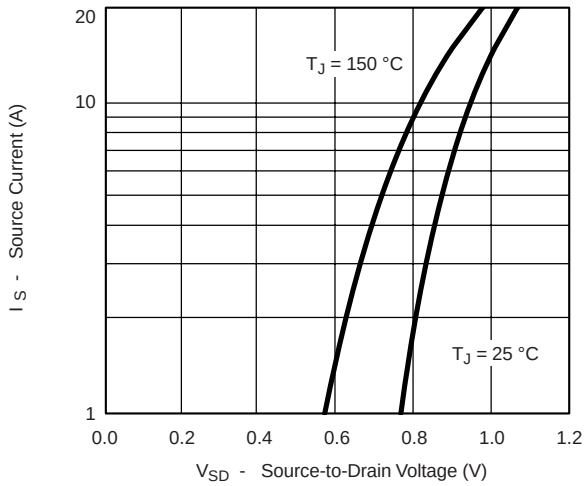


Gate Charge

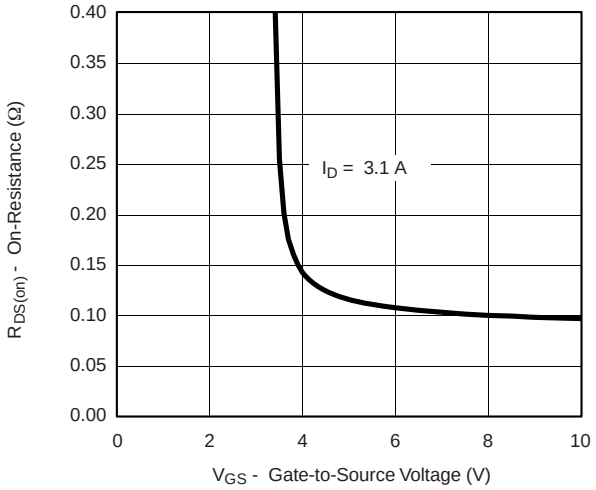


On-Resistance vs. Junction Temperature

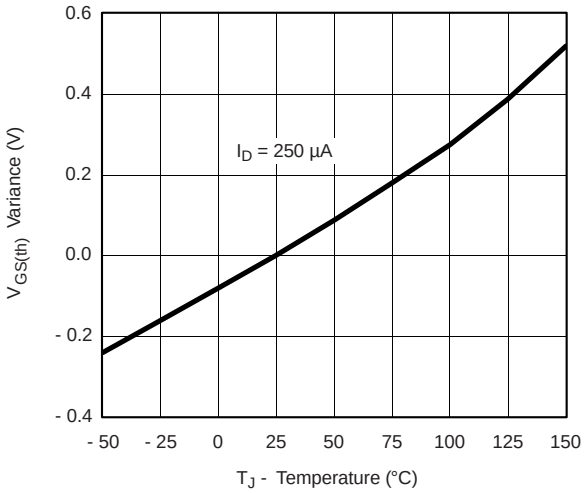
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



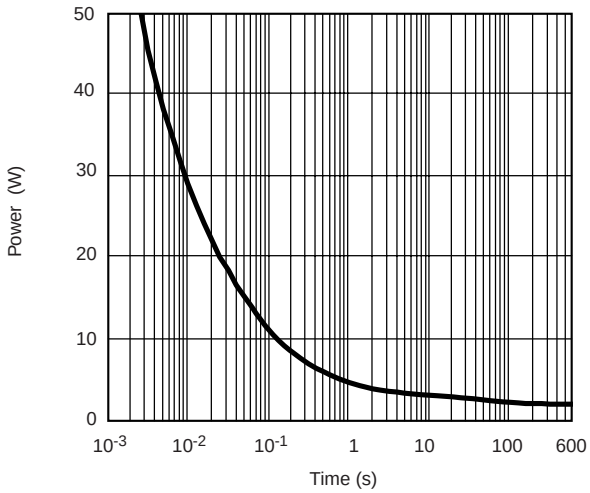
Source-Drain Diode Forward Voltage



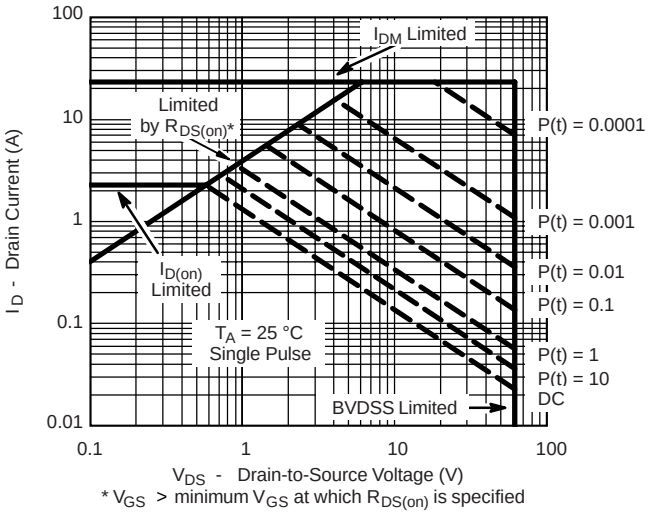
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

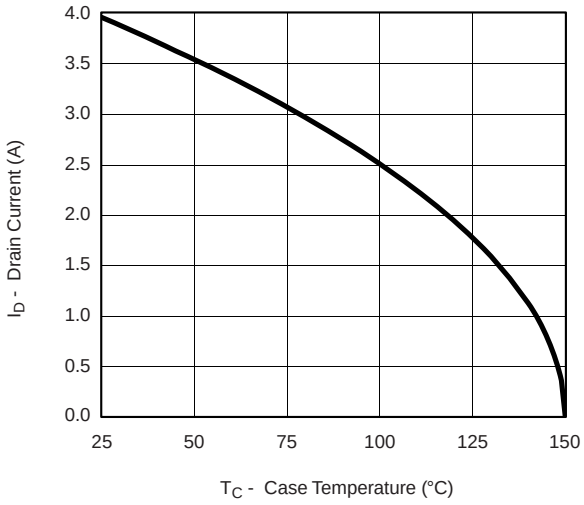


Single Pulse Power

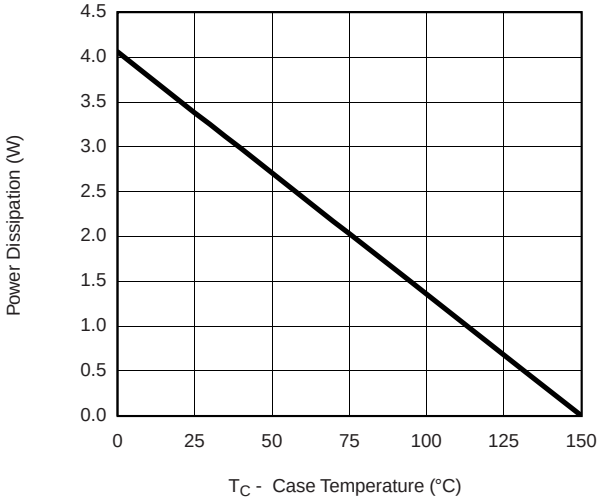


Safe Operating Area, Junction-to-Case

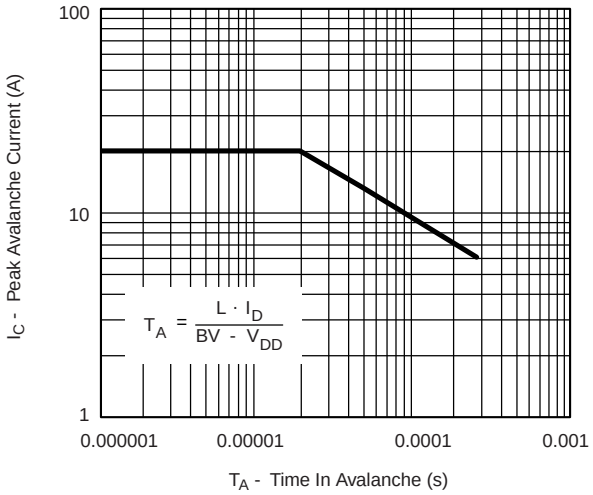
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



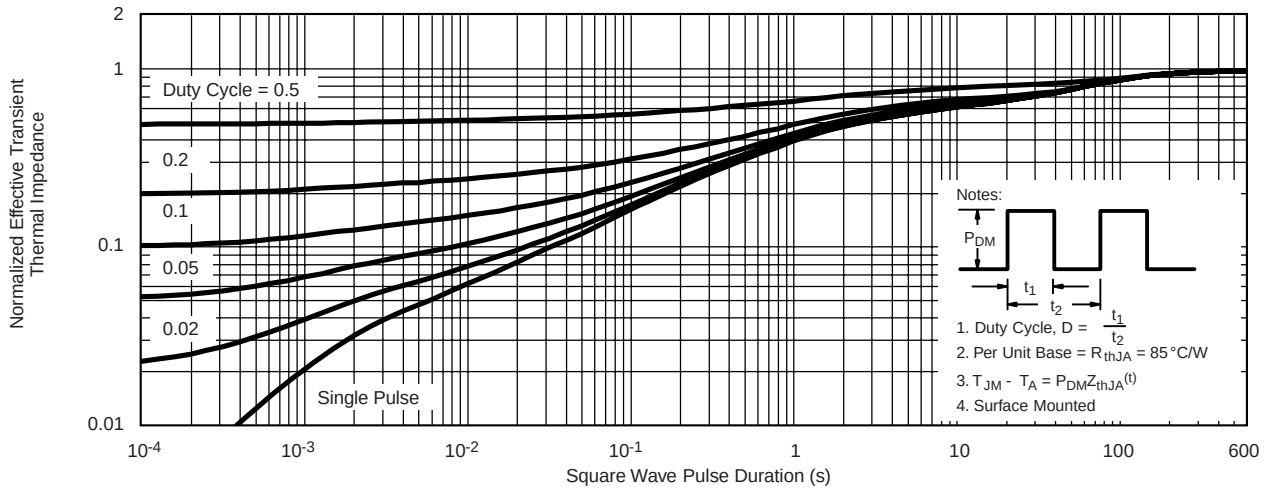
Power Derating, Junction-to-Foot



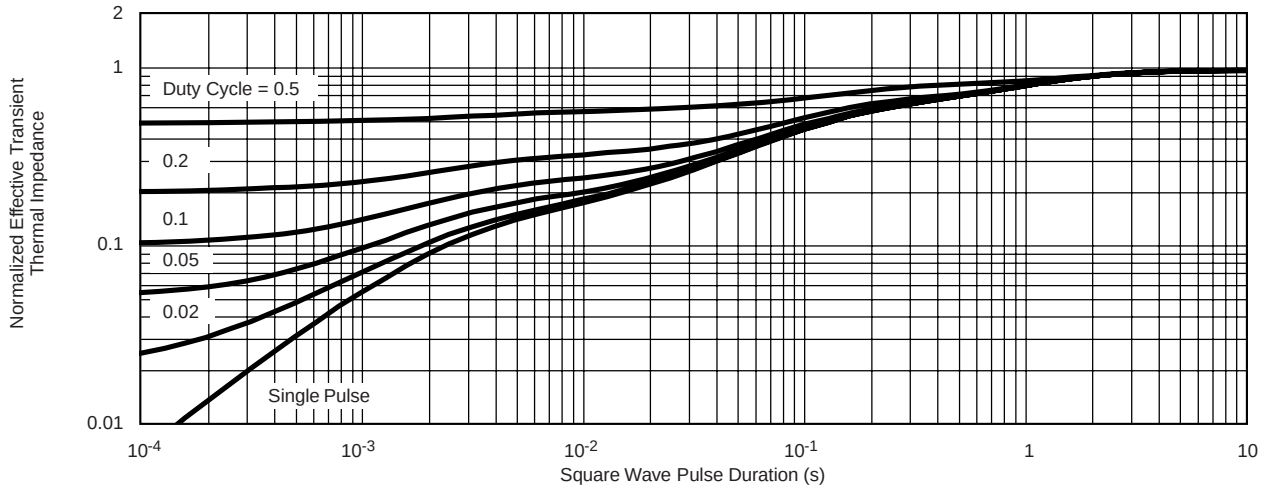
Single Pulse Avalanche Capability

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

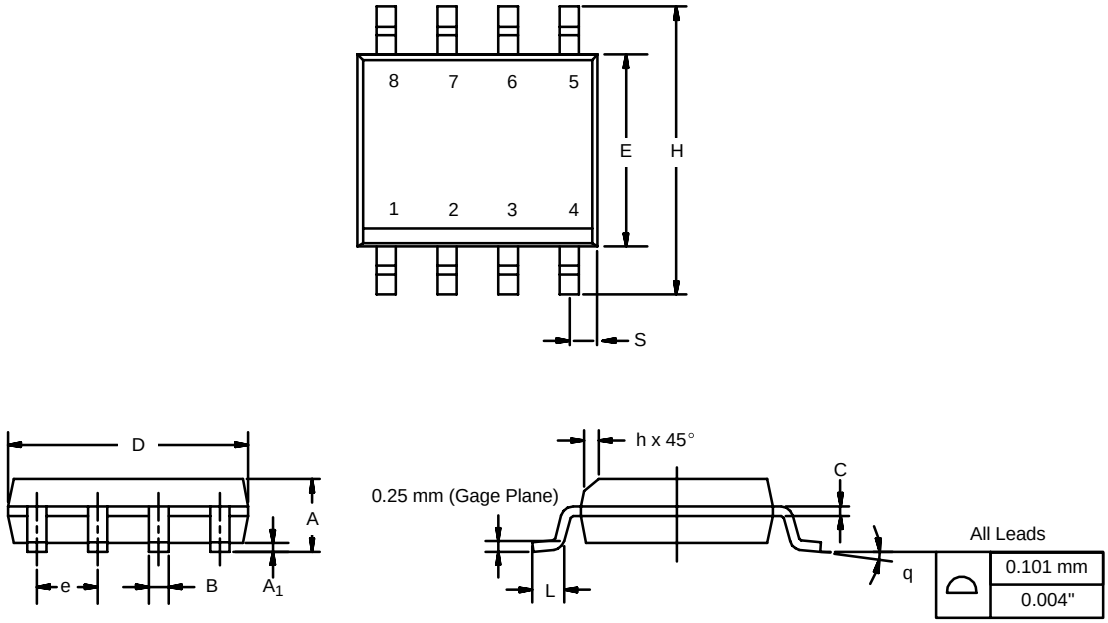


Normalized Thermal Transient Impedance, Junction-to-Ambient



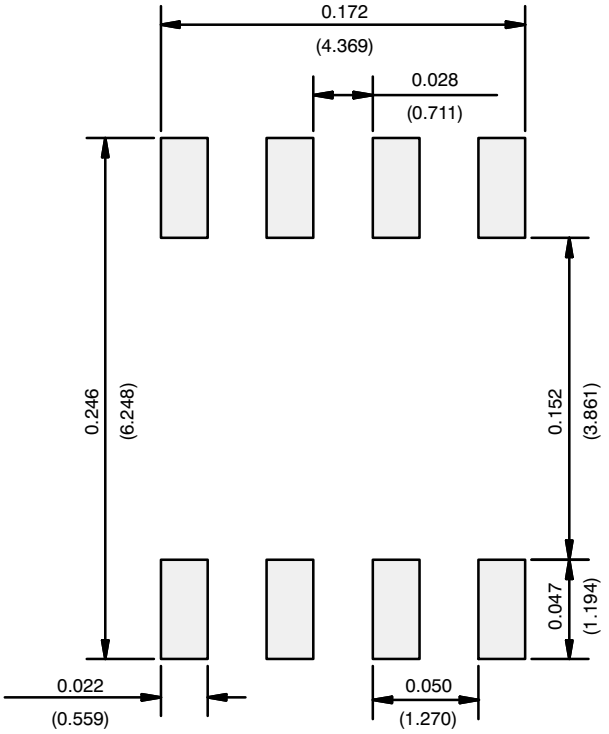
Normalized Thermal Transient Impedance, Junction-to-Foot

SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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