Triple Outputs Switching Converter for AMOLED Display

FEATURES

- Input voltage: 2.5V ~ 4.8V
- Excellent line and load transient response
- Programmable output voltage by ESWIRE from 4.6V to 5V in 100mV steps (Default: 4.6V)
- Programmable output voltage by ESWIRE from -6.6V to -0.5V in 100mV steps (Default: -4V)
- Programmable output voltage by ASWIRE from 6.5V to 8.0V in 50mV (SET=H) or in 100mV (SET=L) steps (Default: 7.6V)
- Max Output current for ELVDD and ELVSS
- **800mA @ V_{IN}=2.5V, ELVDD=4.6V, ELVSS= -4.0V**
- **900mA @ V_{IN}=2.9V, ELVDD=4.6V, ELVSS= -4.5V**
- 150mA Max Output current for AVDD
- Short Circuit Protection (SCP)
- WLCSP 2.017X2.017 - 25B

APPLICATIONS

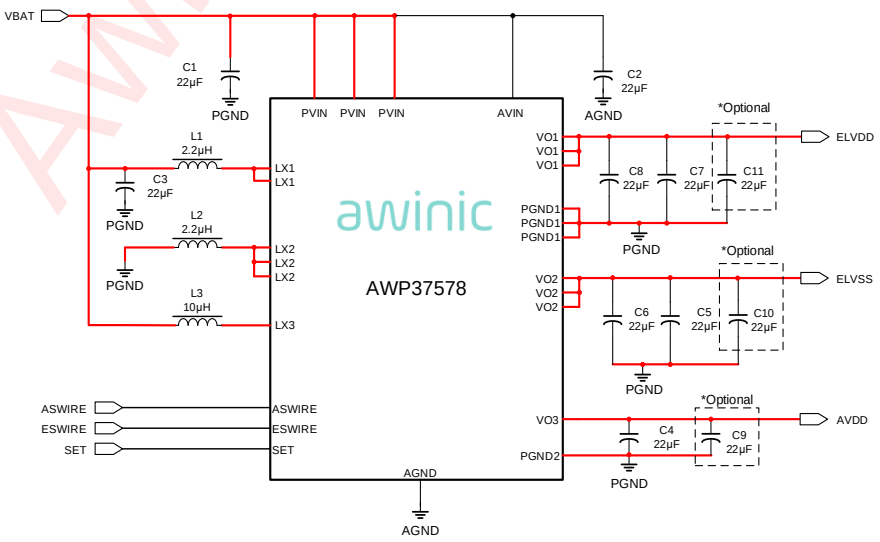
Active Matrix OLED

GENERAL DESCRIPTION

The AWP37578CSR is specially designed for AMOLED (Active Matrix organic LED) Display panels. It integrates two high performance boost converters, VO1 (positive voltage ELVDD) and VO3 (AVDD), one inverting buck-boost converter for VO2 (negative voltage ELVSS). These converters have excellent line and load transient response.

The VO3 can be programmed by ASWIRE, the VO1 and VO2 can be programmed by ESWIRE. All these interfaces can turn on/off corresponding converters.

TYPICAL APPLICATION CIRCUIT



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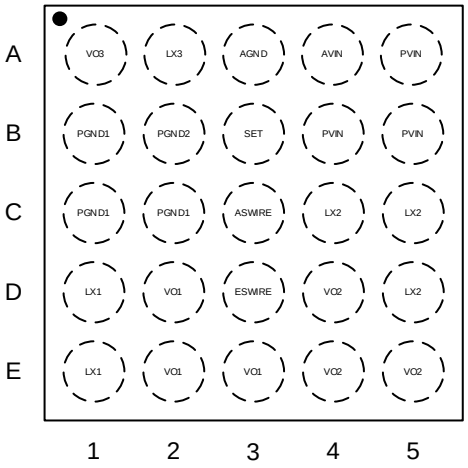
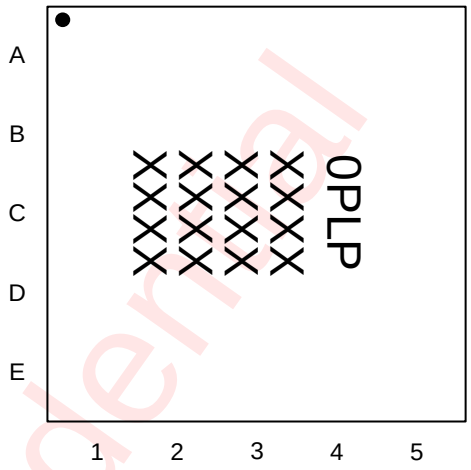
PIN CONFIGURATION AND TOP MARK

AWP37578CSR
(Top View)



AWP37578CSR Marking
(Top View)



0PLP - AWP37578CSR
XXXX/XXXX/XXXX/XXXX - Production Tracing Code

PIN DEFINITION

Ball No.	Symbol	I/O	Description
D1, E1	LX1	Output	Switching node of ELVDD Boost converter
D2, E2, E3	VO1	Output	Output voltage of ELVDD Boost converter
B1, C1, C2	PGND1	GND	Power ground for ELVDD Boost converter
C4, C5, D5	LX2	Output	Switching node of ELVSS inverting Buck-Boost converter
D4, E4, E5	VO2	Output	Output voltage of ELVSS inverting Buck-Boost converter
A5, B4, B5	PVIN	Input	Input supply voltage for Power
A2	LX3	Output	Switching node of AVDD Boost converter
A1	VO3	Output	Output voltage of AVDD Boost converter
B2	PGND2	GND	Power ground for AVDD Boost converter
A4	AVIN	Input	Input supply voltage for analog
A3	AGND	GND	Analog ground
D3	ESWIRE	Input	S-wire control input (Active-High) for ELVDD and ELVSS
C3	ASWIRE	Input	S-wire control input (Active-High) for AVDD
B3	SET	Input	GPIO input to select AVDD output voltage range and steps

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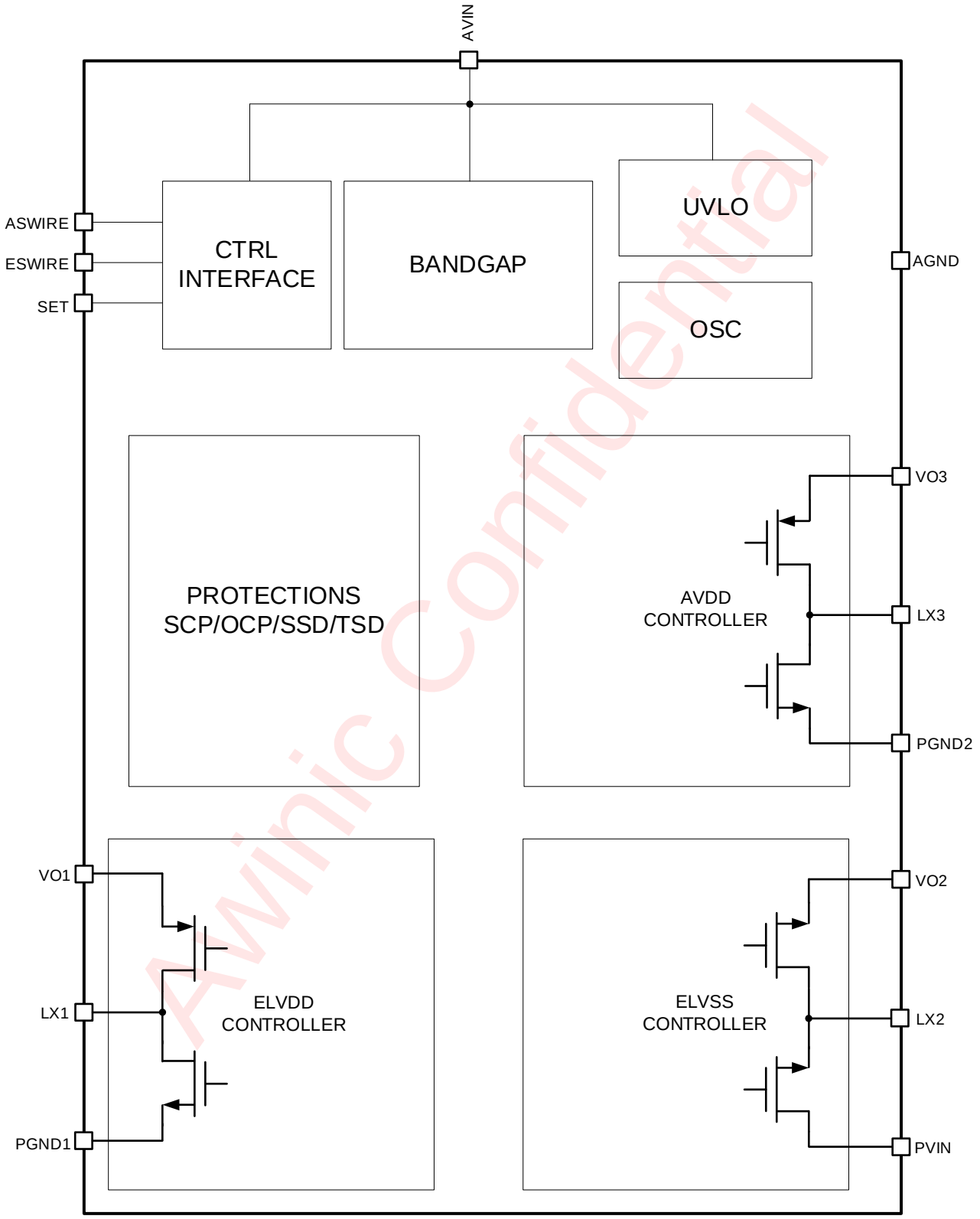
FUNCTIONAL BLOCK DIAGRAM



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ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWP37578CSR	-40°C ~ 85°C	WLCSP 2.017X2.017 - 25B	0PLP	MSL1	RoHS+HF	4500 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS		RANGE
Supply voltage range AVIN, PVIN		-0.3V to 6V
Input voltage range	ASWIRE, ESWIRE, SET	-0.3V to 6V
Output voltage range	VO1	-0.3V to 6V
	LX1	-0.3V to 7V
	VO3	-0.3V to 10V
	LX3	-0.3V to VO3+0.3V
	VO2	-8V to 0.3V
	LX2	-8V to PVIN+0.3V
Junction-to-ambient thermal resistance θ_{JA}		58°C/W
Operating free-air temperature range T_A		-40°C to 85°C
Operating junction temperature range T_J		-40°C to 125°C
Maximum operating junction temperature T_{JMAX}		165°C
Storage temperature T_{STG}		-65°C to 160°C
Lead temperature (soldering 10 seconds)		260°C
ESD(Including HBM CDM)(NOTE 2)		
HBM		±2kV
CDM		±1.5kV
Latch-Up		
Test standard: JESD78F		+IT：+200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2023(HBM). ESDA/JEDEC JS-002-2022(CDM).

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Recommended Operating Conditions

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{IN}	Input voltage		2.5	3.7	4.8	V
C_{IN}	Input capacitance		40	66		μF
C_{OUT}(NOTE 3)	Output capacitance	C_{OUT} of VO1	44			μF
		C_{OUT} of VO2	44			μF
		C_{OUT} of VO3	22			μF
L_1(NOTE 4)	Inductance for VO1			2.2		μH
				4.7		μH
L_2(NOTE 4)	Inductance for VO2			2.2		μH
				1.0		μH
L_3(NOTE 4)	Inductance for VO3			10		μH
				4.7		μH
T_A	Operating free-air temperature range		-40	25	85	°C

NOTE3: The minimum value of the required capacitor for 900mA load at V_{VO1}= 4.6V or V_{VO2} = -4.0V is 13.2μF and for 150mA load at V_{VO3} = 7.6V is 3.9μF. In order to improve the stability at lower input voltage and heavy loads, it is recommended that another 22μF capacitor be added to the VO outputs.

NOTE4: In addition to typical application, AWP37578CSR can supports L1 = 4.7μH, L2 = 1.0μH and L3 = 4.7μH.

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ELECTRICAL CHARACTERISTICS

AVIN = PVIN = 3.7V, V_{VO1} = 4.6V, V_{VO2} = -4V, V_{VO3} = 7.6V, typical values are at T_A = T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT AND THERMAL PROTECTION						
AVIN, PVIN	Input voltage range		2.5	3.7	4.8	V
I_{SD}	Shutdown current	ASWIRE = ESWIRE = GND, total current flowing into AVIN and PVIN			1.5	μA
I_Q	Quiescent current	ASWIRE = ESWIRE = HIGH, total current flowing into AVIN and PVIN			6	mA
V_{UVLO}	Under-voltage lockout threshold	AVIN Falling	1.75	2.05	2.15	V
		AVIN Rising	1.85	2.15	2.25	V
T_{SD}	Thermal shutdown temperature	Temperature Rising		165		°C
ELVDD BOOST CONVERTER(VO1)						
V_{VO1}	Output voltage		4.6	4.6	5	V
	Output voltage accuracy	No load	-0.5		0.5	%
		No load, T_A = -40°C to +85°C	-0.8		0.8	%
I_{O1MAX}(NOTE 5)	Maximum Output Current	AVIN = PVIN = 2.5V ~ 4.8V, V_{VO2}= -4.0V	800			mA
		AVIN = PVIN = 2.9V ~ 4.8V, V_{VO2}= -4.5V	900			mA
R_{DSONS}	Switch on-resistance	I_{DS} = 200mA		80		mΩ
R_{DSONR}	Rectifier on-resistance			60		mΩ
f_{SW1}	Switching frequency			1.45		MHz
			-10		10	%
I_{LIMIT1}	Switch current limit	Inductor peak current	2.8	3.5		A
V_{SCP1}	Short-circuit threshold in operation	Voltage decrease from nominal V_{VO1}		0.9x V_{VO1}		V
t_{SCP1}	Short-circuit detection time in operation			1		ms
R_{DCHG1}	Discharge resistance	FD = ON, I_{O1} = 1mA	30	50	70	Ω
Line Regulation	$V_{VO1\_LINEREG}$	I_{O1} = 100mA, V_{IN} = 2.5V to 4.8V		10		mV
Load Regulation	$V_{VO1\_LOADREG}$	I_{O1} = 1mA ~ 900mA		25		mV
ELVSS INVERTING BUCK-BOOST CONVERTER (VO2)						
V_{VO2}	Output voltage range		-6.6	-4.0	-0.5	V
	Output voltage accuracy	No load	-25		25	mV
		No load, T_A = -40°C to +85°C	-40		40	mV
I_{O2MAX}(NOTE 5)	Maximum Output Current	AVIN = PVIN = 2.5V ~ 4.8V, V_{VO2}= -4.0V			-800	mA
		AVIN = PVIN = 2.9V ~ 4.8V, V_{VO2}= -4.5V			-900	mA
R_{DSONS}	Switch on-resistance	I_{DS} = 200mA		45		mΩ
R_{DSONR}	Rectifier on-resistance			45		mΩ

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW2}	Switching frequency			1.45		MHz
			-10		10	%
I_{LIMIT2}	Switch current limit	AVIN = PVIN = 2.5 V	4.8	5.8		A
R_{DCHG2}	Discharge resistance	FD = ON, I_{O2} = 1 mA	30	50	70	Ω
V_{SCP2}	Short circuit threshold in operation	Voltage increase from nominal V_{VO2}		0.8x V_{VO2}		V
t_{SCP2}	Short circuit detection time in operation			1		ms
V_{SSD}	Start-up short detection threshold			200		mV
t_{SSD}	Start-up short detection time			5		ms
Line Regulation	$V_{VO2\_LINEREG}$	I_{O2} = 100mA, V_{IN} = 2.5V to 4.8V		10		mV
Load Regulation	$V_{VO2\_LINEREG}$	I_{O2} = 1mA ~ 900mA		25		mV
AVDD BOOST CONVERTER (VO3)						
V_{VO3}	Output voltage	SET = HIGH (step: 50mV)	6.5	7.6	8.0	V
		SET = LOW (step: 100mV)	6.5	7.6	8.0	V
	Output voltage accuracy	No load	-0.8		0.8	%
		No load, T_A= -40°C to +85°C	-1.0		1.0	%
I_{O3MAX}	Maximum Output Current	AVIN = PVIN = 2.5V ~ 4.8V	150			mA
R_{DSONS}	Switch on-resistance	I_{DS} = 30mA		300		mΩ
R_{DSONR}	Rectifier on-resistance			500		mΩ
f_{SW3}	Switching frequency			1.45		MHz
			-10		10	%
I_{LIMIT3}	Switch current limit	Inductor peak current	0.8	1.0		A
R_{DCHG3}	Discharge resistance	FD = ON, I_{O3} = 1 mA	40	70	100	Ω
V_{SCP3}	Short-circuit threshold in operation	Voltage decrease from nominal V_{VO3}		0.8x V_{VO3}		V
t_{SCP3}	Short-circuit detection time in operation			1		ms
Line Regulation	$V_{VO3\_LINEREG}$	I_{O3} = 50mA, V_{IN} = 2.5V to 4.8V		5		mV
Load Regulation	$V_{VO3\_LINEREG}$	I_{O3} = 1mA ~ 150mA		10		mV
LOGIC SET						
V_{IH}	High level input voltage	AVIN = PVIN = 2.5V ~ 4.8V	0.84			V
V_{IL}	Low level input voltage	AVIN = PVIN = 2.5V ~ 4.8V			0.36	V
CTRL INTERFACE (ASWIRE,ESWIRE)						
V_{IH}	High level input voltage	AVIN = PVIN = 2.5V ~ 4.8V	0.84			V
V_{IL}	Low level input voltage	AVIN = PVIN = 2.5V ~ 4.8V			0.36	V
R_{SWIRE}	Pull down resistance of ASWIRE and ESWIRE interfaces	V_{SWIRE}=1.8V		300		kΩ

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{LOW}(NOTE 6)	Low-level pulse duration		2	10	25	μs
t_{HIGH}(NOTE 6)	High-level pulse duration		2	10	25	μs
t_{OFF}(NOTE 6)	Shutdown pulse duration (ASWIRE/ESWIRE = low)		200			μs
t_{INIT}(NOTE 6)	Initialization time			400	500	μs
t_{STORE}(NOTE 6)	Data storage/accept time period		160			μs
POWER SEQUENCE						
t_{DELAY}(NOTE 6)	VO2 start up time delay VO1			5		ms
t_{SS1}(NOTE 6)	VO1 soft-start time			3		ms
t_{SS2}(NOTE 6)	VO2 soft-start time			3		ms
t_{SS3}(NOTE 6)	VO3 soft-start time			3		ms

NOTE5: The specific parameters of the peripheral inductors are as follows:

L1: DFE252012F-2R2M=P2 3.3A, 82mΩ, 252012 L2: DFE252012F-2R2M=P2 3.3A, 82mΩ, 252012

L3: DFE252012F-100M=P2 1.4A, 480mΩ, 252012

Test Condition: Ambient temperature is 60°C, the load current is only between the VO1 and VO2, VO3 is no load, AWP37578CSR works stably in laboratory test environment.

NOTE6: Guaranteed by design characterization and correlation with process controls. Not fully test in production.

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TYPICAL CHARACTERISTICS

AVIN = PVIN = VIN = 3.7V, V_{VO1}= 4.6V, V_{VO2}= -4V, V_{VO3}= 7.6V, L1= 2.2μH, L2= 2.2μH, L3= 10μH. Typical values are at T_A = T_J = 25°C (unless otherwise noted)

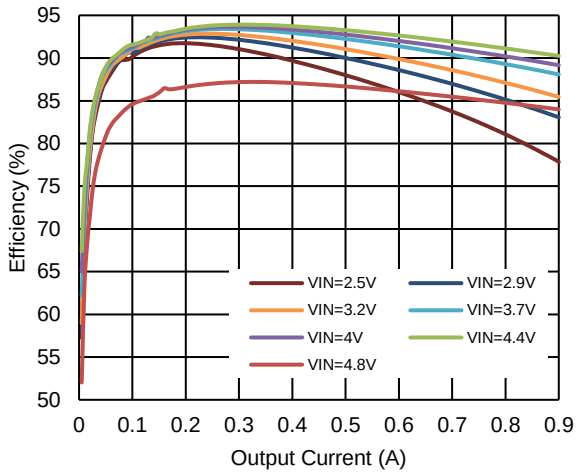

Figure 1. VO1 and VO2 Combined Efficiency

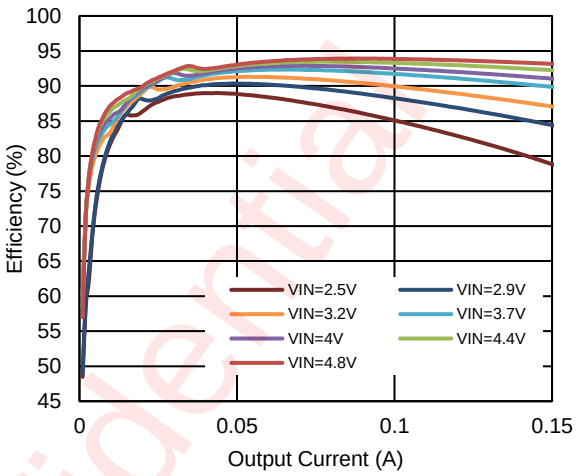

Figure 2. VO3 Efficiency

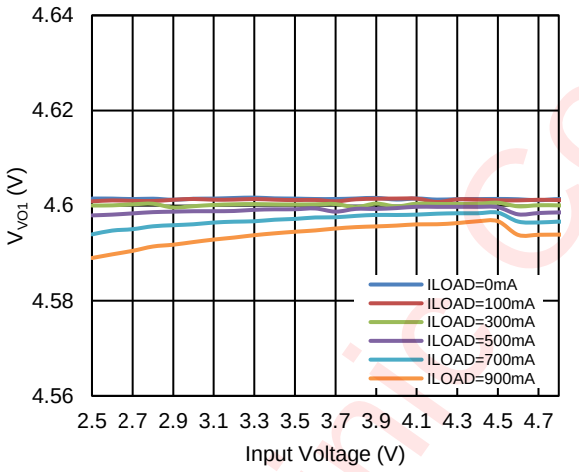

Figure 3. VO1 Line Regulation

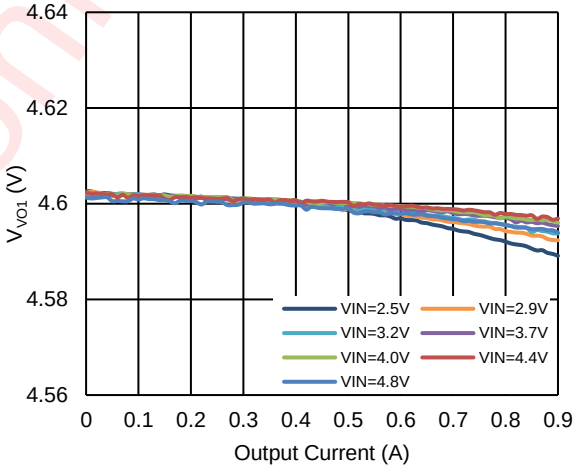

Figure 4. VO1 Load Regulation

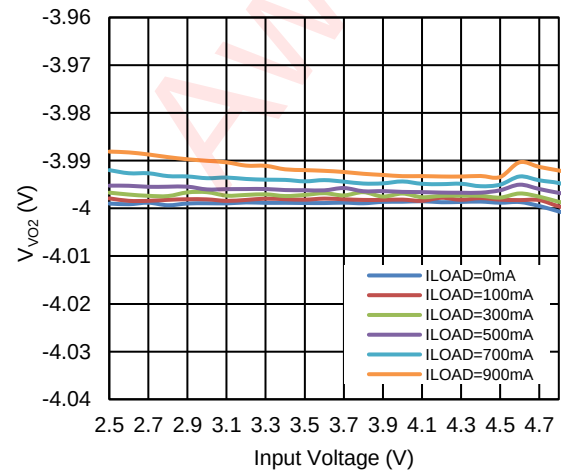

Figure 5. VO2 Line Regulation

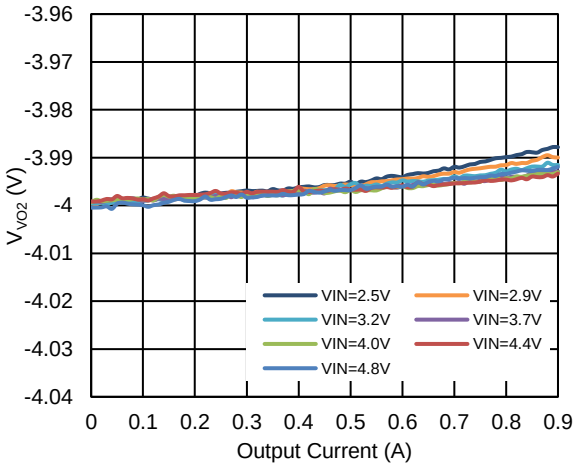

Figure 6. VO2 Load Regulation

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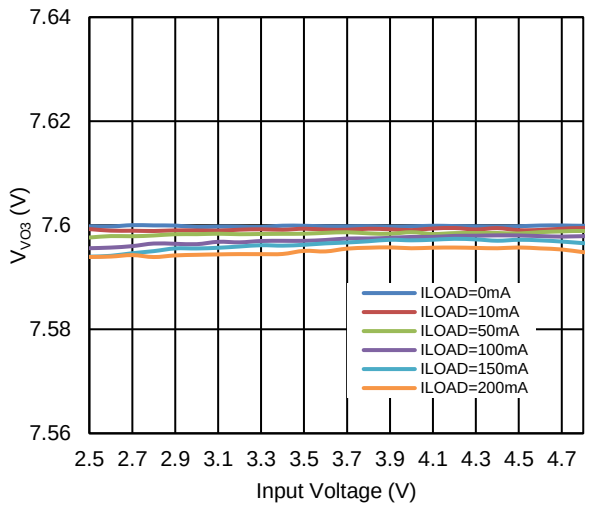

Figure 7. VO3 Line Regulation

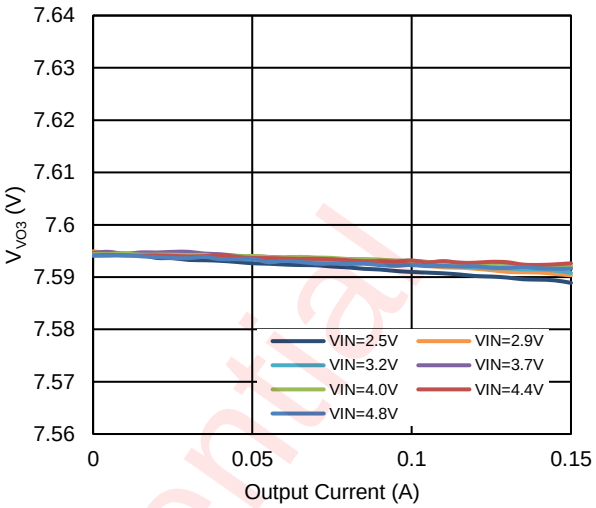

Figure 8. VO3 Load Regulation

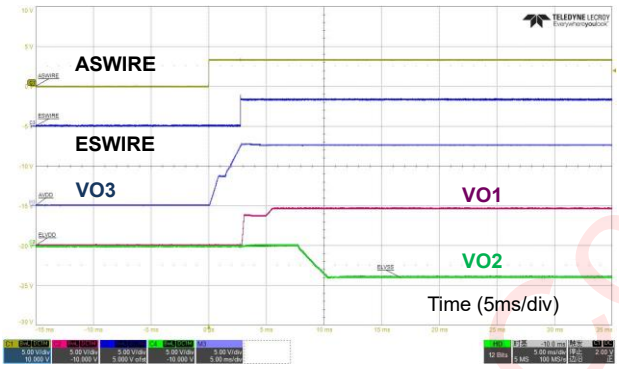

Figure 9. Start up Sequence
(ASWIRE starts 3ms before ESWIRE)

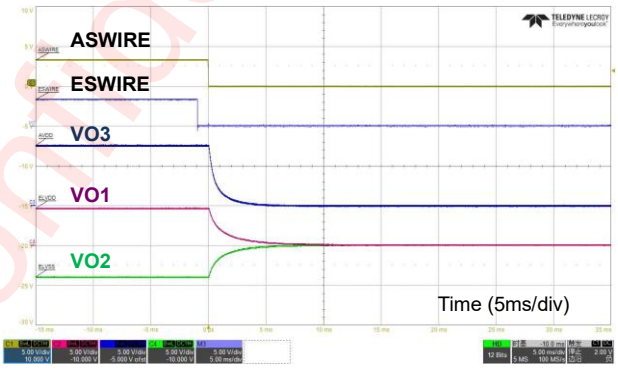

Figure 10. Shut down Sequence with FD ON
(ESWIRE stops 3ms before ESWIRE)

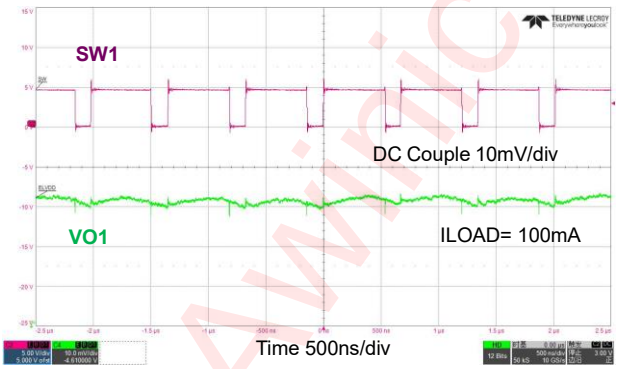

Figure 11. VO1 Switching and Output Waveforms at light load

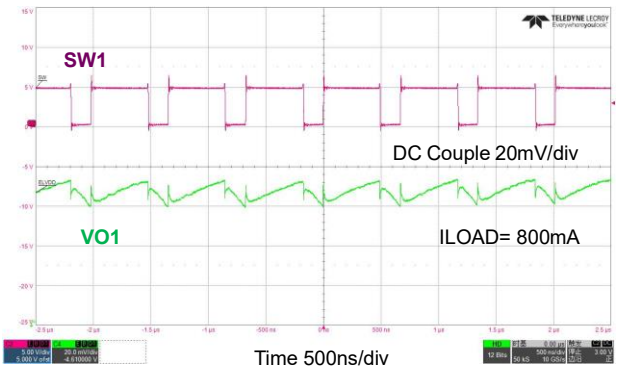

Figure 12. VO1 Switching and Output Waveforms at heavy load

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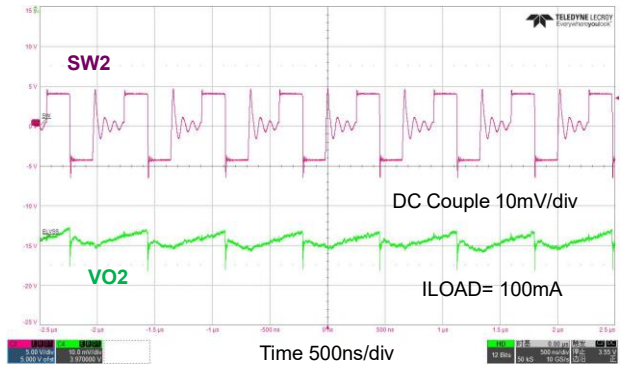

Figure 13. VO2 Switching and Output Waveforms at light load

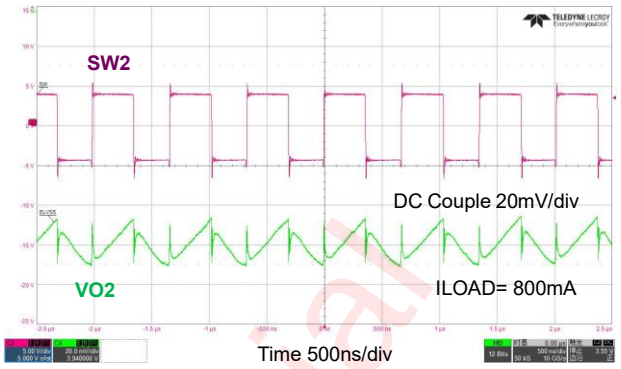

Figure 14. VO2 Switching and Output Waveforms at heavy load

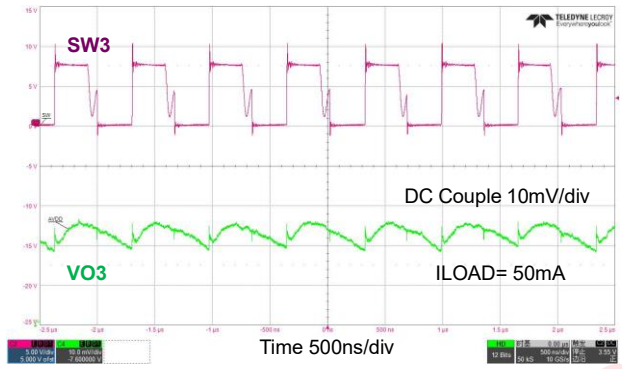

Figure 15. VO3 Switching and Output Waveforms at light load

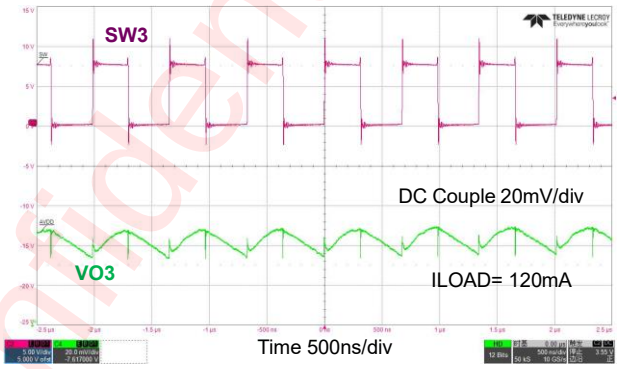

Figure 16. VO3 Switching and Output Waveforms at heavy load

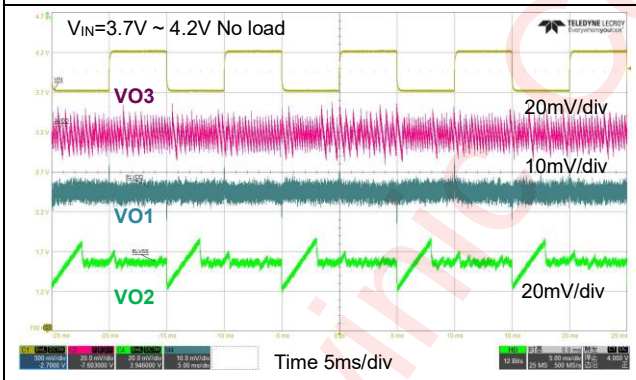

Figure 17. Line transient at No load

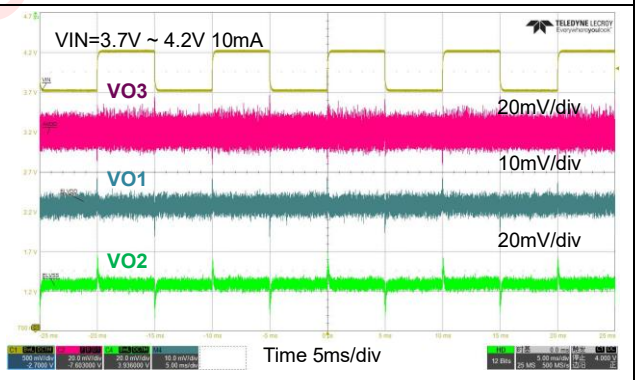

Figure 18. Line transient at light load (10mA)

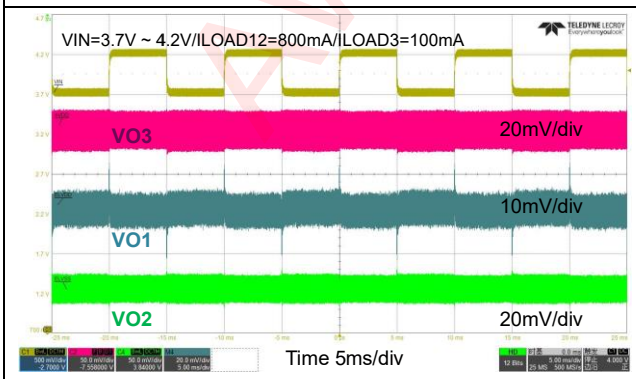

Figure 19. Line transient at heavy load

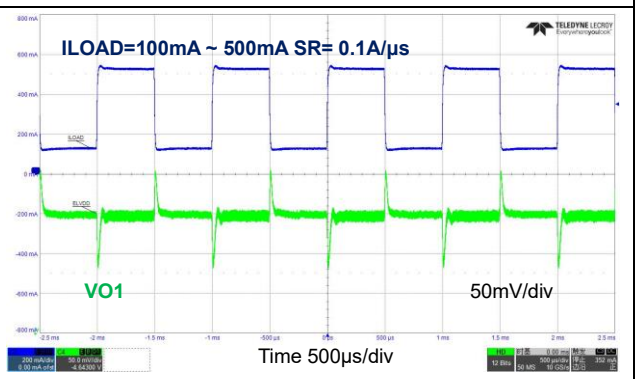

Figure 20. VO1 load transient (100~500mA/SR=0.1A/μs)

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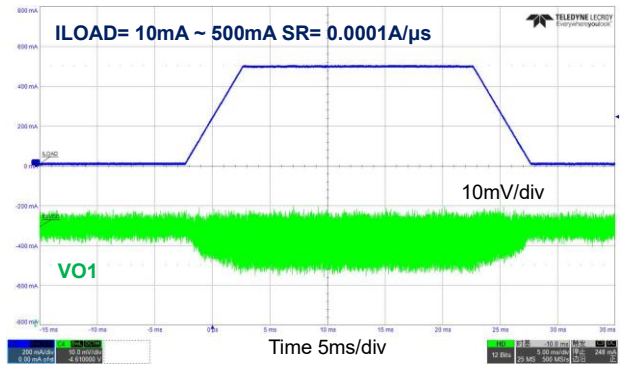

Figure 21. VO1 load transient (10~500mA/SR=0.0001A/μs)

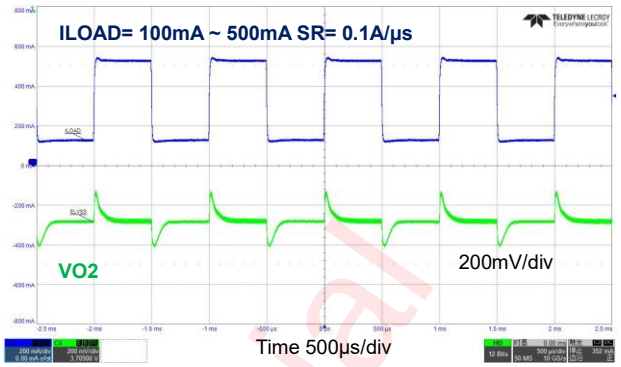

Figure 22. VO2 load transient (100~500mA/SR=0.1A/μs)

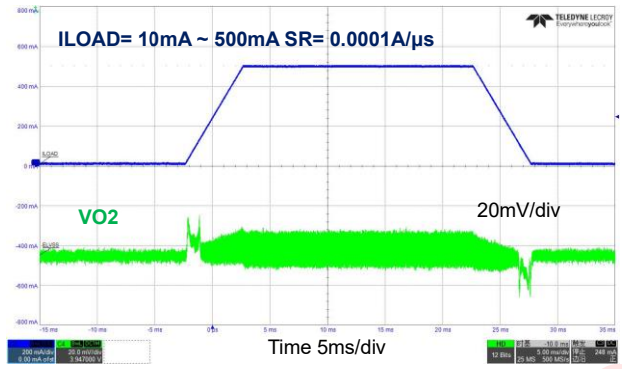

Figure 23. VO2 load transient (10~500mA/SR=0.0001A/μs)

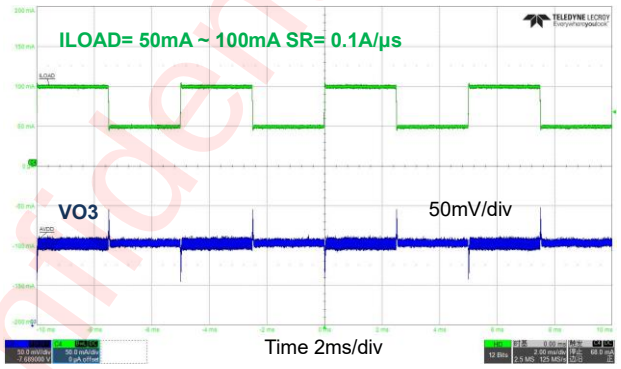

Figure 24. VO3 load transient (50~100mA/SR=0.1A/μs)

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DETAILED FUNCTIONAL DESCRIPTION

Sequence

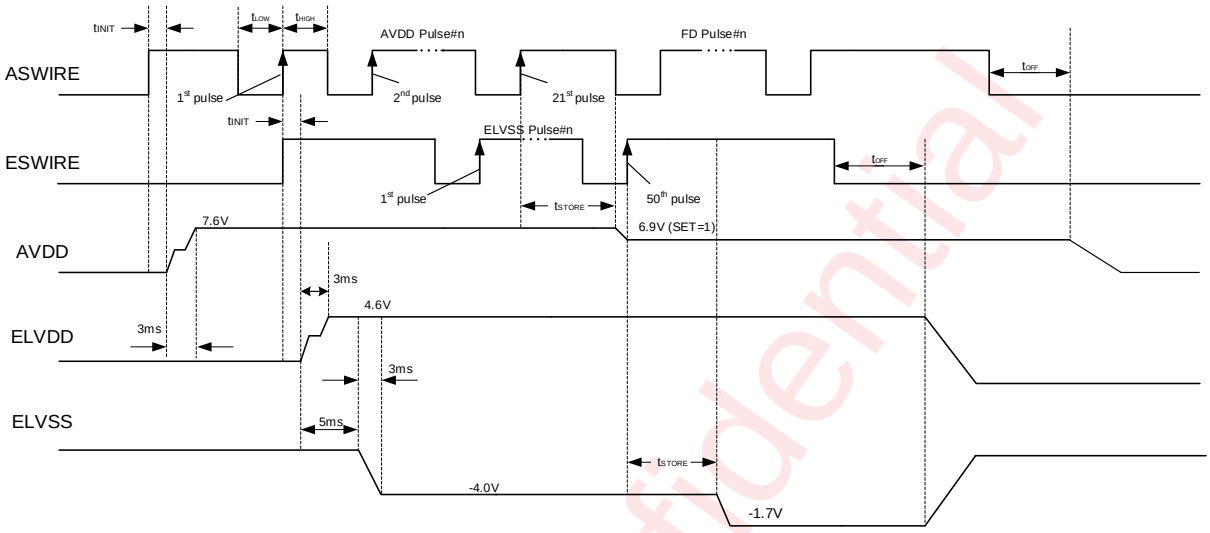

Figure 25. Timing diagram

The AVDD boost converter operates with a cycle-by-cycle peak current limit topology and fixed 1.45MHz frequency. The AVDD output voltage can be programmed through ASWIRE interface, and the output voltage table can be changed by the condition of SET interface. When SET = LOW, AVDD is available from 6.5V to 8.0V with 100mV steps, while SET = HIGH, AVDD is available from 6.5V to 8.0V with 50mV steps. The programming table of AVDD output voltage is shown in Table 1.

The AVDD boost converter begins soft-start to its default voltage 7.6V with a t_{INIT} time delay after the ASWIRE logic level goes high. The soft-start lasts for 3ms typically.

The AVDD output voltage is programmable by applying different pulses to ASWIRE interface, which counts the rise edges, plus a high logic level to ASWIRE lasts longer than a t_{STORE} time is detected after controll pulses stop, AVDD starts altering to the target voltage. The AVDD boost converter turns off with a t_{OFF} time delay after the logic level of ASWIRE interface goes from high to low.

Table 1 Programming of AVDD output voltage

SET=0		SET=1	
ASWIRE Pulse	**AVDD**	**ASWIRE Pulse**	**AVDD**
0	**7.6V**	**0**	**7.60V**
1	7.8V	1	7.90V
2	7.7V	2	7.85V
3	**7.6V**	3	7.80V
4	7.5V	4	7.75V
5	7.4V	5	7.70V
6	7.3V	6	7.65V

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SET=0		SET=1	
ASWIRE Pulse	**AVDD**	**ASWIRE Pulse**	**AVDD**
7	7.2V	**7**	**7.60V**
8	7.1V	8	7.55V
21	7.0V	9	7.50V
22	6.9V	10	7.45V
23	6.8V	11	7.40V
24	6.7V	12	7.35V
25	6.6V	13	7.30V
26	6.5V	14	7.25V
37	8.0V	15	7.20V
38	7.9V	16	7.15V
		17	7.10V
		18	7.05V
		19	7.00V
		20	6.95V
		21	6.90V
		40	6.85V
		41	6.80V
		42	6.75V
		43	6.70V
		44	6.65V
		45	6.60V
		46	6.55V
		47	6.50V
		68	8.00V
		69	7.95V

The inverting buck-boost and boost converters both operate with a cycle-by-cycle peak current limit topology and fixed 1.45MHz frequency. The ELVSS output voltage can be programmed from -6.6V to -0.5V with 100mV steps. The programming table of ELVSS output voltage is shown in Table 2. The ELVDD output voltage can be programmed from 4.6V to 5.0V with 100mV steps by ESWIRE interface as well. The programming table of ELVDD output voltage is shown in Table 3.

The ESWIRE interface controls the on and off state of ELVDD and ELVSS. The ELVDD boost converter begins soft-start to its default voltage 4.6V with a t_{INIT} time delay after the ESWIRE logic level goes high. The ELVSS buck-boost converter with -4V default value starts to operate 5ms later than the ELVDD boost converter. Both

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converters are implemented with a 3ms soft-start to limit the inrush current. When ESWIRE interface goes low for t_{OFF} time, the ELVDD and ELVSS converters stop operation simultaneously.

The ELVDD and ELVSS output voltage both are programmable by applying different pulses to ESWIRE interface, which also counts the rise edges, plus a high logic level of ESWIRE lasts longer than a t_{STORE} time is detected after controll pulses stop, the ELVDD and ELVSS outputs start altering to the target voltage.

Table 2 Programming of ELVSS output voltage

ESWIRE Pulse	ELVSS	ESWIRE Pulse	ELVSS
0	**-4.0V**	31	-3.6V
1	-6.6V	32	-3.5V
2	-6.5V	33	-3.4V
3	-6.4V	34	-3.3V
4	-6.3V	35	-3.2V
5	-6.2V	36	-3.1V
6	-6.1V	37	-3.0V
7	-6.0V	38	-2.9V
8	-5.9V	39	-2.8V
9	-5.8V	40	-2.7V
10	-5.7V	41	-2.6V
11	-5.6V	42	-2.5V
12	-5.5V	43	-2.4V
13	-5.4V	44	-2.3V
14	-5.3V	45	-2.2V
15	-5.2V	46	-2.1V
16	-5.1V	47	-2.0V
17	-5.0V	48	-1.9V
18	-4.9V	49	-1.8V
19	-4.8V	50	-1.7V
20	-4.7V	51	-1.6V
21	-4.6V	52	-1.5V
22	-4.5V	53	-1.4V
23	-4.4V	54	-1.3V
24	-4.3V	55	-1.2V
25	-4.2V	56	-1.1V
26	-4.1V	57	-1.0V

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ESWIRE Pulse	ELVSS	ESWIRE Pulse	ELVSS
27	**-4.0V**	58	-0.9V
28	-3.9V	59	-0.8V
29	-3.8V	60	-0.7V
30	-3.7V	61	-0.6V
		62	-0.5V

Table 3 Programming of ELVDD output voltage

ESWIRE Pulse	ELVDD
0/no pulse	**4.6V**
71	**4.6V**
76	5.0V
77	4.9V
78	4.8V
79	4.7V

ELVSS Transition

AWP37578CSR also has the slew rate control during the transition of the ELVSS output voltage, which aims to accomplish smooth voltage changes. The ramp time is 100μs typically, step is 100mV (Actually ramp step is 12.5 mV/12.5 μs). The wider the transition range of the ELVSS output voltage, the longer the transition time.

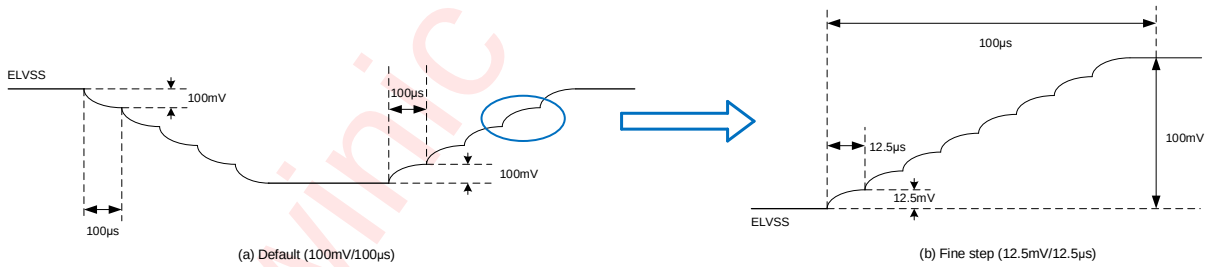

Figure 26. The output voltage of ELVSS transition time

Maximum Output Current Capacity

AWP37578CSR operates with an input voltage range of 2.5V to 4.8V. However, due to different input and output voltage, the maximum output current capacity is quite different, and also affected by peripheral inductors and capacitors, additional input capacitors are recommended for lower input supply voltage.

EMI Description

AWP37578CSR can configured the SW edge rate by applying different pulses to ESWIRE interface, the default is fastest, the pulse numbers are shown in Table 4. Slower SW edge rate can optimize RF interference, at the same time the efficiency will be decreased. If SW edge rate configuration is required, it is recommended to send ESWIRE pulse after the soft-start completion of the output voltage of ELVDD and ELVSS.

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Table 4 Programming of SW edge rate

ESWIRE Pulse	SW edge rate
0/no pulse	**fastest**
86	slow
87	fast
88	faster
89	**fastest**

Under Voltage Lock-Out

Under Voltage Lock-Out (UVLO) is implemented to detect the input voltage AVIN. Once AVIN drops below UVLO falling threshold, all of the three converters (AVDD, ELVDD and ELVSS) stop switching; If AVIN increases above UVLO rising threshold, the three converters restart switching and resume to their previous settings.

Start-up Short Detection (SSD)

The start-up short detection block detects the ELVSS output voltage to monitor whether ELVSS and ELVDD are short connected. If the ELVSS output voltage is pulled up to 0.2V in 5ms after ESWIRE interface goes high, SSD function is triggered and the ELVDD and ELVSS converters shut down immediately. FD function is on at the same time. Resetting the power supply or pulling the ESWIRE interface low for more than a t_{OFF} time can restart the device.

SSD function is enabled and disabled by the pulse numbers of ASWIRE interface. Number of controll pulse is set differently depending on the logic condition of SET interface. SSD function is off by default, the pulse numbers are shown in Table 5.

Table 5 ASWIRE pulses for SSD function

SET=0		SET=1	
ASWIRE Pulse	**SSD**	**ASWIRE Pulse**	**SSD**
0/no pulse	**OFF**	**0/no pulse**	**OFF**
9	OFF	22	OFF
10	ON	23	ON

Fast discharge (FD)

The output voltage (AVDD, ELVDD and ELVSS) fast discharge function is enabled and disabled by the pulse numbers of ASWIRE interface. Number of controll pulse is set differently depending on the logic condition of SET interface. The pulse numbers are shown in Table 6, FD function is off by default.

When FD function is active, ASWIRE and ESWIRE both stop, all outputs of the device are always discharged to GND until ASWIRE and ESWIRE start again.

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Table 6 ASWIRE pulses for FD function

SET=0		SET=1	
ASWIRE Pulse	**FD**	**ASWIRE Pulse**	**FD**
0/no pulse	**OFF**	**0/no pulse**	**OFF**
11	ON	25	ON
12	OFF	26	OFF

Short Circuit Protection (SCP)

The short circuit protection block monitors the output voltages of the AVDD, ELVDD and ELVSS converters to protect the device of short connections to ground or overload. When a SCP or overload event occurs, all the three converters shut down and FD function is enabled simultaneously. Only resetting the power supply or both pulling the ASWIRE and ESWIRE interface to low at the same time for more than a t_{OFF} time can restart the device.

An SCP or overload event occurs in the following cases:

(1) After the output voltages of all the three converters are properly established, ELVDD output voltage falls below 90% of the target voltage and lasts for 1ms; ELVSS and AVDD output voltage falls below 80% of the target voltage and lasts for 1ms;

(2) In soft-start process, V_{ELVDD}, V_{ELVSS} and V_{AVDD} are not in regulation 4ms when ELVDD and ELVSS output voltages begin to establish;

Thermal Shut-Down (TSD)

The Thermal Shut-Down (TSD) function protects the device when overheating occurs. If the IC's junction temperature exceeds 165°C, three converters stop operation. It can not exit this state automatically. Pulling the SWIRE interface to low for more than a t_{OFF} time or a power-cycle on the input supply restarts the device with the default values.

Device Reset

(1) Power resetting resets the device to default settings;

(2) Pulling ASWIRE interface low for t_{OFF} then the output voltage of AVDD is reset to default value of 7.6V;

(3) Pulling ESWIRE interface low for t_{OFF} then the output voltage of ELVDD and ELVSS are reset to default value of 4.6V and -4V.

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PCB LAYOUT CONSIDERATION

It is recommended to follow the below PCB layout guidelines:

1) A common ground plane between AGND and PGND to minimize ground shifts is recommended.

2) Put inductors as close as possible to the device, creating forbidden area under inductors for each PCB layer. Traces of switching nodes (LX1, LX2 and LX3) should be short and wide.

3) Place input capacitors on PVIN and output capacitors on outputs as close as possible to the device.

4) If vias are used for power paths, multiple vias are necessary to obtain lower equivalent resistance on power paths and facilitate heat dissipation.

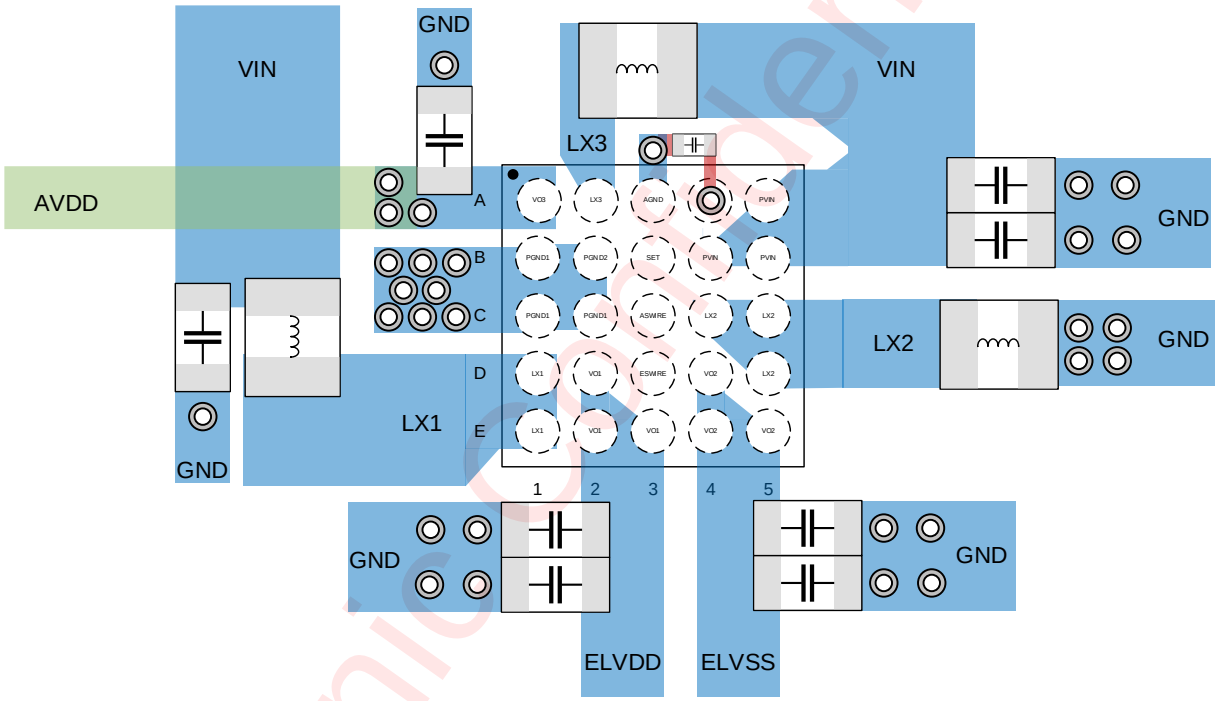

Figure 27. AWP37578 PCB Layout example

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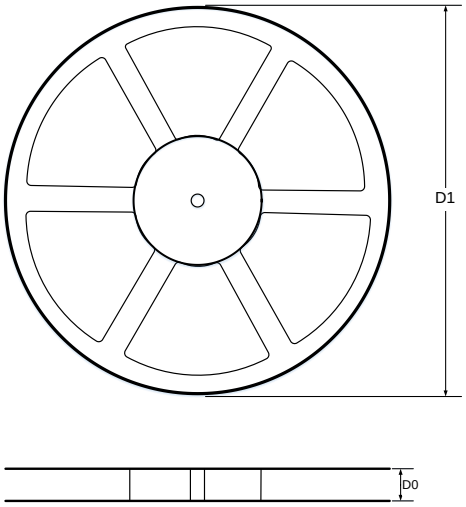
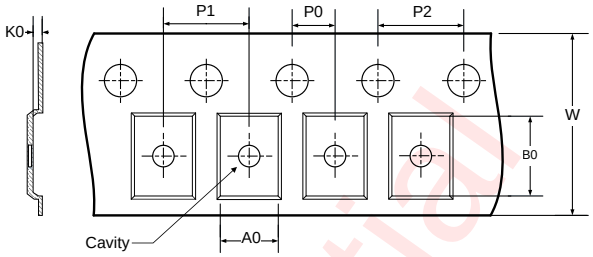
TAPE AND REEL INFORMATION

REEL DIMENSIONS

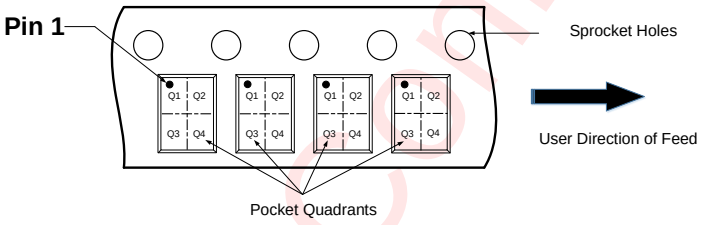


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	2.25	2.25	0.70	2.00	4.00	4.00	8.00	Q1

All dimensions are nominal

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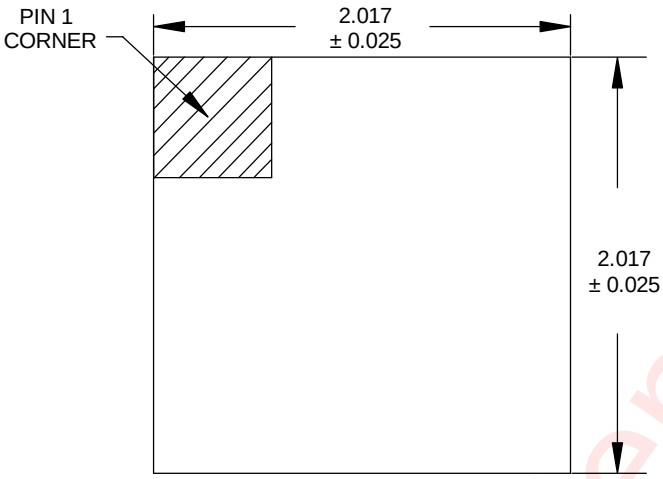
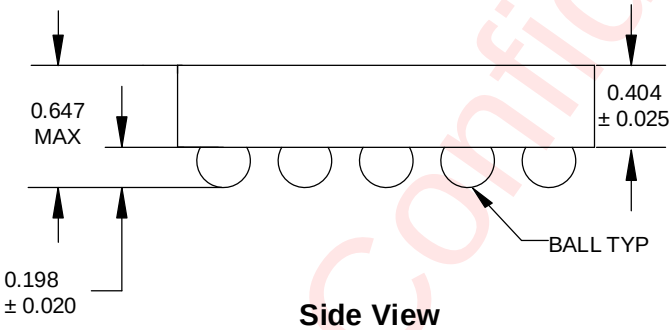
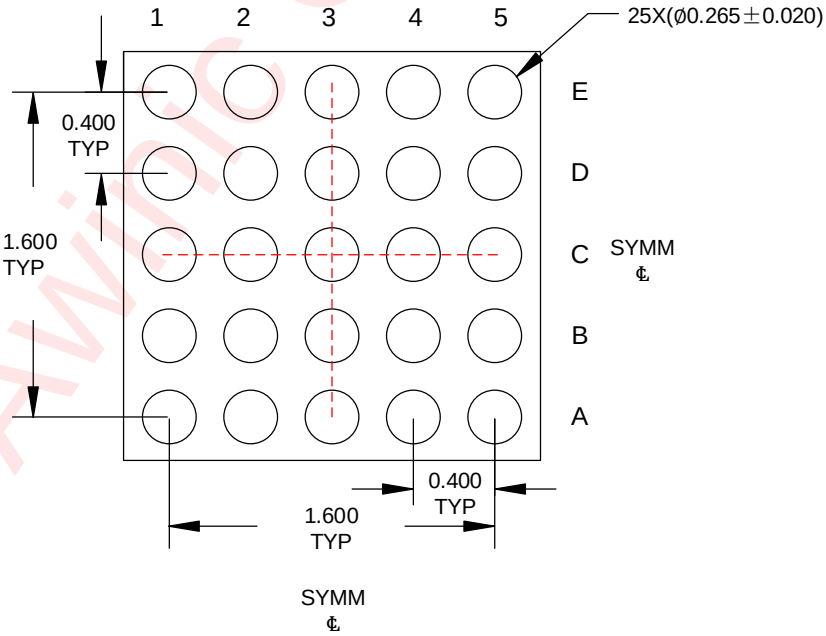
PACKAGE DESCRIPTION



Top View



Side View



Bottom View

Unit: mm

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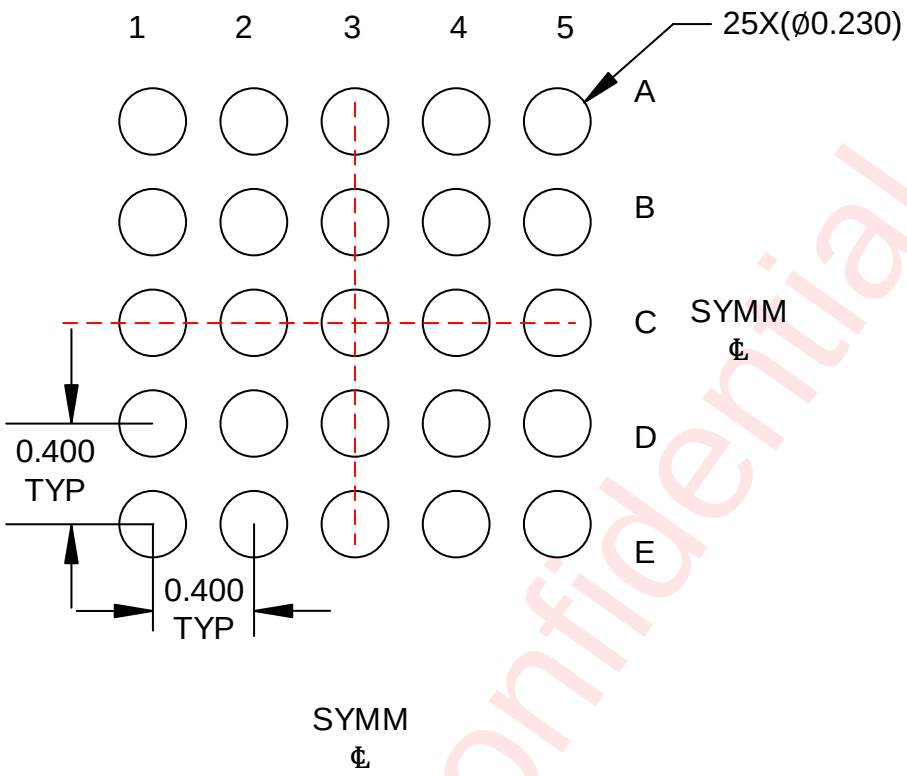
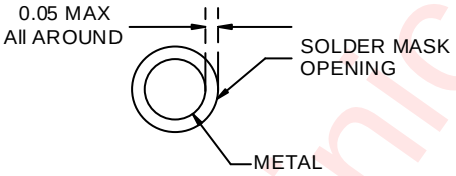
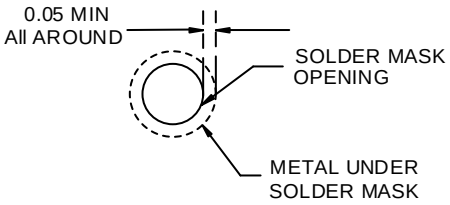
LAND PATTERN DATA





NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

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REVISION HISTORY

Version	Date	Change Record
V1.0	Aug. 2025	Officially released
V1.1	Oct. 2025	1. Added the minimum value of I_{LIMIT1} and I_{LIMIT2} and I_{LIMIT3} (Page6 and Page7) 2. Updated the description of PCB Layout Consideration (Page19)

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