

0.1-5.925GHz SPDT Switch for High Power Applications

Features

- Qualified to AEC-Q100 Grade 2
- Broadband frequency range: 0.1 to 5.925GHz
- High power handling capability of up to 40dBm
- Low insertion loss: 0.66dB typical @ 5.925GHz
- High isolation: 26dB typical @ 5.925GHz
- High switching speed: 1.5 μ s typical
- Low harmonic generation
- Small FCDFN 1.1X0.7-6L package

Applications

- Automotive application
- Multi-Mode GSM/CDMA/WCDMA/LTE and NR including n77, n78, n79 bands
- Cellular modems, tablets and USB Devices
- Other RF front-end modules

General Description

The AW13612PFDR-Q1 is a single-pole dual-throw switch with high power handling capability of up to 40dBm and low insertion loss. It can be used to support band switching and mode switching for GSM, WCDMA, LTE, and NR applications.

The symmetrical design of internal ports makes it convenient for PCB routing and adjustment of receiving and transmitting signals. The band/mode switching is realized by the GPIO pins as referenced in the chip block diagram and the control logic.

The AW13612PFDR-Q1 is provided in a compact FCDFN 1.1X0.7-6L package.

Typical Application Circuit

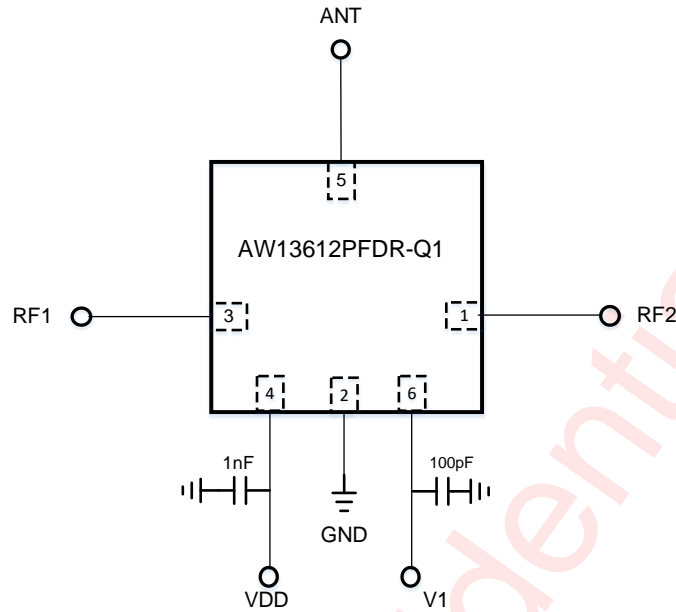
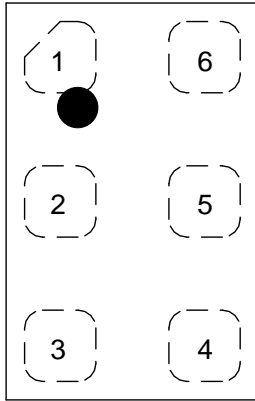


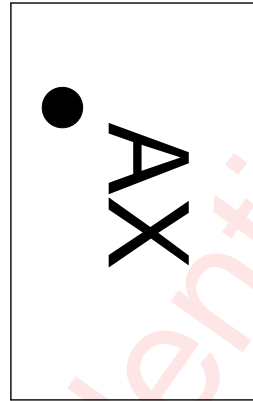
Figure 1 Typical Application Circuit of AW13612PFDR-Q1

Pin Configuration And Top Mark

AW13612PFDR-Q1
(Top view)



AW13612PFDR-Q1 Marking
(Top view)



A - AW13612PFDR-Q1
X - Production Tracing Code

Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	RF2	RF I/O path 2
2	GND	Ground
3	RF1	RF I/O path 1
4	VDD	DC power supply
5	ANT	Antenna port
6	V1	DC control voltage 1

Functional Block Diagram

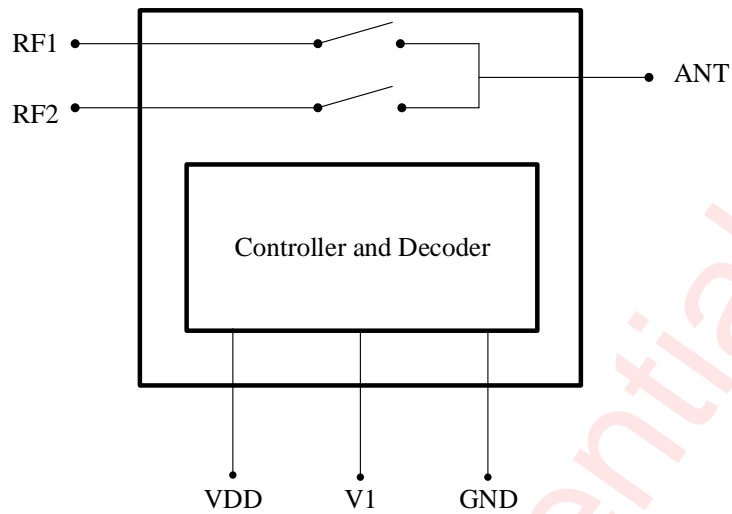


Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW13612PFDR-Q1	-40°C~105°C	FCDFN 1.1X0.7-6L	A	MSL1	ROHS+HF	9000 units/ Tape and Reel

Absolute Maximum Ratings^(NOTE1)

PARAMETERS		RANGE
Supply voltage range VDD		-0.3V to 3.6V
Control Voltage Range	V1	0V to 3.3V
RF input power	GSM 850/900MHz, VSWR=1:1, 25°C	39.5dBm
	GSM 850/900MHz, VSWR=1:1, 105°C	38.5dBm
	GSM 1800/1900MHz, VSWR=1:1, 25°C	40dBm
	GSM 1800/1900MHz, VSWR=1:1, 105°C	39.5dBm
Operating Free-air Temperature Range		-40°C to 105°C
Storage temperature T _{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
HBM ^[2]		±1500V
CDM ^[3]		±1500V

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Reference AEC-Q100-002-RevE.

NOTE3: Reference AEC-Q100-011-RevD.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage	VDD	1.65	1.8	3.3	V
Control Voltage High	V1_H	0.75	1.8	VDD	V
Control Voltage Low	V1_L	0		0.4	V
Operating Temperature	Top	-40	25	105	°C

Electrical Characteristics

VDD=1.8V, V1=0/1.8V, P_{IN}=0dBm, T=+25°C, Z₀=50Ω. (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
IDD	Supply Current	VDD=1.8V		50	80	μA
Tsw	Switching Time	50% CTRL to 90% or 10% RF		1.5	3	μs
IL	Insertion loss	600-960MHz		0.22	0.4	dB
		960-2200MHz ^[1]		0.29	0.5	dB
		2200-2700MHz		0.33	0.55	dB
		3300-4200MHz		0.44	0.65	dB
		4400-5000MHz ^[1]		0.53	0.75	dB
		5150-5925MHz		0.66	0.85	dB
ISO	Isolation, ANT-RFx	600-960MHz	35	41.5		dB
		960-2200MHz ^[1]	31	35.5		dB
		2200-2700MHz	30	34		dB
		3800-4200MHz	25	30.5		dB
		4400-5000MHz ^[1]	22	29		dB
		5150-5925MHz	22	26		dB
RL ^[1]	Return loss	600-960MHz	20	28.5		dB
		960-2200MHz	15	21.5		dB
		2200-2700MHz	14	19.5		dB
		3800-4200MHz	11	15.5		dB
		4400-5000MHz	10	13.5		dB
		5150-5925MHz	10	12		dB
2fo ^[1]	Second harmonics	PIN=34dBm, 850/900MHz, CW, VSWR=1:1		-57	-45	dBm
		PIN=32dBm, 1800/1900MHz, CW, VSWR=1:1		-61	-50	dBm
3fo ^[1]	Third harmonics	PIN=34dBm, 850/900MHz, CW, VSWR=1:1		-74	-60	dBm
		PIN=32dBm, 1800/1900MHz, CW, VSWR=1:1		-79	-65	dBm
IIP2 ^[1]	Input 2nd-order Intercept Point	26dBm@1950MHz, -20dBm@4090MHz	105	117		dBm
IIP3 ^[1]	Input 3rd-order Intercept Point	26dBm@2560MHz, -10dBm@3310MHz	65	79		dBm

[1] Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

Power ON and OFF Sequence

It is very important that the user adheres to the correct power-on/off sequence in order to avoid damaging the device. The control signal V1 should be set to 0V unless VDD is set in the operating voltage range.

Power ON:

- 1) Apply voltage supply --- VDD
- 2) Set Controls---V1
- 3) Apply RF input

Change switch position from one RF port to another:

- 1) Remove RF input
- 2) Change control voltages V1 to set the switch to desired RF port
- 3) Apply RF input

Power OFF:

- 1) Remove RF input
- 2) Remove control voltages-V1
- 3) Remove VDD input

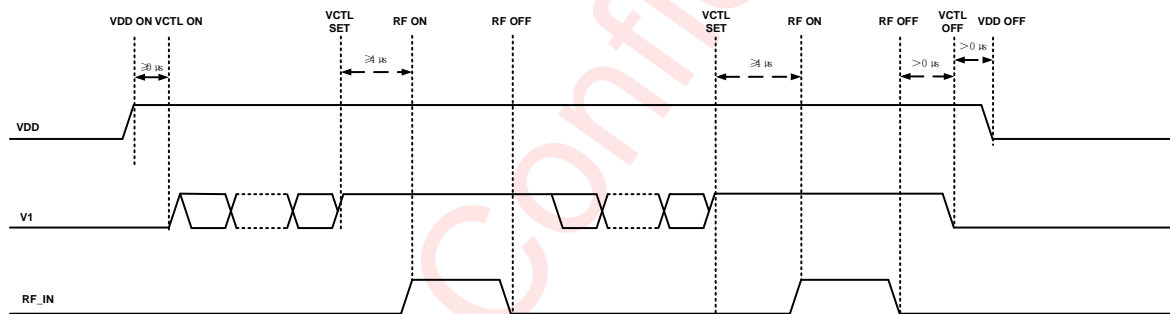
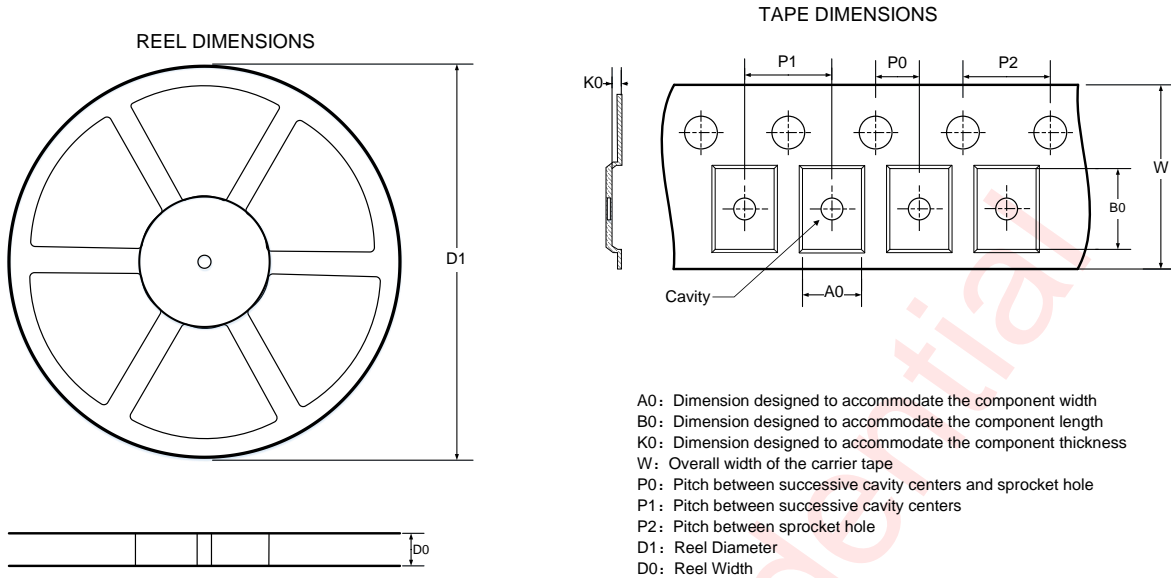


Figure 4 Power on/Change switch/Power off sequence

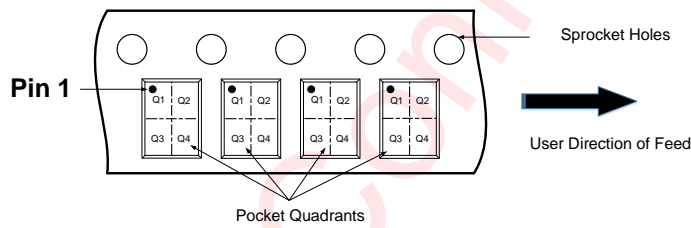
AW13612PFDR Control Logic

State	Active Path	V1
0	ANT to RF1	0
1	ANT to RF2	1

Tape And Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	0.82	1.22	0.46	2	2	4	8	Q1

All dimensions are nominal

Figure 5 Tape and Reel

Package Description

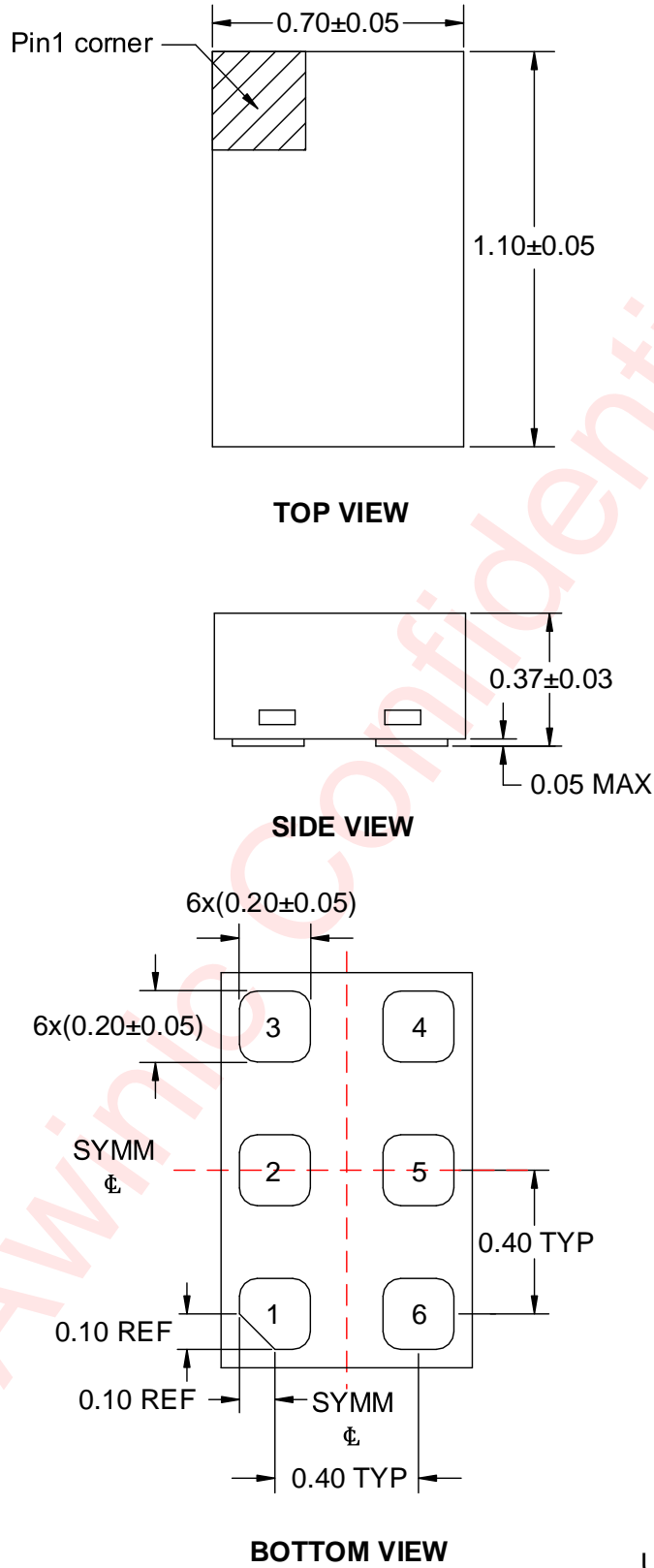
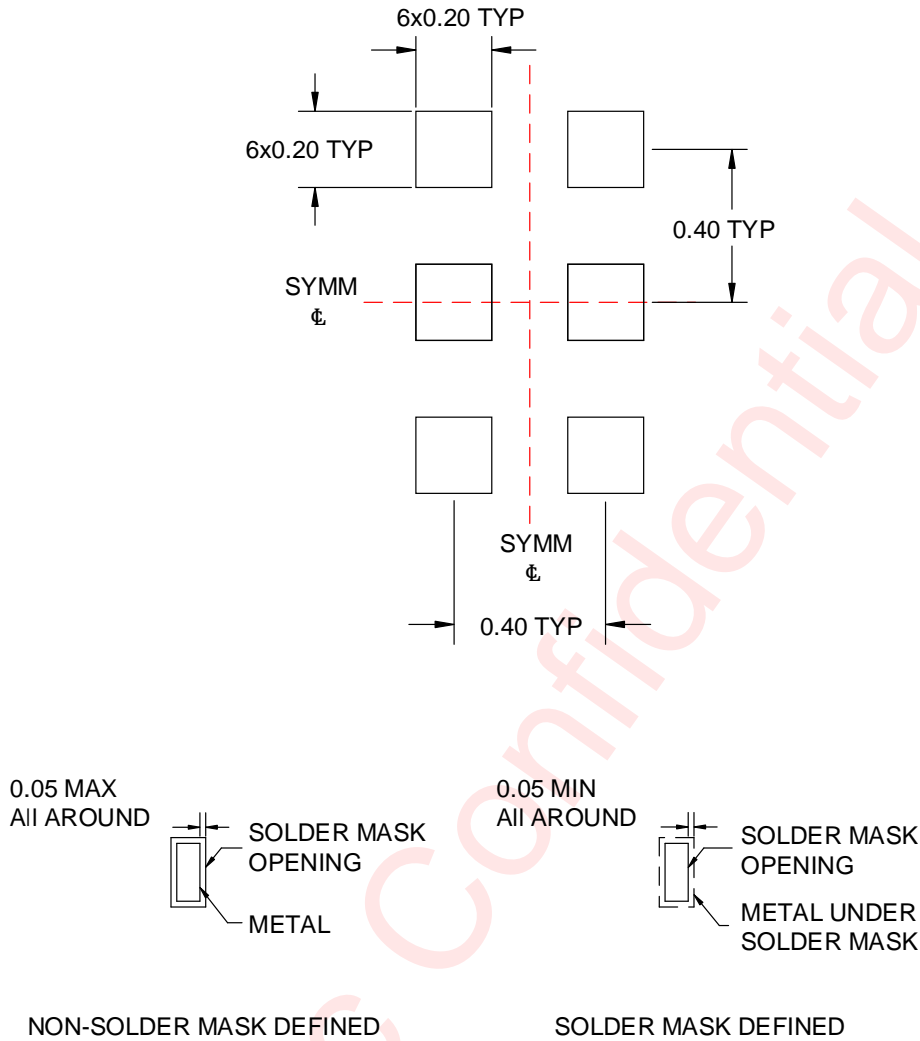


Figure 6 Package Outline

Land Pattern Data



Unit: mm

Figure 7 Land Pattern Data

Revision History

Version	Date	Change Record
V1.0	Apr. 2025	Officially Released

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