Non-Crack-Noise, Ultra-Low-THD+N, Ultra-Low-EMI, Mono, Filter-Free, Class-D Audio Amplifier

Features

- **NCN Function Protects the Speaker, Three Mode Selectable: NCN1, NCN2, NCNOFF**
- **Ultra low THD+N:0.007%**
- **Unique RNS**
- **High SNR:95dB**
- **EEE Function, Greatly reduces EMI over the full bandwidth**
- **Excellent Pop-Click Suppression**
- **Pin compatible with AW8055(B)**
- Filter-Free Class-D Architecture
- Gain of 12V/V(21.5dB)
- Low noise: 53μV@12V/V
- Up to 87% Efficiency
- High PSRR (75dB at 217Hz)
- Low Quiescent Current (3.5mA)
- Low Shutdown Current (<0.1μA)
- Power Supply Range: 2.5V~5.5V
- Over-Current Protection
- Over-Temperature Protection
- MSOP-8L Package

Applications

- Cellular Phones
- MP3/PMP
- GPS
- Digital Photo Frame
- HAC (Hearing Aid Compatibility)

General Description

The AW8056B is a non-crack-noise (NCN), ultra-low-EMI, filter-free, unique RNS technology, second generation Class-D audio amplifier. Ultra low THD+N, Unique NCN function, which adjusts the system gain automatically while detecting the "Crack" distortion of output signal, protects the speaker from damage at high power levels and invites the user to bask in immense musical enjoyment.

AW8056B NCN output power can be set to 0.72w or 0.85w for different speakers, this feature is embedded in order to protect speakers from damage caused by an excessive sound level.

The AW8056B features a unique RNS technology, which effectively reduces RF energy, attenuate the RF TDD-noise, an acceptable audible level to the customer.

The AW8056B features the EEE (Enhanced Emission Elimination) function which greatly reduces EMI over the full bandwidth. The AW8056B achieves better than 20dB margin under FCC limits with 24 inch of cable.

The filter-free PWM architecture and internal gain setting reduces external components count, board area consumption, system cost and simplifies the design. The over-current, over-temperature is prepared inside of the device.

The AW8056B is available in a MSOP-8L Package. The AW8056B is specified over the industrial temperature range of -40℃ to +85℃.

Typical Application

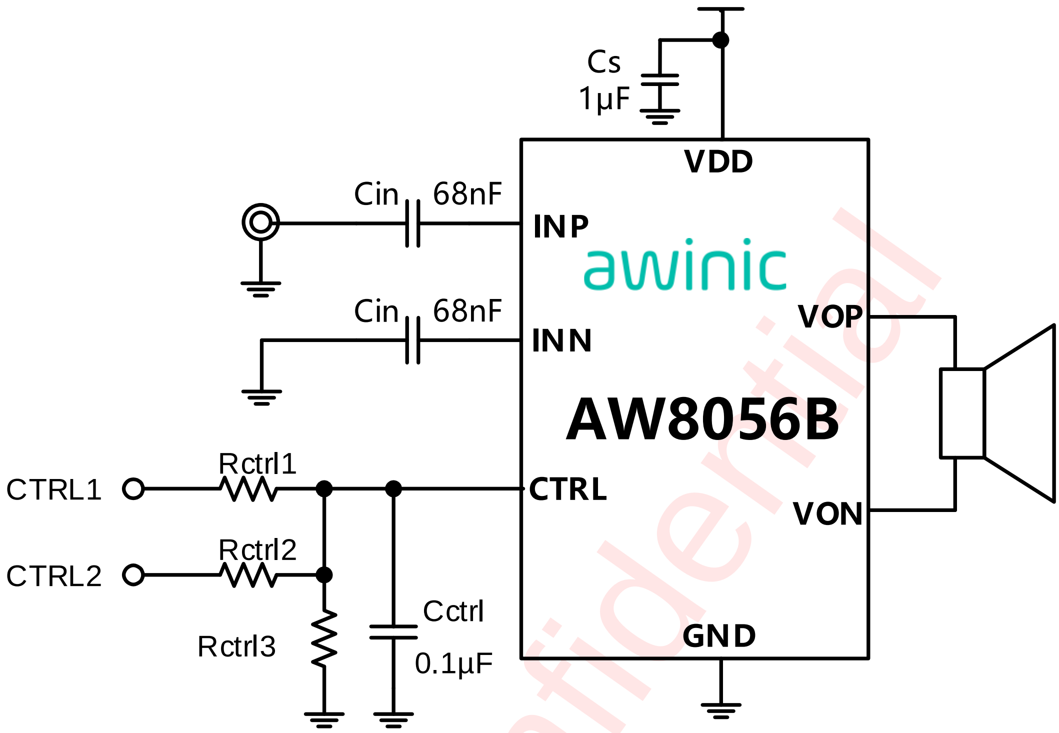


Figure 1. **AW8056B Application Schematic With Single-Ended Input**

Pin Configuration and Top Mark

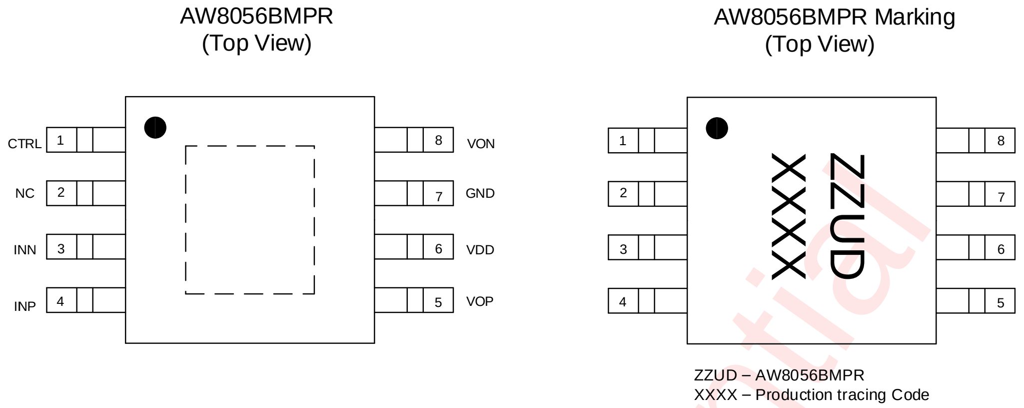


Figure 2. Pin Configuration and Top Mark of AW8056B

Pin Definition

No.	Symbol	Description
1	CTRL	Shutdown and NCN control pin
2	NC	Not connect
3	INN	Negative audio input
4	INP	Positive audio input
5	VOP	Positive audio output
6	VDD	Power Supply
7	GND	Power ground
8	VON	Negative audio output

Typical Application

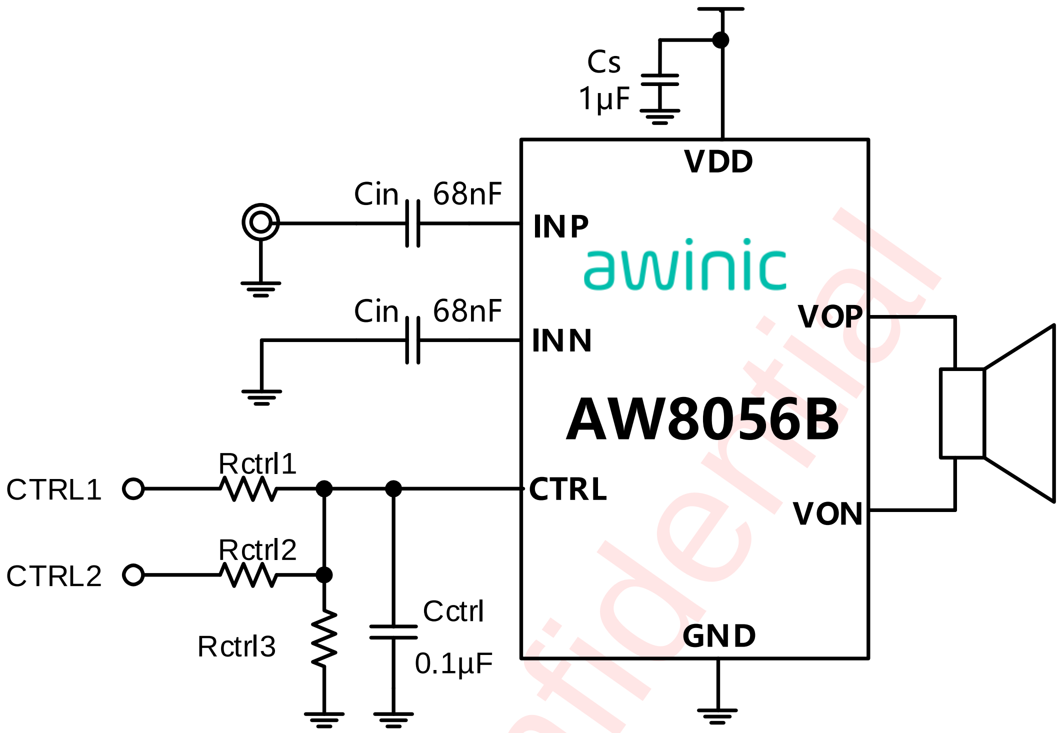


Figure 3. **AW8056B Application Schematic With Single-Ended Input**

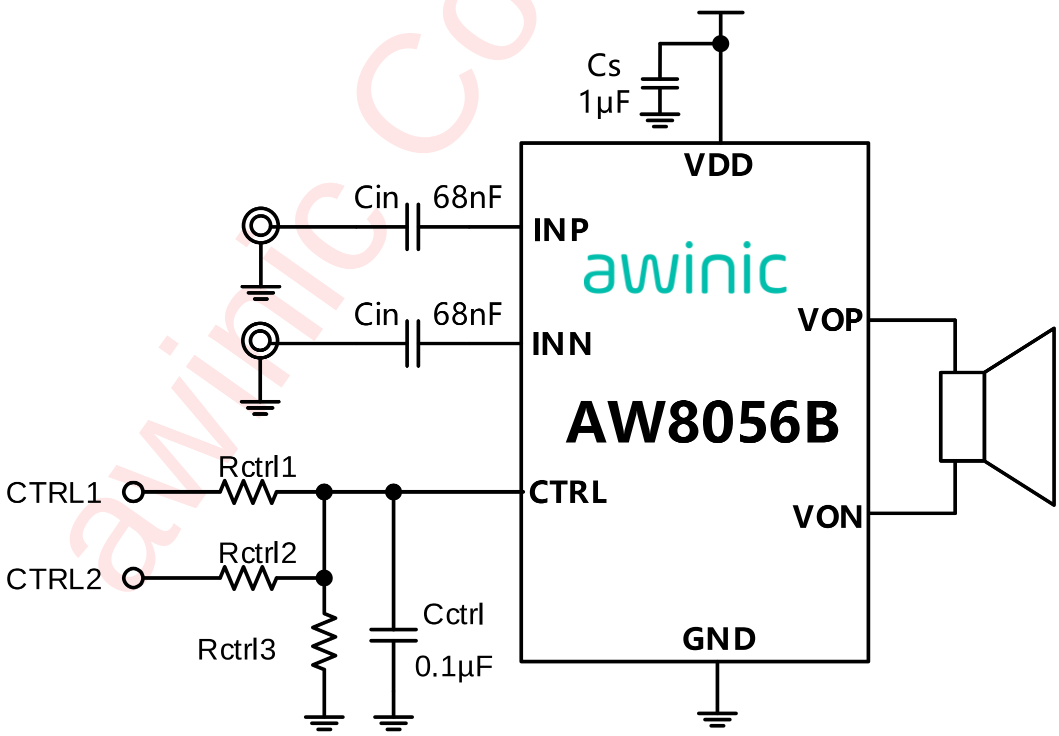


Figure 4. **AW8056B Application Schematic With Differential Input**

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW8056BMPR	-40℃～85℃	MSOP-8L	ZZUD	MSL3	RoHS+HF	3000 units/Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS	RANGE
Supply voltage range V_{DD}	-0.3V to 6V
Input voltage range	-0.3V to V_{DD}+0.3V
Junction-to-ambient thermal resistance θ_{JA}	90℃/W
Operating free-air temperature range	-40℃ to 85℃
Maximum operating junction temperature T_{JMAX}	125℃
Storage temperature T_{STG}	-65℃ to 150℃
Lead temperature (soldering 10 seconds)	260℃
ESD(Including CDM HBM MM)(NOTE 2)	
HBM (human body model)	±2kV
CDM (charged-device model)	±1.5kV
Latch-Up	
Test condition: JESD78E	+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017

Test method of the charged-device model: ESDA/JEDEC JS-002-2018

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	2.5		5.5	V
V_{NCN1}	NCN1 mode threshold voltage	1.20		VDD	V
V_{NCN2}	NCN2 mode threshold voltage	0.80		1.10	V
V_{NCNO}	NCNOFF mode threshold voltage	0.36		0.68	V
V_{SD}	Shutdown mode threshold voltage	0		0.14	V
T_A	Operating free-air temperature range	-40°	25	85	°C

Electrical Characteristics

Test Condition: V_{DD}=3.6V ,T_A=25℃, R_L=8Ω+33uH，Cin=33nF，f=1kHz (Unless otherwise specified)

Parameter		Conditions	Min	Typ	Max	Units
V_{DD}	Power supply voltage		2.5		5.5	V
V_{OS}	Output offset voltage	Input AC grounded，V_{DD}=2.5V to 5.5V	-25	0	25	mV
I_q	Quiescent current	V_{DD}=3.6V，Input AC grounded, no load		3.5		mA
I_{SD}	Shutdown current	V_{DD}=3.6V，CTRL =0V		0.1	1	μA
f_{SW}	Modulation Frequency	V_{DD}=2.5V to 5.5V	600	800	1000	kHz
T_{SD}	Thermal Protect level			160		℃
T_{SDR}	Thermal Hysteresis			120		℃
PSRR	Power supply rejection ratio	V_{DD}=4.2V，Vp-p_sin=200mV, 217Hz		75		dB
		V_{DD}=4.2V，Vp-p_sin=200mV, 1kHz		75		dB
CMRR	Common mode rejection ratio			70		dB
A_V	Gain			21.5		dB
Operating Characteristics						
P_O	Output power	THD+N=10%， R_L=4Ω+33uH，V_{DD}=5V		2.60		W
		THD+N=1%，R_L=4Ω+33uH，V_{DD}=5V		2.11		W
		THD+N=10%， R_L=8Ω+33uH，V_{DD}=5V		1.58		W
		THD+N=1%， R_L=8Ω+33uH，V_{DD}=5V		1.28		W
		THD+N=10%， R_L=4Ω+33uH，V_{DD}=4.2V		1.79		W
		THD+N=1%， R_L=4Ω+33uH，V_{DD}=4.2V		1.45		W
		THD+N=10%， R_L=8Ω+33uH，V_{DD}=4.2V		1.10		W
		THD+N=1%， R_L=8Ω+33uH，V_{DD}=4.2V		0.89		W
		THD+N=10%， R_L=4Ω+33uH，V_{DD}=3.6V		1.28		W
		THD+N=1%， R_L=4Ω+33uH，V_{DD}=3.6V		1.04		W
		THD+N=10%， R_L=8Ω+33uH，V_{DD}=3.6V		0.79		W
		THD+N=1%， R_L=8Ω+33uH，V_{DD}=3.6V		0.65		W
η	Efficiency	V_{DD}=3.6V，Po=1W，R_L=8Ω+33uH		87		%
THD+N	Total harmonic distortion plus noise	V_{DD}=5V，Po=0.5W，R_L=8Ω+33uH, f=1kHz		0.007		%
		V_{DD}=5V，Po=1W，R_L=4Ω+33uH, f=1kHz		0.008		%
Vn	Output noise	f=20Hz-20kHz,input AC grounded		53		uV
SNR	Signal-to-noise ratio	V_{DD} = 5 V, P_O = 1 W, R_L = 8Ω+33uH		95		dB
t_{ST}	Start-up time			40		ms
t_{WK}	Wake-up mode setting time		40			ms
t_{SD}	Shutdown setting time		80			ms
t_{MOD}	Each mode setting time		0.1			ms
NCN						
P_O NCN	NCN1 output power	f=1kHz，R_L=8Ω+33uH，V_{DD}=4.2V		0.85		W
	NCN2 output power	f=1kHz，R_L=8Ω+33uH，V_{DD}=4.2V		0.72		W

Parameter		Conditions	Min	Typ	Max	Units
T_{AT}	Attack time(-11dB)	V_{DD}=4.2V		45		ms
T_{RL}	Release time(11dB)	V_{DD}=4.2V		1		s
A_{MAX}	Max attenuation	V_{DD}=4.2V		-11		dB
V_{NCN1}	NCN1 mode threshold voltage		1.20		V_{DD}	V
V_{NCN2}	NCN2 mode threshold voltage		0.80		1.10	V
V_{NCNO}	NCNOFF mode threshold voltage		0.36		0.68	V
V_{SD}	Shutdown mode threshold voltage		0		0.14	V

MEASUREMENT SETUP

AW8056B features switching digital output, as shown in Figure 5. Need to connect a low pass filter to VOP/VON output respectively to filter out switch modulation frequency, then measure the differential output of filter to obtain analog output signal.

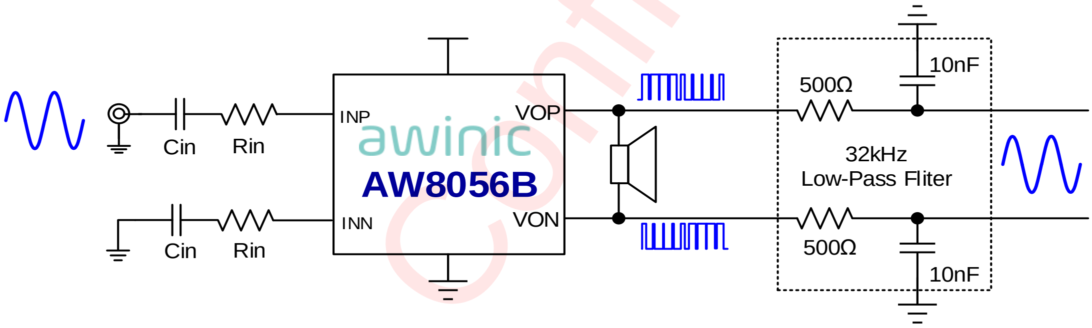


Figure 5. AW8056B test setup

Low pass filter uses resistance and capacitor values listed in Table 1.

Table 1 AW8056B recommended values for low pass filter

R_{filter}	C_{filter}	Low-pass cutoff frequency
500Ω	10nF	32kHz
1kΩ	4.7nF	34kHz

Output Power Calculation

According to the above test methods, the differential analog output signal is obtained at the output of the low pass filter. The valid values Vo_rms of the differential signal as shown below:

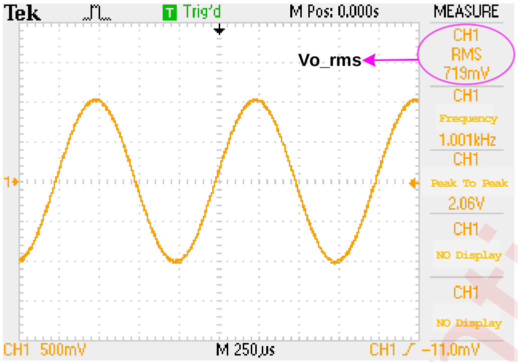
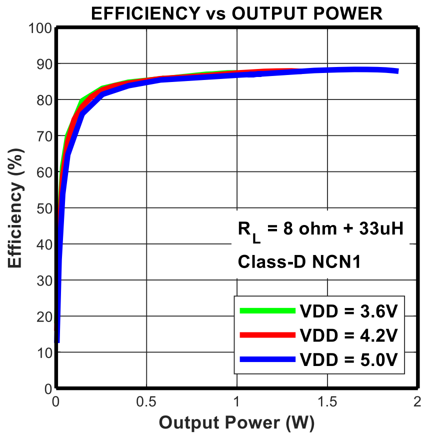


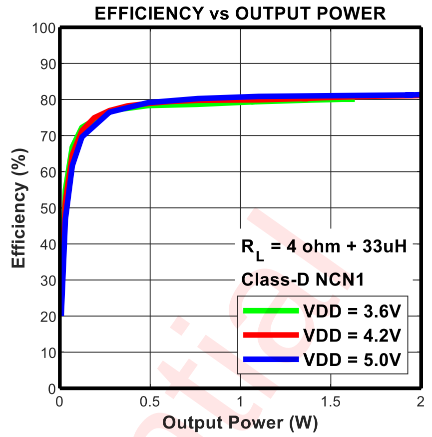
Figure 6. Valid value of AW8056B output signal

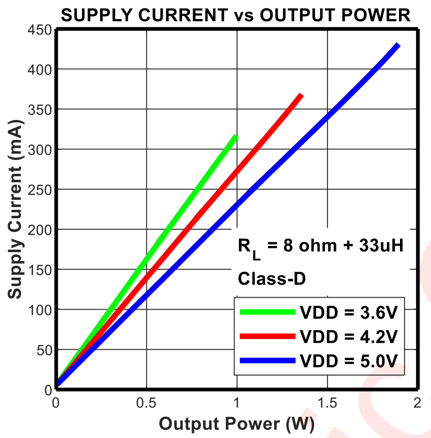
The power calculation of Speaker is as follows:

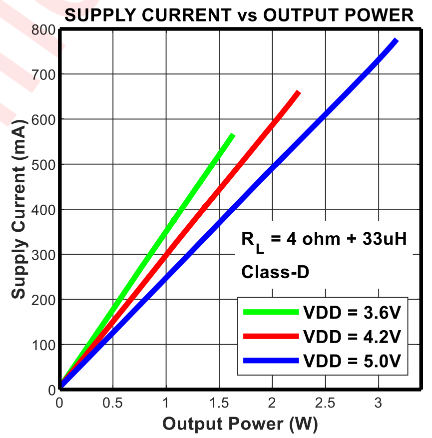
$$P_L = \frac{(Vo\_rms)^2}{R_L} \quad (R_L\text{: load impedance of the speaker})$$

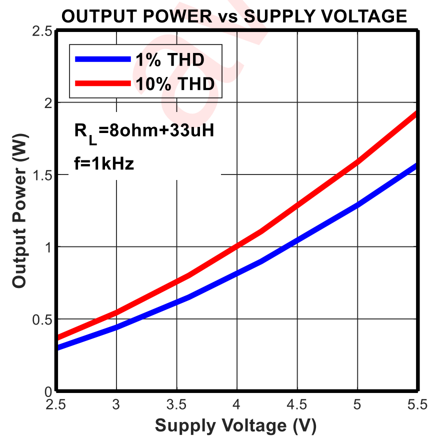
Typical Operating Characteristic

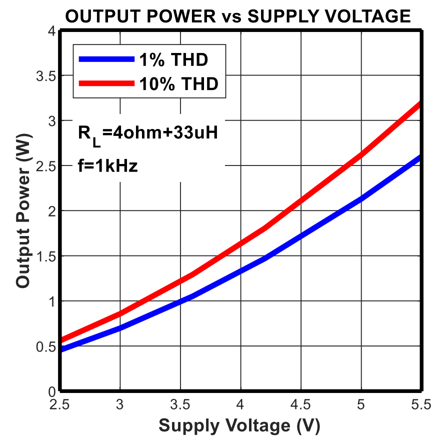


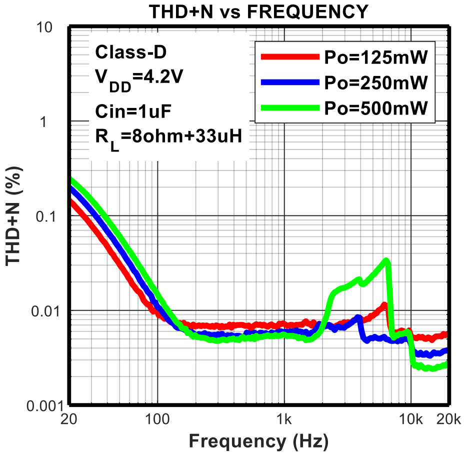


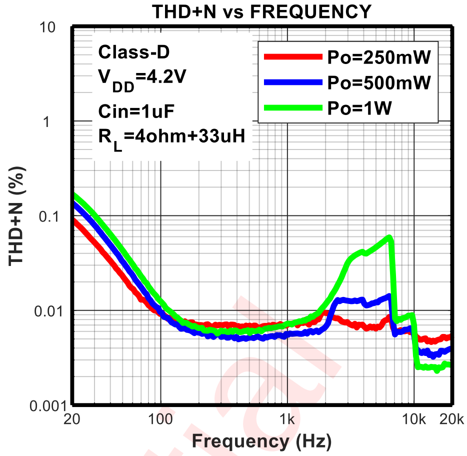


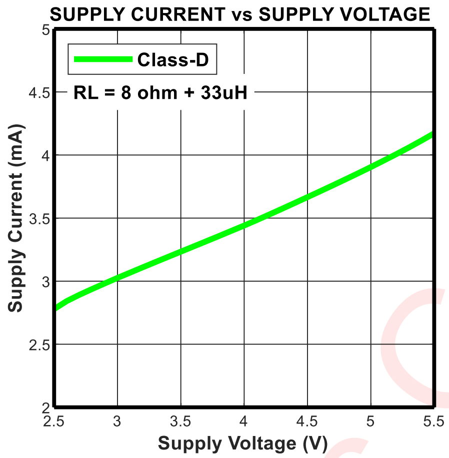


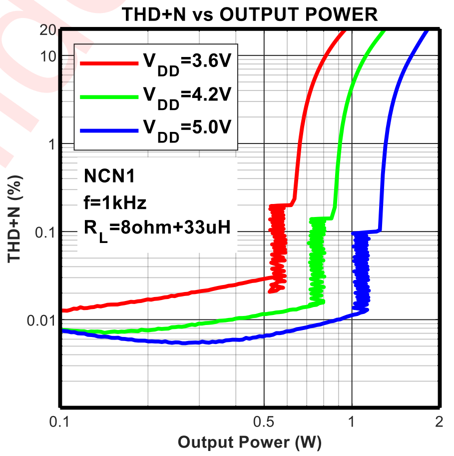


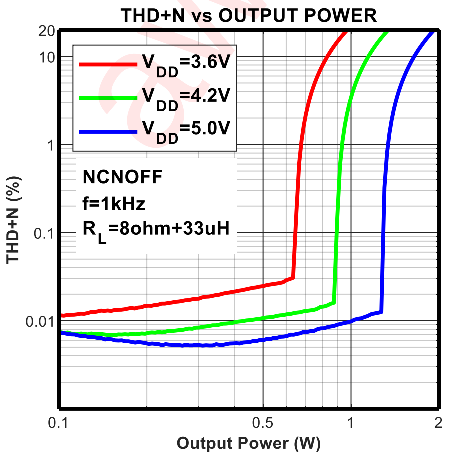


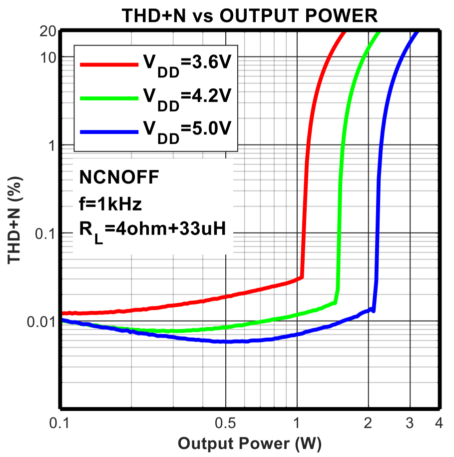

THD+N vs FREQUENCY
Class-D
V_{DD}=4.2V
Cin=1uF
R_L=8ohm+33uH
Po=125mW
Po=250mW
Po=500mW
THD+N (%)
Frequency (Hz)

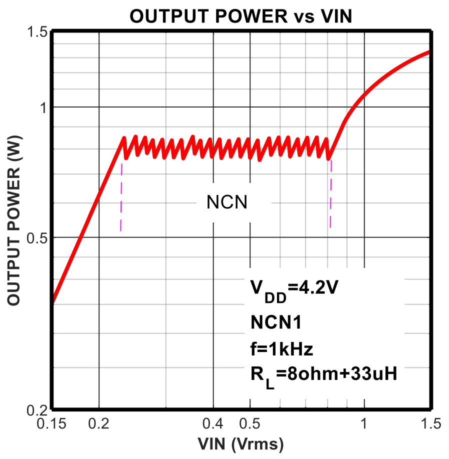

THD+N vs FREQUENCY
Class-D
V_{DD}=4.2V
Cin=1uF
R_L=4ohm+33uH
Po=250mW
Po=500mW
Po=1W
THD+N (%)
Frequency (Hz)

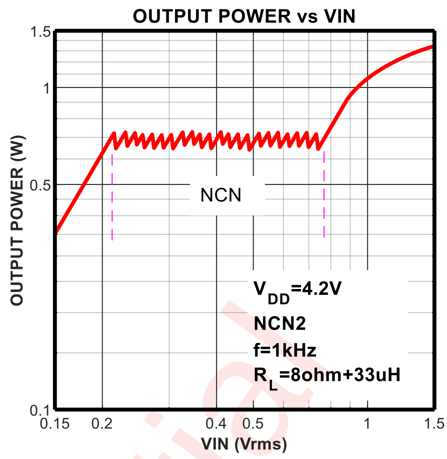

SUPPLY CURRENT vs SUPPLY VOLTAGE
Class-D
RL = 8 ohm + 33uH
Supply Current (mA)
Supply Voltage (V)

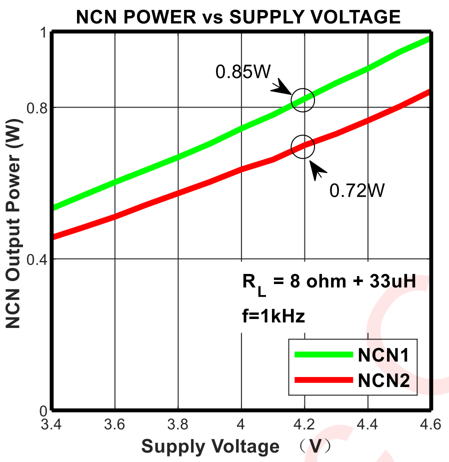

THD+N vs OUTPUT POWER
V_{DD}=3.6V
V_{DD}=4.2V
V_{DD}=5.0V
NCN1
f=1kHz
R_L=8ohm+33uH
THD+N (%)
Output Power (W)

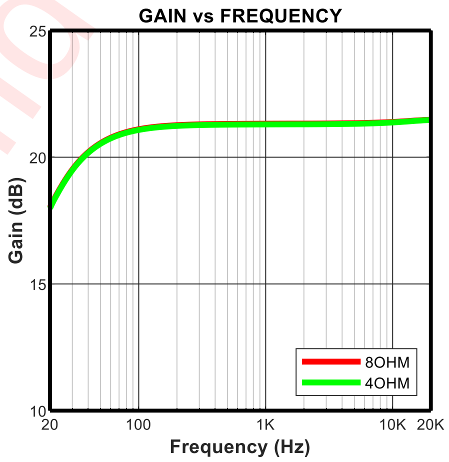

THD+N vs OUTPUT POWER
V_{DD}=3.6V
V_{DD}=4.2V
V_{DD}=5.0V
NCNOFF
f=1kHz
R_L=8ohm+33uH
THD+N (%)
Output Power (W)

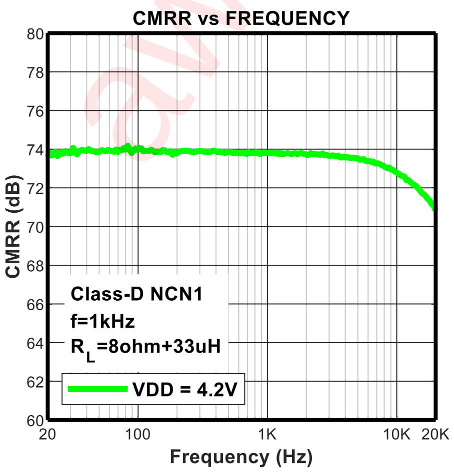

THD+N vs OUTPUT POWER
V_{DD}=3.6V
V_{DD}=4.2V
V_{DD}=5.0V
NCNOFF
f=1kHz
R_L=4ohm+33uH
THD+N (%)
Output Power (W)

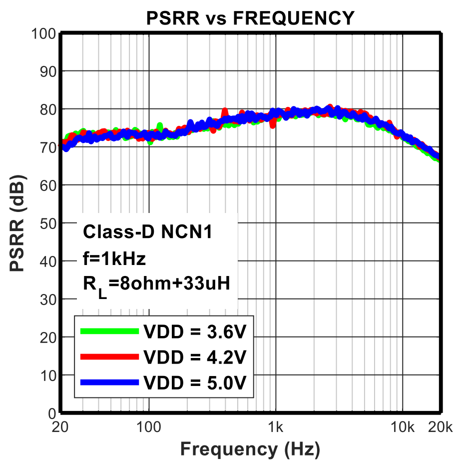

OUTPUT POWER vs VIN
OUTPUT POWER (W)
VIN (Vrms)
NCN
VDD=4.2V
NCN1
f=1kHz
RL=8ohm+33uH

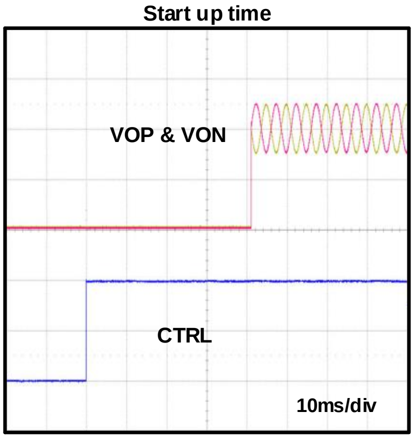

OUTPUT POWER vs VIN
OUTPUT POWER (W)
VIN (Vrms)
NCN
VDD=4.2V
NCN2
f=1kHz
RL=8ohm+33uH

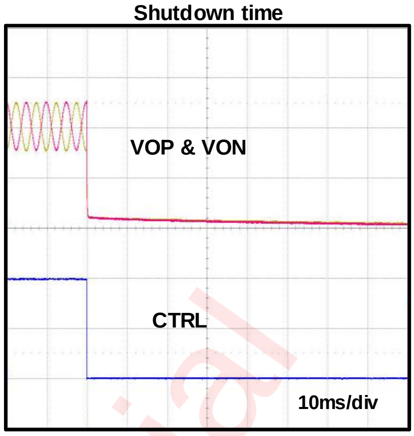

NCN POWER vs SUPPLY VOLTAGE
NCN Output Power (W)
Supply Voltage （V）
0.85W
0.72W
RL = 8 ohm + 33uH
f=1kHz
NCN1
NCN2

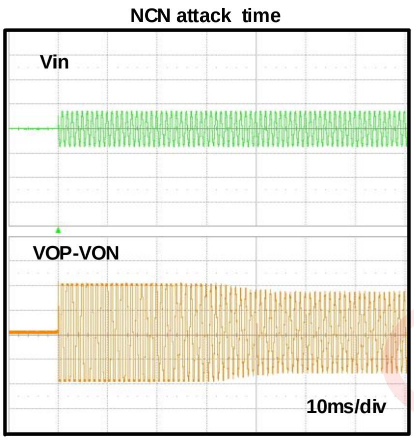

GAIN vs FREQUENCY
Gain (dB)
Frequency (Hz)
8OHM
4OHM

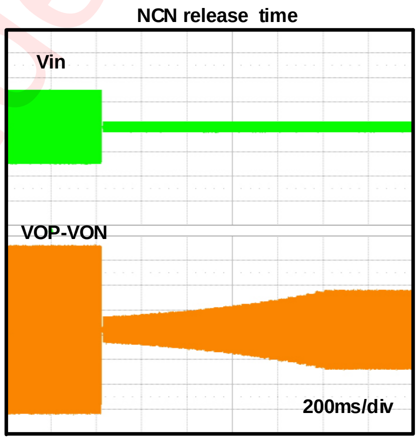

CMRR vs FREQUENCY
CMRR (dB)
Frequency (Hz)
Class-D NCN1
f=1kHz
RL=8ohm+33uH
VDD = 4.2V


PSRR vs FREQUENCY
PSRR (dB)
Frequency (Hz)
Class-D NCN1
f=1kHz
RL=8ohm+33uH
VDD = 3.6V
VDD = 4.2V
VDD = 5.0V


Start up time
VOP & VON
CTRL
10ms/div


Shutdown time
VOP & VON
CTRL
10ms/div


NCN attack time
Vin
VOP-VON
10ms/div


NCN release time
Vin
VOP-VON
200ms/div

Block Diagram

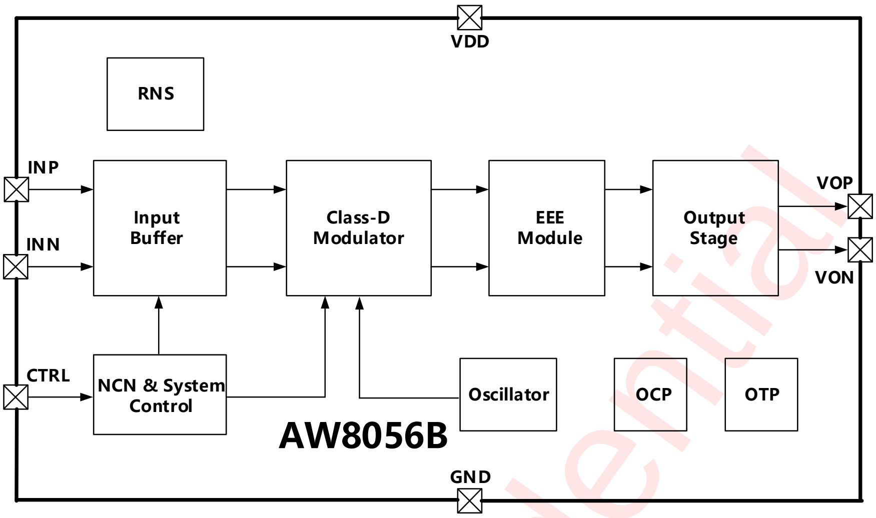


Figure 7. Functional Block Diagram of AW8056B

Operation

The AW8056B is a non-crack-noise (NCN), ultra-low-EMI, filter-free, second generation Class-D audio amplifier. Ultra low THD+N, Unique NCN function, which adjusts the system gain automatically while detecting the "Crack" distortion of output signal, protects the speaker from damage at high power levels and brings the most comfortable listening experience to the customers.

AW8056B NCN output power can be set to 0.72W or 0.85W for different speaker, this feature is embedded in order to protect speakers from damage caused by an excessive sound level.

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The filter-free PWM architecture and internal gain setting reduces external components count, board area consumption, system cost and simplifies the design. The over-current, over-temperature is prepared inside of the device.

The AW8056B is available in a MSOP-8L Package. The AW8056B is specified over the industrial temperature range of -40℃ to +85℃.

RNS (RF TDD Noise Suppression)

TDD Noise Causes

GSM cell phones use TDMA (Time Division Multiple Access) slot sharing technology. The time is divided into periodic frames in TDMA, and each frame is subdivided into a plurality of time slots. In order to transmit signals to the base station, the signals sent from the base stations to the plurality of mobile terminals are arranged in a predetermined time slot in the transmission. In this case, each TDMA frame contains 8 time slots, the entire frame is about 4.615ms long, and each slot time is 0.577ms.

With GSM handset, the RF power amplifier will transmit once every 4.615ms (217Hz), and the signal will produce intermittent Burst current and strong electromagnetic radiation. Intermittent Burst current will form a power fluctuation of 217 Hz; High frequency (900MHz and 1800MHz) RF signals form a 217Hz RF envelope signal. 217Hz power fluctuations will be conducted through the conduction to the audio signal path, 217Hz RF envelope signal will be coupled through the radiation into the audio signal path, if the protection is not good, it will produce an audible TDD Noise, which includes the 217Hz noise And a harmonic noise signal of 217 Hz.

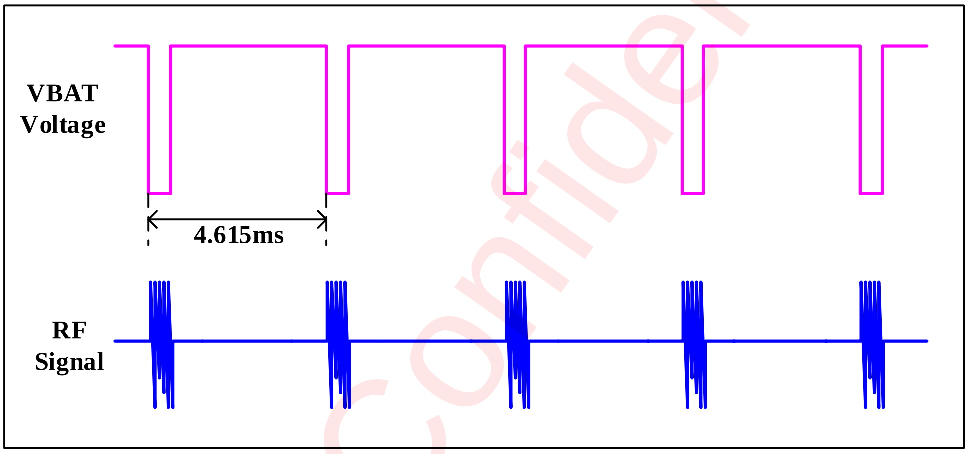


Figure 8. Schematic Diagram of Power Supply Voltage and RF Signal during GSM RF Operation

RNS fully inhibit the conduction and radiation interference by the AWINIC unique circuit architecture. Effectively improve the ability to suppress TDD Noise.

Conduction noise suppression

When the RF power amplifier is operating, it will draw the current from the battery by 217Hz frequency, Power supply will be introduced to 217Hz power ripple since the battery has a certain internal resistance, it will be coupled to the speaker through the audio power amplifier. The ability to suppress power fluctuations depends on the PSRR of the audio power amplifier.

$$PSRR = 20\log\left(\frac{vdd_{ac}}{vout_{ac}}\right)$$

Due to the input and output of the fully differential amplifier is perfectly symmetrical, theoretically, the effect of the power supply fluctuation on the two outputs is exactly the same, and the differential output is completely unaffected by the power supply fluctuation. In practice, due to process bias and other factors, the amplifier will have a certain mismatch, PSRR is generally better than 60dB, it shows the output relative to the power fluctuations can be reduced by 1000 times, such as 500mVp power fluctuations, the differential output of 0.5 mV, which basically can meet the application requirements.

But in practical applications, the power amplifier may encounter conduction of TDD Noise problem even if its PSRR is 60dB or 80dB, why is this? Because we also need to consider the impact of peripheral power mismatches of audio power amplifiers

For conventional audio power amplifiers, when the input resistor Rin and the input capacitor Cin mismatch, will greatly affect the audio power amplifier PSRR indicators, in the case of 24dB gain, PSRR will be weakened to 46dB or so if the input resistance and Capacitor with 1% mismatch. PSRR will be weakened to 28dB or so if the input resistance and input capacitance mismatch with 10% mismatch, when the power fluctuations, it is easy to produce audible TDD Noise.

In order to enhance the audio power amplifier PSRR in the input resistance and input capacitance mismatch case, AW8056B features a unique conduction noise suppression circuit, making the power amplifier to maintain a high PSRR value even in the input resistance, the input capacitance deviation of 10% or more, this greatly inhibits the generation of conducted noise.

Radiation noise suppression

Input traces, output traces, horn loops, and even power and ground loops are likely to be subject to RF radiation interference in the audio signal module, longer input traces and output traces similar to the antenna, especially vulnerable RF radiation effects.

The reasonable PCB layout can reduce the influence of RF radiation in the design, such as shorten the line length of input and output as much as possible; audio devices should be shielded and far away from the RF antenna, maintain the integrity of the device to audio signal pathway; to increase the small bypass capacitor RF signals in the sensitive nodes. However, in practical applications, PCB layout is difficult to fully consider the influence of RF radiation on the audio signal path, and some RF energy will still be coupled to the audio signal path to form audible TDD Noise. Therefore, AW8056B features a unique RF radiation suppression circuit, a shielding layer inside the chip, effectively prevent high frequency energy into RF chip, to ensure that the drive single of the amplifier provided to the speaker will not be affected by the antenna RF radiation, thus avoiding the antenna RF Radiation caused by TDD Noise.

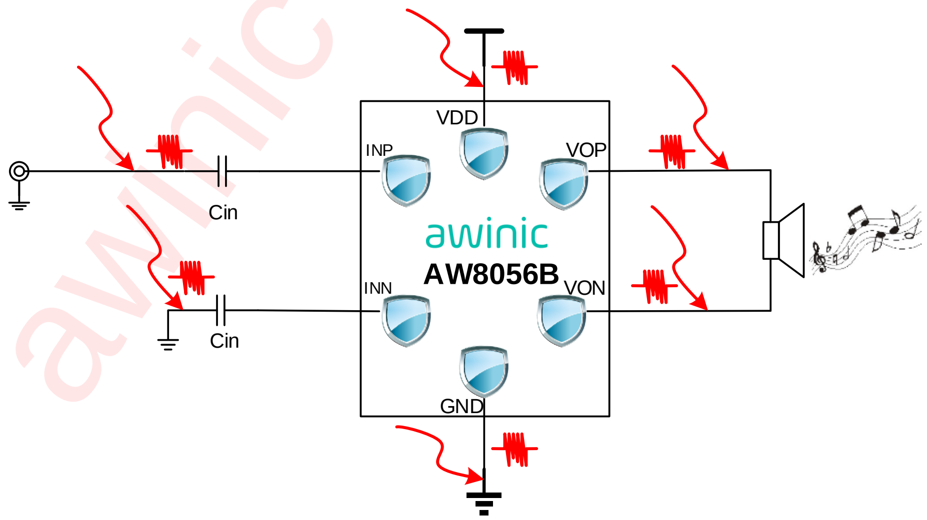


Figure 9. RF Energy Coupling Diagram

NCN

In audio application, output signal will be undesirable distortion caused by too large input and power supply voltage down with battery, and clipped output signal may cause permanent damage to the speaker. The AW8056B features unique non-crack-noise (NCN) Function, which adjusts system gain automatically to generate desired output by detecting the “Crack” distortion of output signal, protects the speaker from damage at high power levels and brings the most comfortable listening experience to the customers.

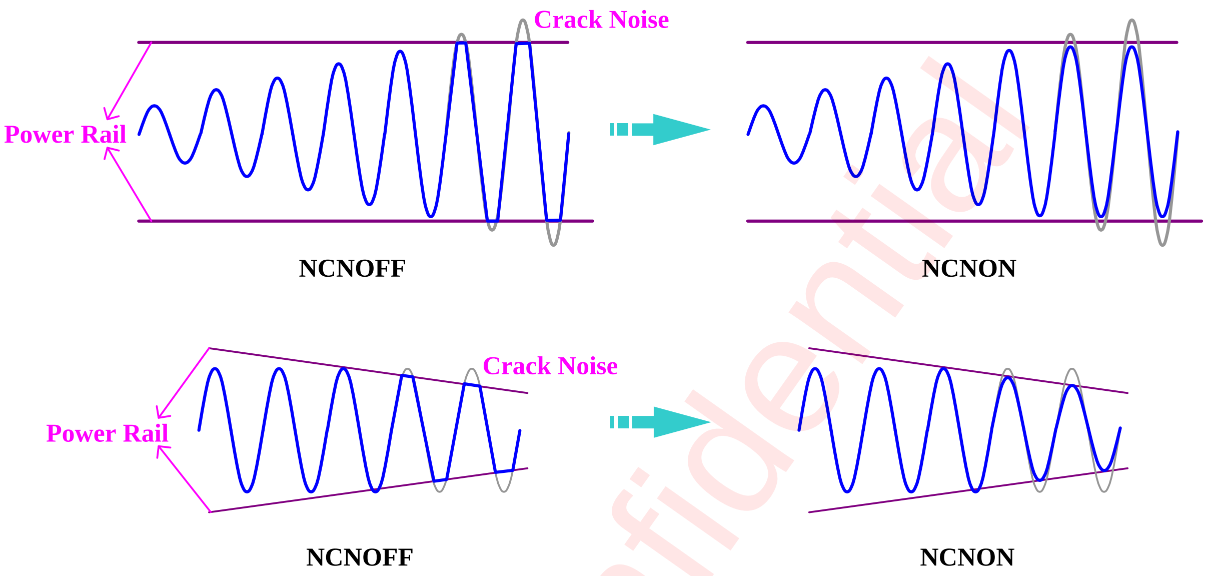


Figure 10. NCN Function Diagram

Attack time

Attack time is the time it takes for the gain to be reduced once the audio signal exceeds the NCN threshold. Fast attack times allow the NCN to react quickly and prevent transients such as symbol crashes from being distorted. However, fast attack times can lead to volume pumping, where the gain reduction and release becomes noticeable, as the NCN cycles quickly. Slower attack times cause the NCN to ignore the fast transients, and instead act upon longer, louder passages. Selecting an attack time that is too slow can lead to increased distortion in the case of the No Clip function. Attack time is set 35ms~55ms in AW8056B.

Release time

Release time is the time it takes for the gain to return to its normal level once the audio signal returns below the NCN threshold. A fast release time allows the NCN to react quickly to transients, preserving the original dynamics of the audio source. However, similar to a fast attack time, a fast release time contributes to volume pumping. A slow release time reduces the effect of volume pumping. Release time is set 0.8s~1.2s in AW8056B.

CTRL Pin Setting

By setting the voltage of CTRL pin to select each mode of AW8056B, as shown in Table 2. The connection of external resistors to CTRL pin is shown in figure11. CTRL1 and CTRL2 are setting by GPIO to H(V_{IO}) or L(GND). **The GPIO of two CTRL pins should have pull-down function.**

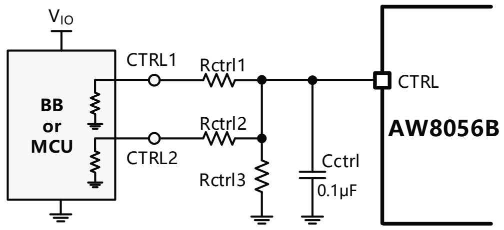


Figure 11. CTRL Pin Setting (1)

Table 2 Operating Modes

CTRL1	CTRL2	Mode
H	H	NCN1
H	L	NCN2
L	H	NCNOFF
L	L	SHUTDOWN

Set resistance constants according to high level (VIO:1.8V~5V) of GPIO, as shown in Table 3, it is recommended to use 1% tolerance resistors or better. Bypass capacitor C_{ctrl}（0.1μF）connects CTRL pin to GND filters any noise, and aids in voltage stability.

Table 3 CTRL External Resistors Setting

V_{IO}	1.8V	2.6V	2.8V	3.0V	3.3V	5V
Rctrl1	27KΩ	33KΩ	33KΩ	33KΩ	33KΩ	56KΩ
Rctrl2	56KΩ	68KΩ	68KΩ	68KΩ	68KΩ	120KΩ
Rctrl3	82KΩ	27KΩ	24KΩ	22KΩ	18KΩ	15KΩ

If the system only needs NCN1 mode and SHUTDOWN mode, a simplified external resistor and capacitor can be used. CTRL pin setting is shown in Figure 12 and Table 4. **The GPIO of CTRL pin should have pull-down function.** R_{ctrl} and C_{ctrl} should be set with time constant of 1ms or larger in order to eliminate noise.

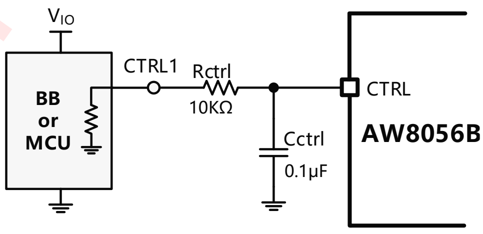


Figure 12. CTRL Pin Setting (2)

Table4 Operating Modes

CTRL1	Mode
H	NCN1
L	SHUTDOWN

Operating Modes Switching

The AW8056B enters shutdown mode when the CTRL pin is "L"(GND). In order to return from power-down or shutdown mode, it needs to be set NCN1 mode first (both CTRL1 and CTRL2 to "H"). After wake-up, the AW8056B enters each mode (NCN1, NCN2 and NCNOFF) by CTRL1 and CTRL2 setting, as shown in Table 2. Timing of operating modes switching is shown in Figure 13.

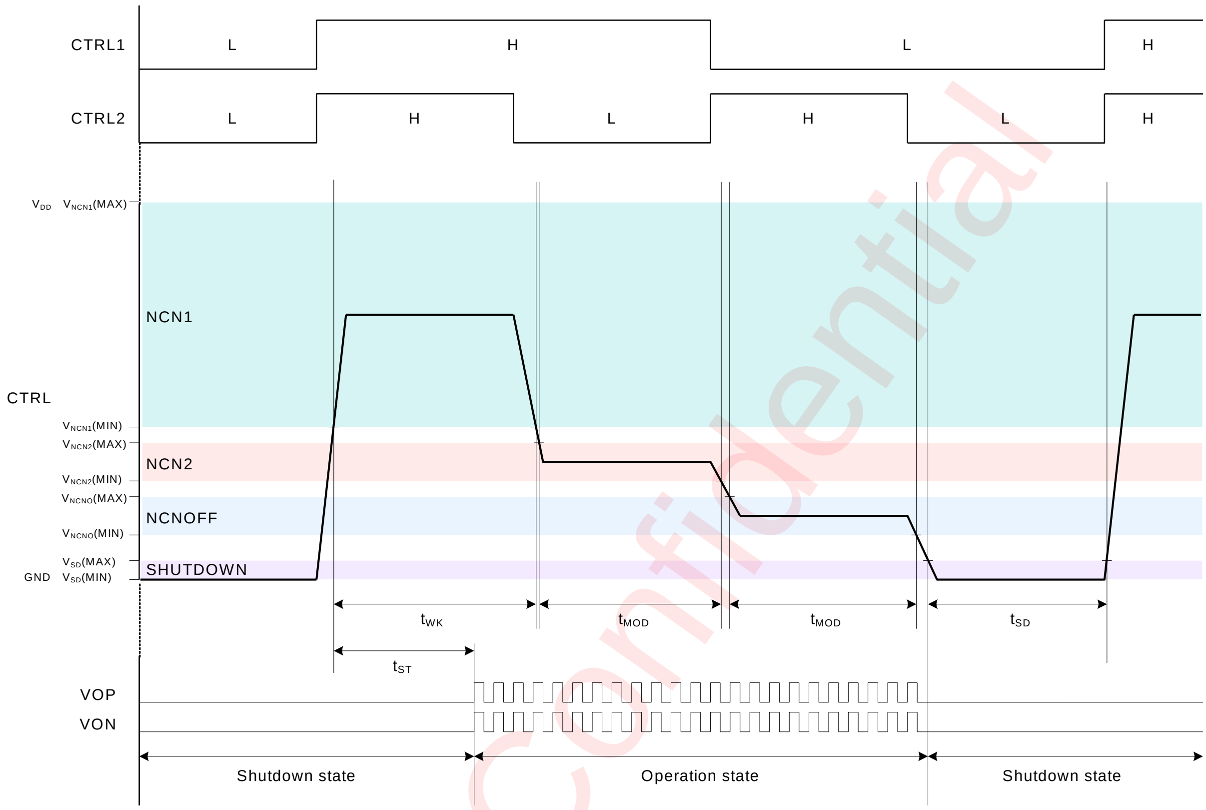


Figure 13. AW8056B Timing Diagram

Filter-Free Modulation Scheme

The AW8056B features a filter-free PWM architecture that reduces the LC filter of the traditional Class-D amplifier, increasing efficiency, reducing board area consumption and system cost.

Pin-Compatible with AW8055(B)

The AW8056B is pin compatible with AW8055(B) .

EEE

The AW8056B features a unique Enhanced Emission Elimination (EEE) technology, that controls fast transition on the output, greatly reduces EMI over the full bandwidth.

Pop-Click Suppression

The AW8056B features unique timing control circuit, that comprehensively suppresses pop-click noise, eliminates audible transients on shutdown, wakeup, and power-up/down.

Efficiency

Efficiency of a Class D amplifier is attributed to the switching operation of the output stage transistors. In a Class D amplifier, the output transistors act as current steering switches and consume negligible additional power. Any power loss associated with the Class D output stage is mostly due to the I2R loss of the MOSFET on-resistance and supply current. The AW8056B features efficiency of 87%.

Protection Function

When a short-circuit occurs between VOP/VON pin and VDD/GND or VOP and VON, the over-current circuit shutdown the device, preventing the device from being damaged. When the condition is removed, the AW8056B reactivate itself. When the junction temperature is high, the over-temperature circuit shutdown the device. The circuit switches back to normal operation when the temperature decreases to safe levels.

Applications Information

Supply Decoupling Capacitor（C_S）

The AW8056B is a high-performance audio amplifier that requires adequate power supply decoupling. Place a low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the AW8056B is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the 1μF ceramic capacitor, place a 10μF capacitor on the VDD supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

Input Capacitor

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. The input capacitors and internal input resistors (9KΩ) form a high-pass filter with the corner frequency, fc.

$$f_C = \frac{1}{2\pi RinCin} = 260\,Hz\ .$$

Setting the high-pass filter point high can block the 217Hz GSM noise coupled to inputs. Better matching of the input capacitors improves performance of the circuit and also help to suppress pop-click noise.

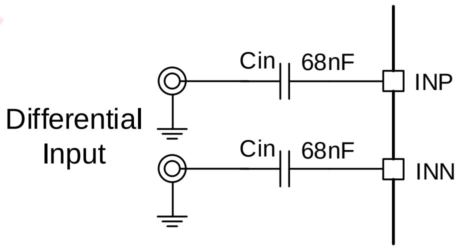


Figure 14. Differential Input

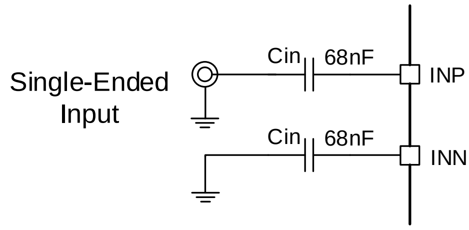


Figure 15. Single-Ended Input

Ferrite Chip Bead and Capacitor

The AW8056B passed FCC and CE radiated emissions with no ferrite chip beads and capacitors with speaker trace wires 24 inch.Use ferrite chip beads and capacitors if device near the EMI sensitive circuits and/or there are long leads from amplifier to speaker, placed as close as possible to the output pin.

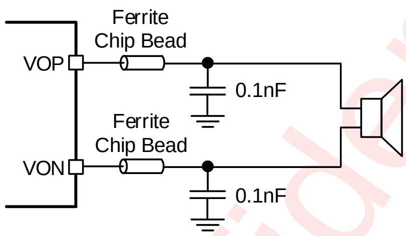


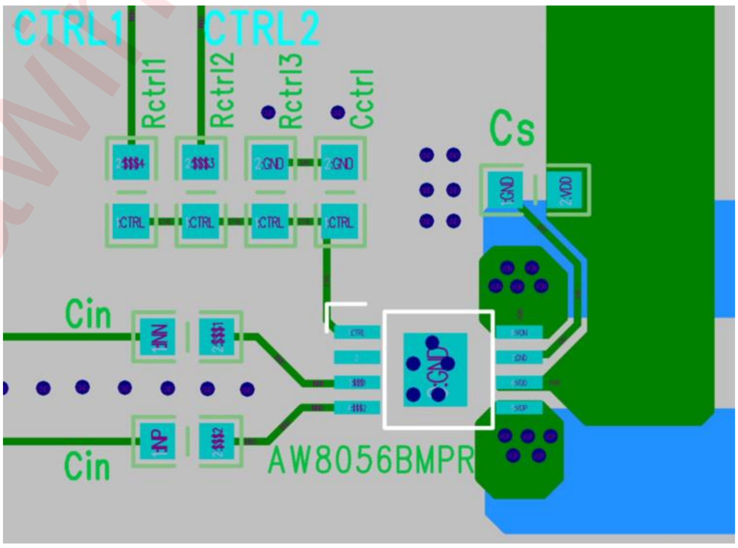
Figure 16. Ferrite Chip Bead and capacitor

PCB Layout Consideration

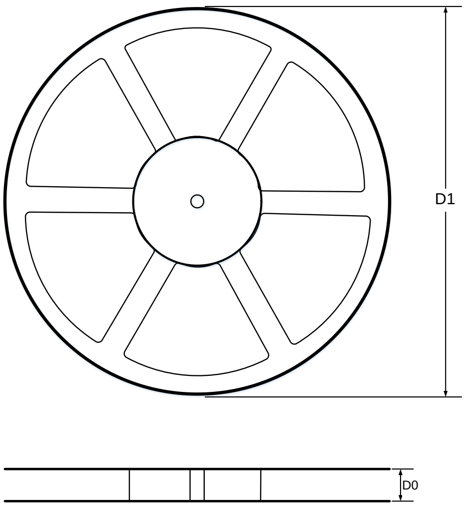
In order to obtain excellent performance of AW8056B, PCB layout must be carefully considered. The design consideration should follow the following principles:

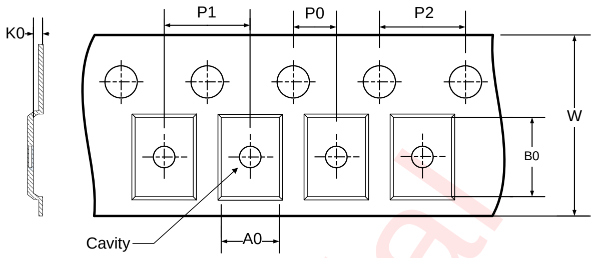
1. Try to provide a separate short and thick power line to AW8056B, the copper width is recommended to be larger than 1.2mm. The decoupling capacitors should be placed as close as possible to power supply pin.

2. The input capacitors should be close to AW8056B INN and INP input pin, the input line should be parallel to suppress noise coupling.

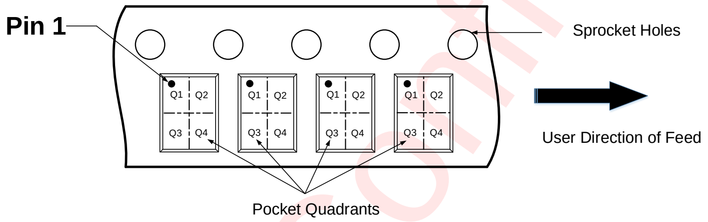


Tape And Reel Information





A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width



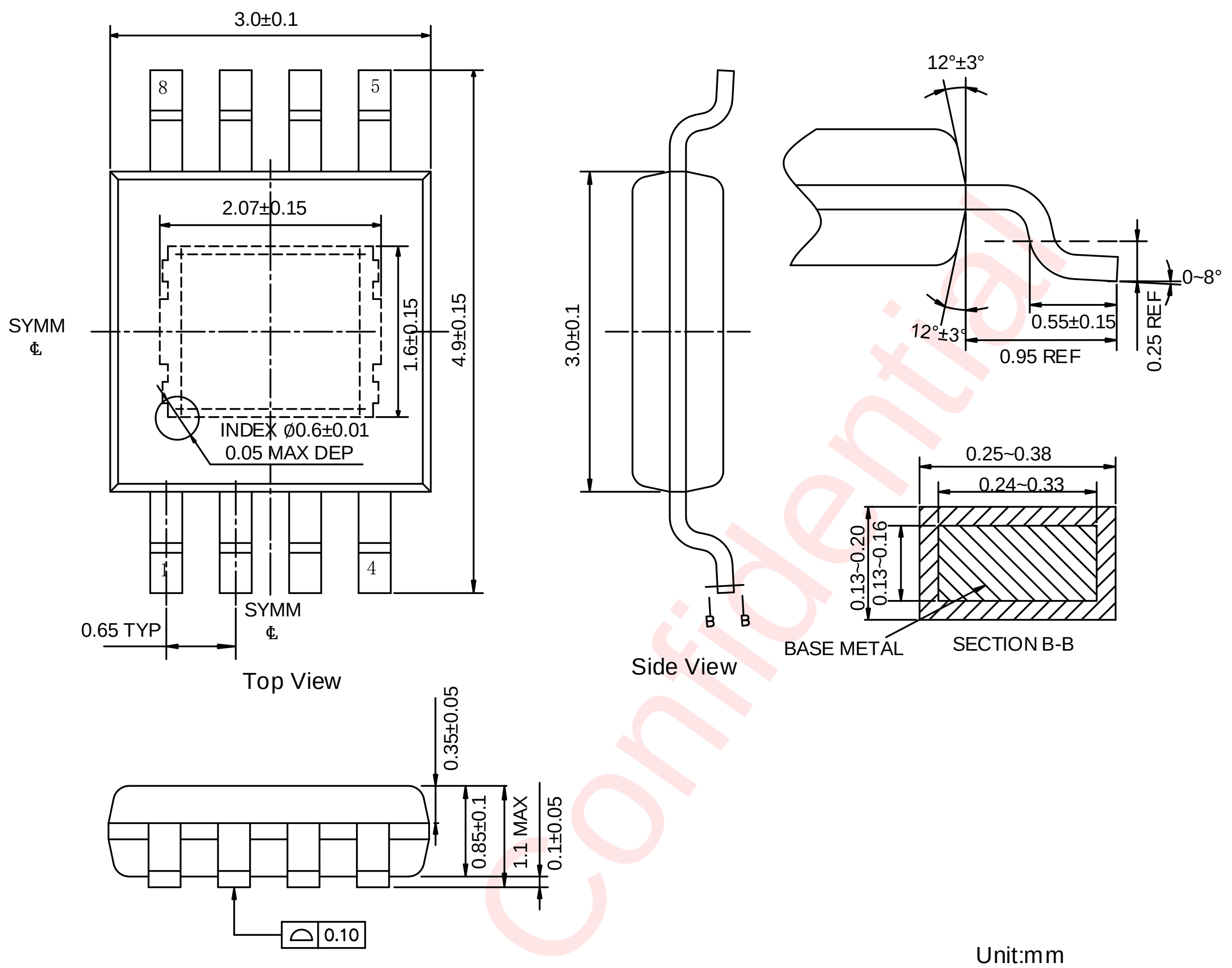
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	5.25	3.35	1.25	2	8	4	12	Q1

All dimensions are nominal

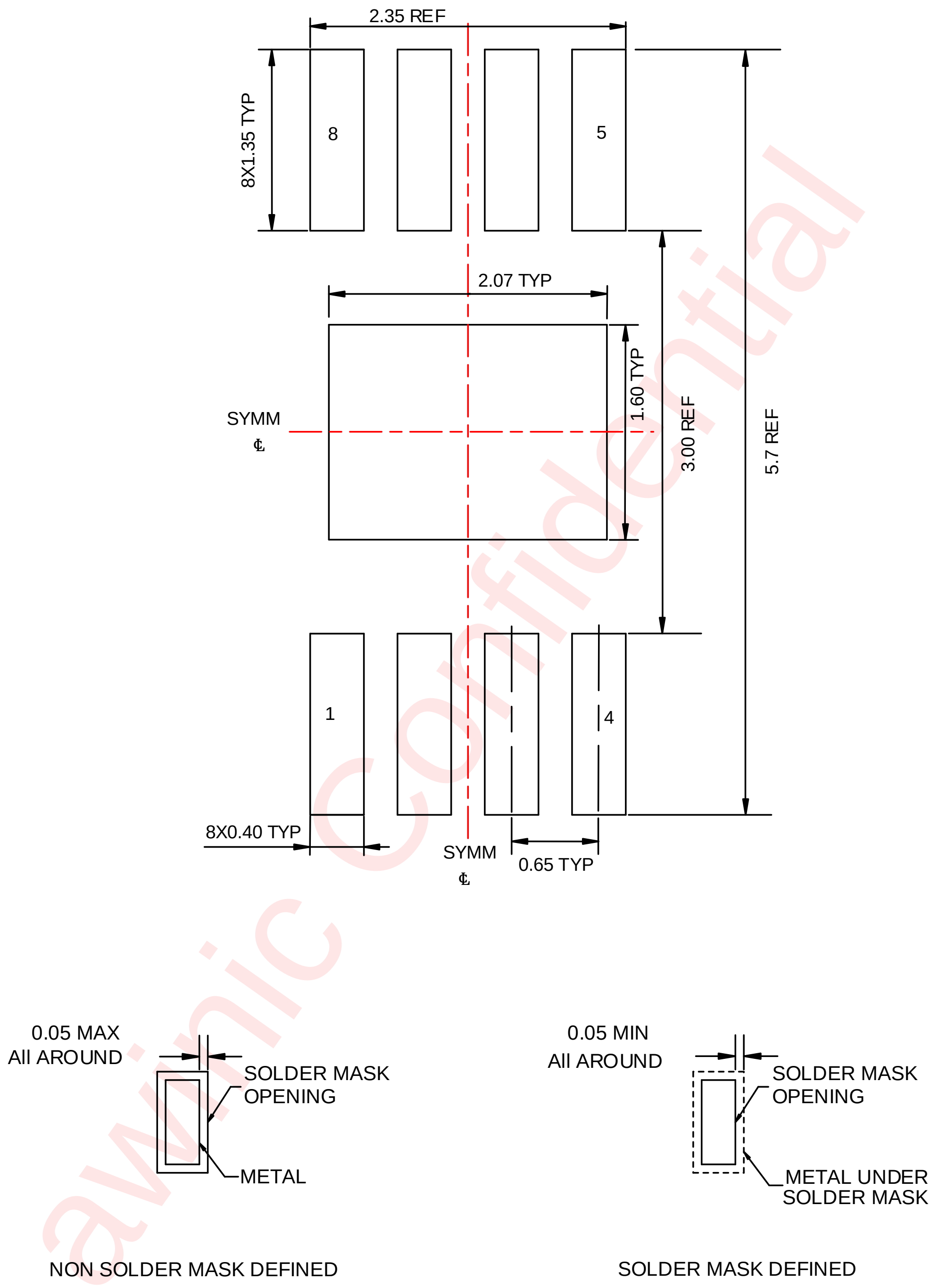
Package Description



Side View

Unit:mm

Land Pattern Data



UNIT: mm

Version Information

Version	Release date	Description
V1.0	2022-08-23	Initial release

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