1.5A Ultra-small Load Switch with Slew Rate Control

FEATURES

- Integrated P-channel MOSFET load switch
- Input voltage: 1.2V to 5.5V
- 1.5A maximum continuous switch current
- Switch on-resistance(typ.):
  Rdson=50mΩ at V_{IN}=5.5V
  Rdson=56mΩ at V_{IN}=4.2V
  Rdson=64mΩ at V_{IN}=3.3V
  Rdson=78mΩ at V_{IN}=2.5V
  Rdson=109mΩ at V_{IN}=1.8V
  Rdson=225mΩ at V_{IN}=1.2V
- Controlled slew rate to limit inrush current
- Internal EN Pull-Down Resistor
- Quick output discharge
- FOWLP 0.76mm×0.76mm×0.50mm-4B package

APPLICATIONS

- Smartphones and Tablets
- Portable Devices
- Wearables

GENERAL DESCRIPTION

The AW35121 is a load switch with output slew rate control. The device integrates a 64mΩ (typ.) P-channel MOSFET, which can operate over a wide input range of 1.2V to 5.5V.

The AW35121 features output slew rate control, limiting inrush current during turn-on to protect downstream devices.

TYPICAL APPLICATION CIRCUITS

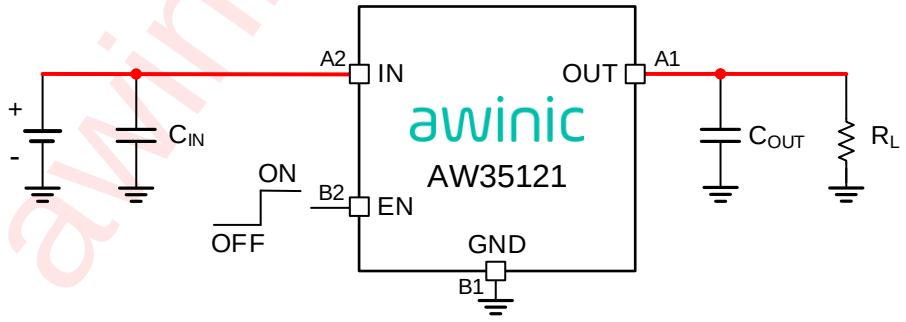


Figure 1 Typical Application circuit of AW35121

PIN CONFIGURATION AND TOP MARK

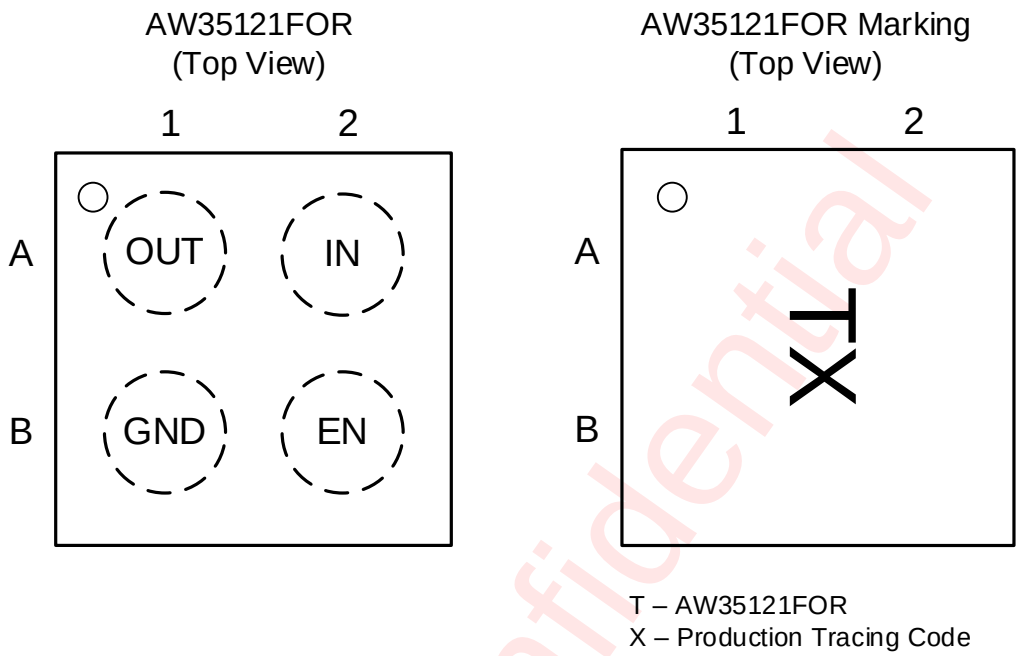


Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

Pin	Name	Description
A1	OUT	Switch output
A2	IN	Switch input and power supply
B1	GND	Device ground
B2	EN	Switch control input, active high, internal 6.85MΩ pull down resistor.

FUNCTIONAL BLOCK DIAGRAM

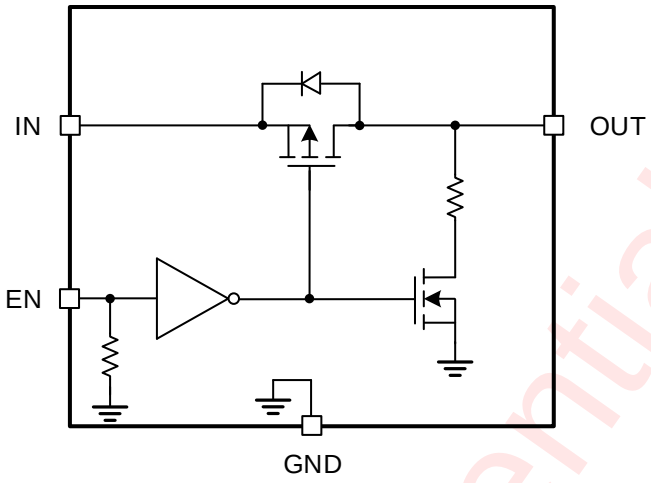


Figure 3 Functional Block Diagram

TYPICAL APPLICATION CIRCUITS

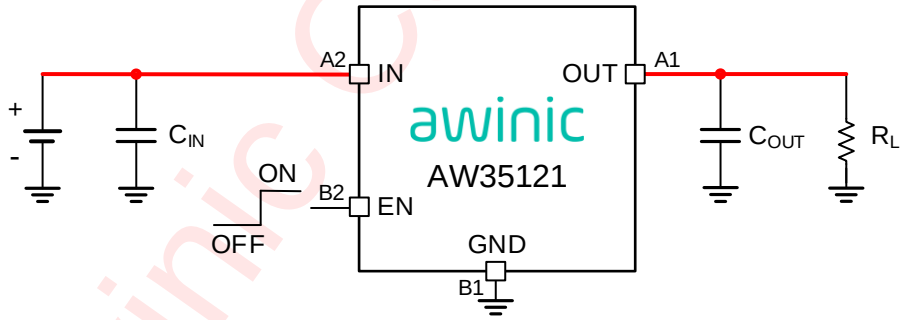


Figure 4 Typical Application circuit of AW35121

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW35121FOR	-40℃～85℃	FOWLP 0.76mm×0.76 mm-4B	T	MSL1	ROHS+HF	3000 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS		RANGE
Supply Voltage Range V_{IN}		-0.3V to 6V
Input Voltage Range	EN	-0.3V to 6V
Output Voltage Range	OUT	-0.3V to 6V
Maximum Continuous Switch Current for VIN ≥ 2V(NOTE 2)		1.5A
Maximum Peak Switch Current for VIN ≥ 2.5V(NOTE 3)		2A
Junction-to-ambient Thermal Resistance θ_{JA}(NOTE 4)		184°C/W
Operating Free-air Temperature Range		-40°C to 85°C
Maximum Junction Temperature T_{JMAX}		150°C
Storage Temperature T_{STG}		-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)		260°C
ESD		
HBM (Human Body Model) (NOTE 5)		±2kV
CDM(Charged Device Model) (NOTE 6)		±1.5kV
MM(Machine Model) (NOTE 7)		±200V
Latch-Up		
Latch-Up (NOTE 8)		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Limited by thermal design.

NOTE3: Limited by thermal design, and tested in 10ms width pulse current.

NOTE4: Thermal resistance from junction to ambient is highly dependent on PCB layout.

NOTE5: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE6: All pins. Test Condition: ESDA/JEDEC JS-002-2014.

NOTE7: All pins. Test Condition: JESD22-A115C.

NOTE8: Test Condition: JESD78E.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input Voltage	1.2		5.5	V
V_{EN}	EN Voltage	0		5.5	V
V_{OUT}	Output Voltage	0		V_{IN}	V
C_{IN}	Input capacitance	0.1	1		μF
C_{OUT}	Output load capacitance	0.1	1		μF

ELECTRICAL CHARACTERISTICS

T_A = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V_{IN} = 5V, C_{IN} = 1μF, I_{IN}≤ 1.5A and T_A = 25°C.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
I_Q	Input quiescent current	V_{IN}=3.3V, V_{EN}=3.3V, I_{OUT}=0A, T_A=25°C		2	12	nA
		V_{IN}=3.3V, V_{EN}=3.3V, I_{OUT}=0A, T_A=85°C		9		nA
		V_{IN}=5.5V, V_{EN}=5.5V, I_{OUT}=0A, T_A=25°C		5	25	nA
		V_{IN}=5.5V, V_{EN}=5.5V, I_{OUT}=0A, T_A=85°C		10		nA
I_{SD}	Shutdown current from IN to GND	V_{IN}=1.2V, V_{EN}=0V, T_A=25°C		2		nA
		V_{IN}=1.8V, V_{EN}=0V, T_A=25°C		2		nA
		V_{IN}=3.3V, V_{EN}=0V, T_A=25°C		4	44	nA
		V_{IN}=4.0V, V_{EN}=0V, T_A=25°C		7		nA
		V_{IN}=4.5V, V_{EN}=0V, T_A=25°C		22		nA
		V_{IN}=5.0V, V_{EN}=0V, T_A=25°C		62	970	nA
		V_{IN}=5.0V, V_{EN}=0V, T_A=55°C		90		nA
		V_{IN}=5.0V, V_{EN}=0V, T_A=85°C		350		nA
		V_{IN}=5.5V, V_{EN}=0V, T_A=25°C		171		nA
I_{LEAKEN}	EN pin leakage current	V_{IN}=0V, V_{EN}=5.0V			1.5	μA
R_{EN}	EN pin pull down resistor	V_{EN}=5.0V		6.85		MΩ
POWER SWITCH						
R_{dson}	Internal switch MOSFET on-state resistance	V_{IN}=5.5V, V_{EN}=high, I_{OUT}=200mA, T_A=25℃		50		mΩ
		V_{IN}=4.2V, V_{EN}=high, I_{OUT}=200mA, T_A=25℃		56		
		V_{IN}=3.3V, V_{EN}=high, I_{OUT}=200mA, T_A=25℃		64		
		V_{IN}=3.0V, V_{EN}=high, I_{OUT}=200mA, T_A=25℃		68	120	
		V_{IN}=1.8V, V_{EN}=high, I_{OUT}=200mA, T_A=25℃		109		
		V_{IN}=1.2V, V_{EN}=high, I_{OUT}=200mA, T_A=25℃		225		
R_{DIS}	Output discharge resistance	V_{IN}=3.3V, V_{EN}=low, T_A=25℃, I_{OUT} Sinking 2mA	50	75	100	Ω
t_R	Output rise time	V_{IN}=3.6V, C_{OUT}=1μF, R_{OUT}=30Ω		165		μs
t_F	Output fall time	V_{IN}=3.6V, C_{OUT}=1μF, R_{OUT}=30Ω		42		μs
t_{ON}	Switch turn on time	V_{IN}=3.6V, C_{OUT}=1μF, R_{OUT}=30Ω		238		μs

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{OFF}	Switch turn off time	V_{IN}=3.6V, C_{OUT}=1μF, R_{OUT}=30Ω		12		μs
t_{EN}	Enable time	V_{IN}=3.6V, C_{OUT}=1μF, R_{OUT}=30Ω		130		μs
V_{IH}	EN input high threshold level		1.2			V
V_{IL}	EN input low threshold level				0.5	V

TIMING DIAGRAM

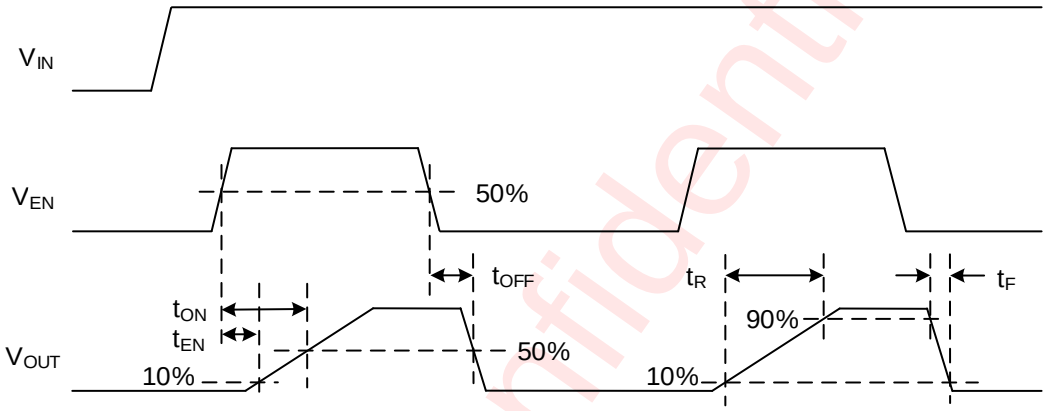


Figure 5 AW35121 Timing Diagram

TYPICAL CHARACTERISTICS

Ambient temperature is 25°C, C_{IN} = C_{OUT}=1μF, unless otherwise noted.

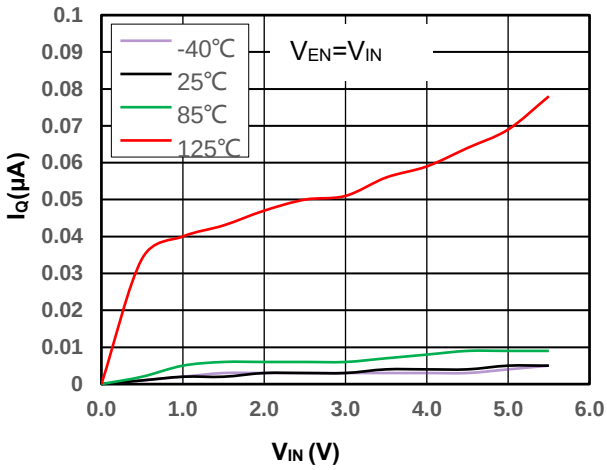


Figure 6 Quiescent Current vs. V_{IN}, No load

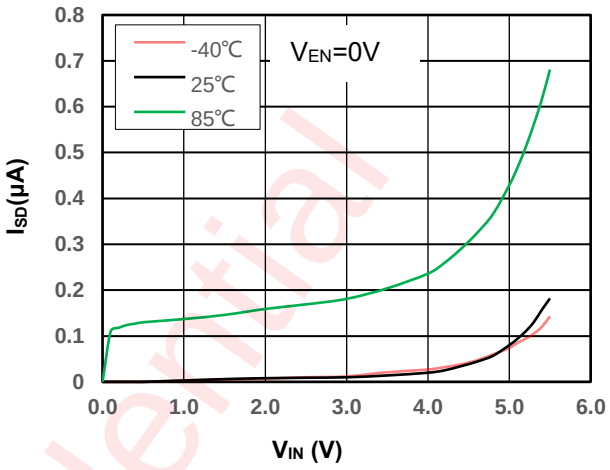


Figure 7 IN Shutdown Current vs. V_{IN}

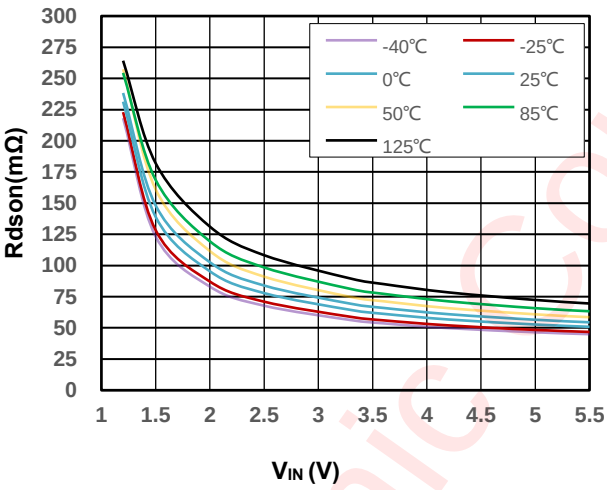


Figure 8 Rdson vs. V_{IN}(I_{OUT}=200mA)

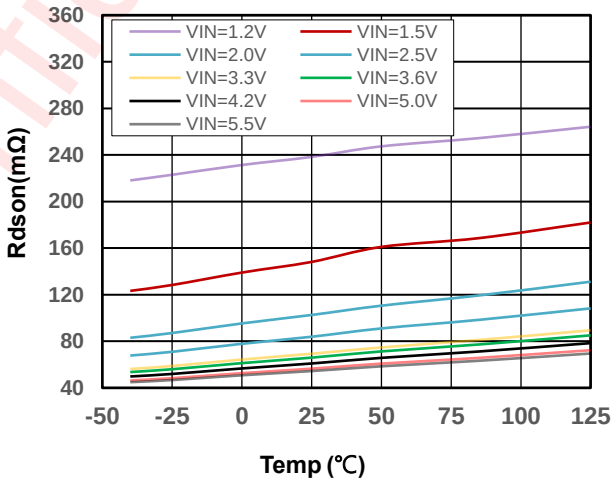


Figure 9 Rdson vs. Temperature(I_{OUT}=200mA)

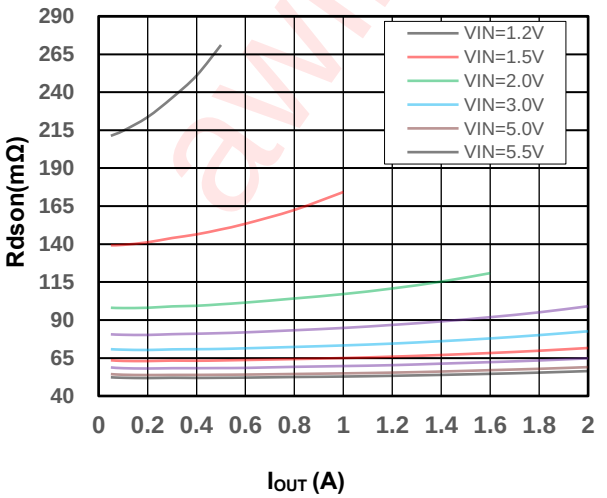


Figure 10 Rdson vs. I_{OUT}

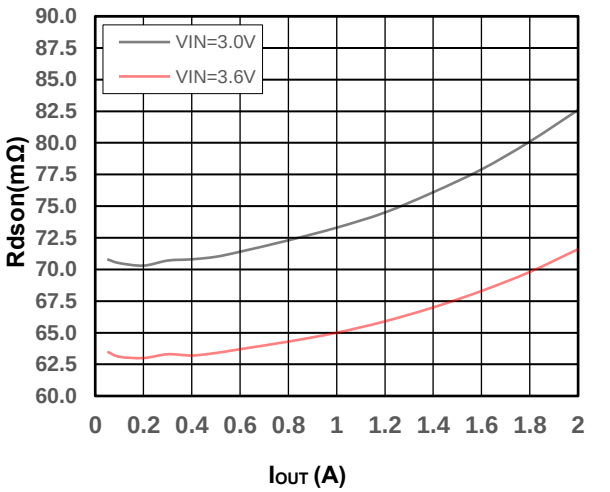
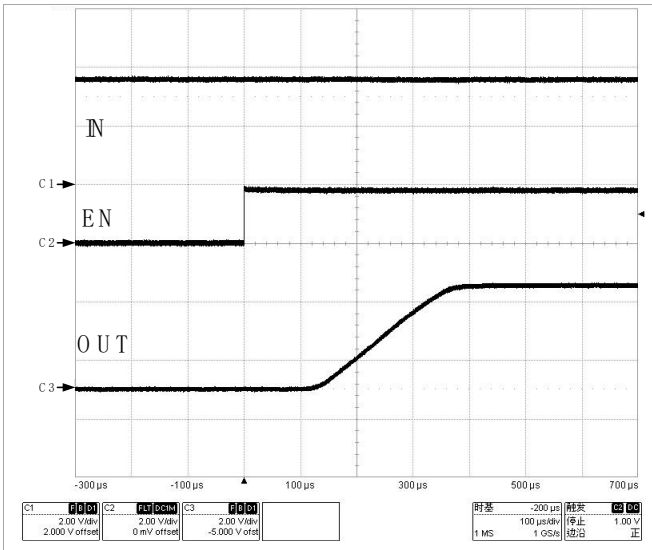
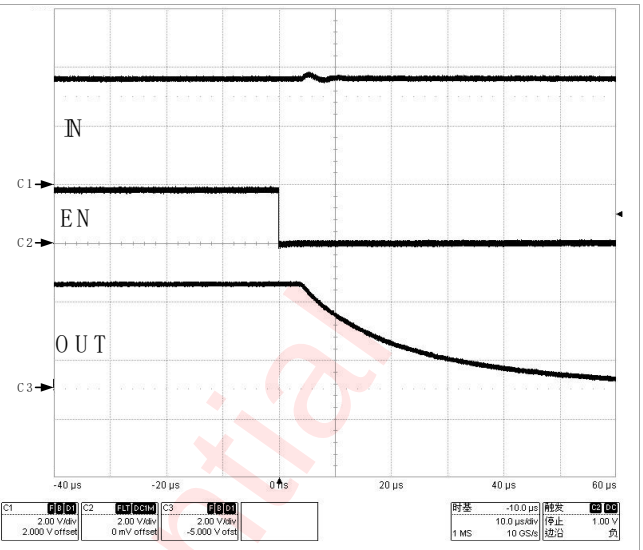


Figure 11 Rdson vs. I_{OUT}



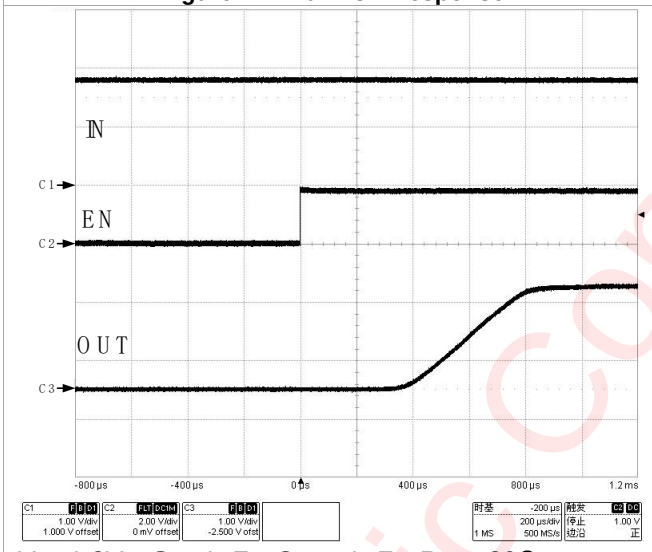
V_{IN}=3.6V，C_{IN}=1μF，C_{OUT}=1μF，R_{load}=30Ω

Figure 12 Turn On Response



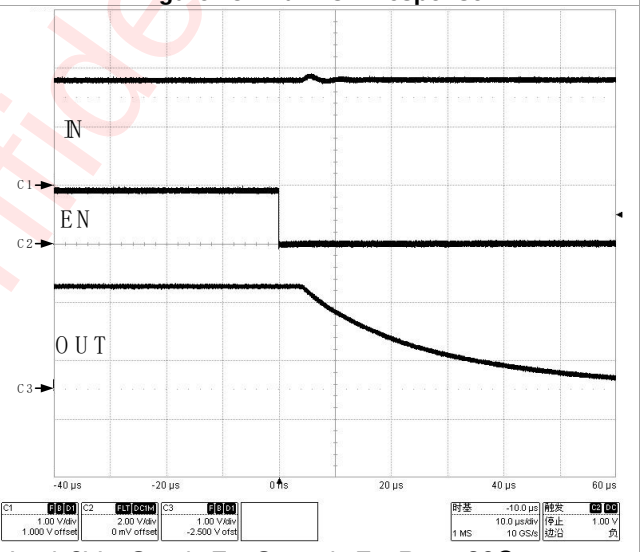
V_{IN}=3.6V，C_{IN}=1μF，C_{OUT}=1μF，R_{load}=30Ω

Figure 13 Turn Off Response



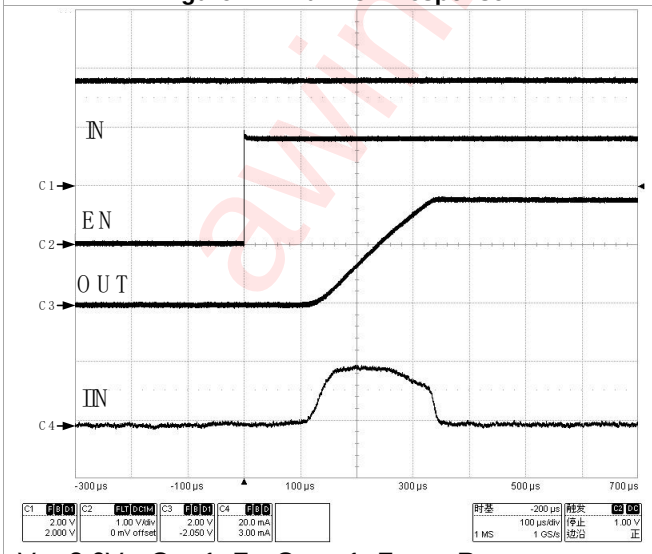
V_{IN}=1.8V，C_{IN}=1μF，C_{OUT}=1μF，R_{load}=30Ω

Figure 14 Turn On Response



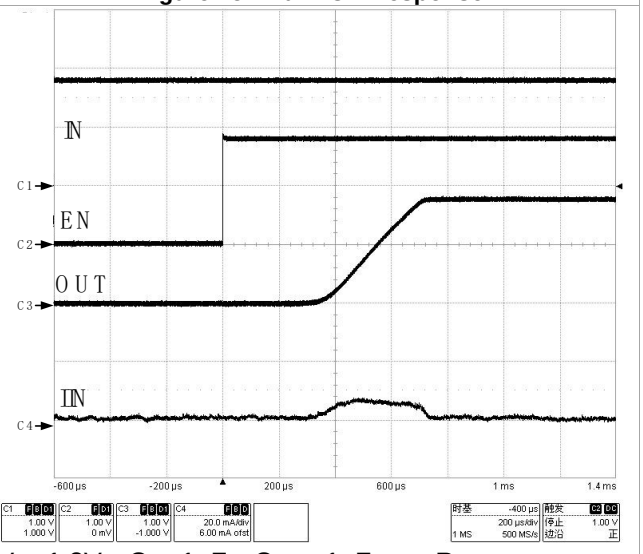
V_{IN}=1.8V，C_{IN}=1μF，C_{OUT}=1μF，R_{load}=30Ω

Figure 15 Turn Off Response



V_{IN}=3.6V，C_{IN}=1μF，C_{OUT}=1μF，no R_{load}

Figure 16 Inrush Current with C_{OUT}=1μF



V_{IN}=1.8V，C_{IN}=1μF，C_{OUT}=1μF，no R_{load}

Figure 17 Inrush Current with C_{OUT}=1μF

DETAILED FUNCTIONAL DESCRIPTION

The AW35121 integrates a high side P channel MOSFET load switch, and provides a low on-resistance for a low voltage drop across the device. A controlled slew rate is used in applications to limit the inrush current. The part can be turned on, with a supply voltage from 1.2V to 5.5V.

TURN ON/OFF CONTROL

Enable pin is active high. The device is opened when EN pin is tied low (disable) or pulled down by internal 6.85MΩ resistor, forcing PMOS switch off. The IN/OUT path is activated with a minimum Vin of 1.2V and EN forced to high level.

Table 1. Functional Table

EN	IN to OUT	OUT to GND
Low	OFF	ON
High	ON	OFF

SLEW RATE CONTROL

When the switch is enabled, the device regulates the gate voltage of MOSFET, and controls the V_{OUT} slew rate during t_R to avoid a large input inrush current. The feature reduces the interference to the power supply.

QUICK OUTPUT DISCHARGE

The AW35121 includes the Quick Output Discharge (QOD) feature, in order to discharge the application capacitor connected on OUT pin. When EN pin is set to low level (disable state), a discharge resistance with a typical value of 75Ω connected between the output and ground, pulls down the output and prevents it from floating.

APPLICATION INFORMATION

POWER SUPPLY RECOMMENDATIONS

The device is designed to operate with a V_{IN} range of 1.2V to 5.5V. This supply must be well regulated and placed as close to the device terminals as possible. It must also be able to withstand all transient and load currents, using a recommended input capacitance of 1μF if necessary. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10μF may be sufficient.

MANAGING INRUSH CURRENT

When the switch is enabled, the output capacitors must be charged up from 0V to V_{IN}. A input inrush current will appear. The Inrush current can be calculated using Equation 1:

$$Iinrush = C_{OUT} \frac{dV_{OUT}}{dt} \quad (1)$$

where:

- C_{OUT} = Output capacitance
- dV_{OUT} = Output voltage, equals to V_{IN}
- dt = Rise time t_R.

The AW35121 offers a controlled slew rate for minimizing inrush current.

POWER DISSIPATION

The power dissipation produced by the power MOSFET Rdson in ON-state can be calculated with the following equation:

$$P_D = Rdson \times (I_{OUT})^2 \quad (2)$$

Where:

- P_D = Power dissipation (W)
- R_{dson} = Power MOSFET on resistance (Ω)
- I_{OUT} = Output current (A)

THERMAL CONSIDERATIONS

Main contributor in term of junction temperature T_J(max) is the power dissipation, and T_J(max) should be restricted to 125°C under ON-state. Junction temperature is directly proportional to power dissipation in the device, it can be calculated by the following equation:

$$T_J = T_A + R_{\theta JA} \times P_D \quad (3)$$

Where:

- T_J = Junction temperature of the device
- T_A = Ambient temperature
- P_D = Power dissipation of the device
- $R_{\theta JA}$ = Junction to ambient thermal resistance. This parameter is highly dependent on board layout.

PCB LAYOUT CONSIDERATION

AW35121 is a low ON-Resistance load switch. In order to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

1. All the peripherals should be placed as close to the device as possible. Place the input capacitor C_{IN} on the top layer (same layer as the AW35121) and close to IN pin, and place the output capacitor C_{OUT} on the top layer (same layer as the AW35121) and close to OUT pin.

2. The AW35121 integrate an up to 1.5A rated PMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R\theta_{JA}$ of the package can be decreased, allowing higher power dissipation. Blue bold paths on Figure 18 are power lines that will flow large current, please route them on PCB as straight, wide and short as possible.

3. Use rounded corners on the power trace from the power supply connector to AW35121 to decrease EMI coupling.

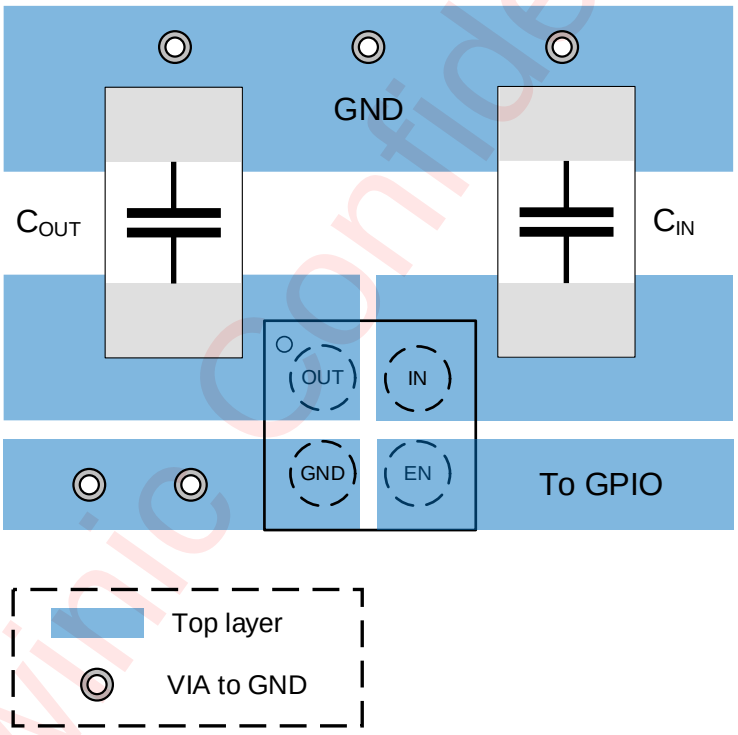
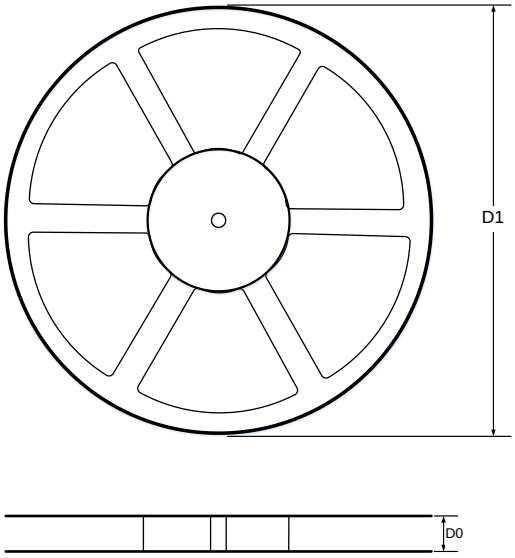


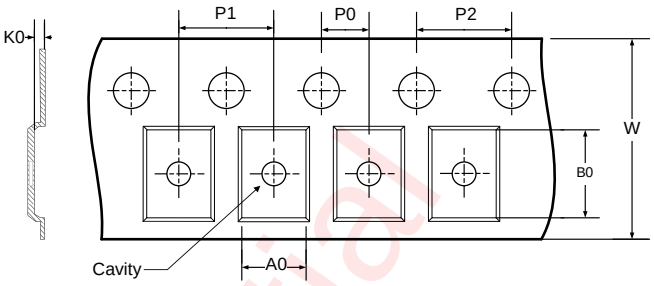
Figure 18 PCB layout example

TAPE AND REEL INFORMATION

REEL DIMENSIONS

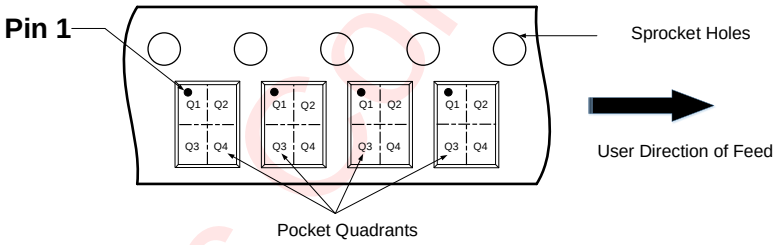


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



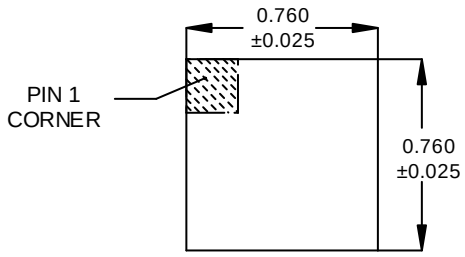
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

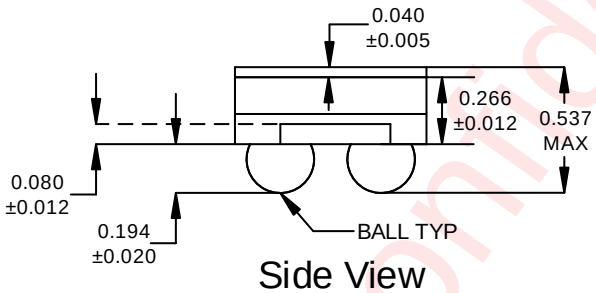
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179	9.2	0.85	0.85	0.59	2	4	4	8	Q1

All dimensions are nominal

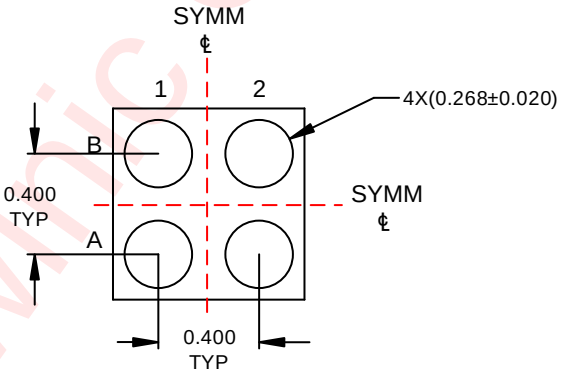
PACKAGE DESCRIPTION



Top View



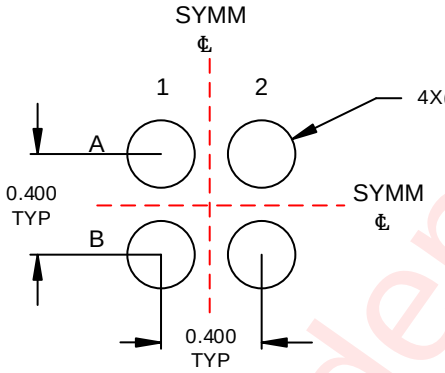
Side View

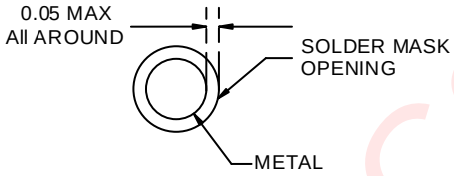


Bottom View

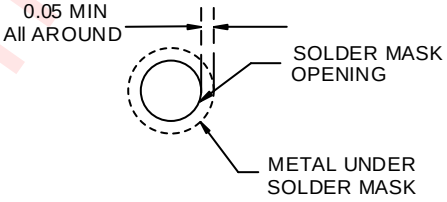
Unit：mm

LAND PATTERN DATA





NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

REVISION HISTORY

Version	Date	Change Record
V1.0	Nov 2019	Datasheet V1.0 Released
V1.1	Jan 2023	Modified Pin Configuration and Top Mark; Modified Figure 18 PCB layout example.

DISCLAIMER

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