

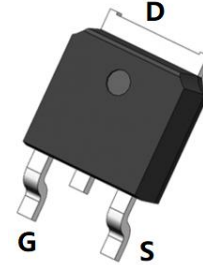


SWD40P04

P-channel Enhancement Mode Power MOSFET

Features

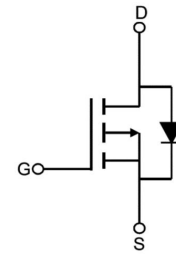
- $V_{DS} = -40V$, $I_D = -40A$
 $R_{DS(ON)} < 13m\Omega$ @ $V_{GS} = -10V$
 $R_{DS(ON)} < 22m\Omega$ @ $V_{GS} = -4.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired



TO-252-2L

Application

- PWM Applications
- Load Switch
- Power Management



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
40P04	SWD40P04	TO-252-2L	13"	2500	25000

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		-40	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ C$	-40	A
		$T_C = 100^\circ C$	-26	A
I_{DM}	Pulsed Drain Current ^{note1}		-160	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}		144	mJ
P_D	Power Dissipation	$T_C = 25^\circ C$	41.6	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		3.6	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	$^\circ C$

**Electrical Characteristics** ($T_J=25^{\circ}\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D = -250μA	-40	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -40V, V _{GS} =0V	-	-	-1	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D = -250μA	-1.0	-1.7	-2.5	V
R _{DS(on)}	Static Drain-Source on-Resistance note3	V _{GS} = -10V, I _D = -20A	-	10	13	mΩ
		V _{GS} = -4.5V, I _D = -10A	-	15	22	
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = -20V, V _{GS} =0V, f=1.0MHz	-	3800	-	pF
C _{oss}	Output Capacitance		-	329	-	pF
C _{rss}	Reverse Transfer Capacitance		-	289	-	pF
Q _g	Total Gate Charge	V _{DS} = -20V, I _D = -20A, V _{GS} = -10V	-	68	-	nC
Q _{gs}	Gate-Source Charge		-	10	-	nC
Q _{gd}	Gate-Drain(“Miller”) Charge		-	14	-	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} = -20V, I _D = -20A, V _{GS} = -10V, R _{GEN} =2.4Ω	-	10	-	ns
t _r	Turn-on Rise Time		-	82	-	ns
t _{d(off)}	Turn-off Delay Time		-	93	-	ns
t _f	Turn-off Fall Time		-	74	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	-40	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-160	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S = -30A	-	-0.8	-1.2	V
trr	Reverse Recovery Time	V _{GS} =0V, I _S = -30A, di/dt=100A/μs	-	20	-	ns
Qrr	Reverse Recovery Charge		-	13	-	nC

Notes: 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: $T_J=25^{\circ}\text{C}$, $V_{DD}=-20V$, $V_G=-10V$, $L=0.5mH$, $R_G=25\Omega$, $I_{AS}=-24A$ 3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

Typical Performance Characteristics

Figure1: Output Characteristics

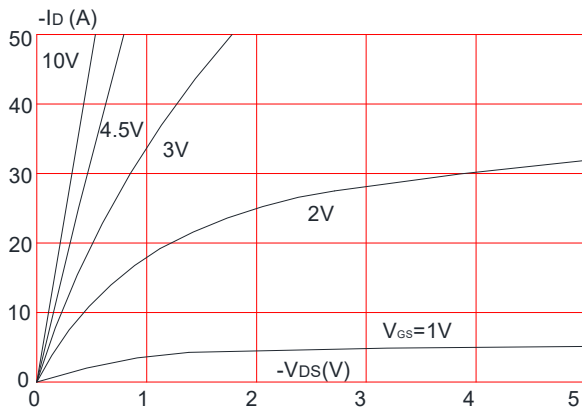


Figure 2: Typical Transfer Characteristics

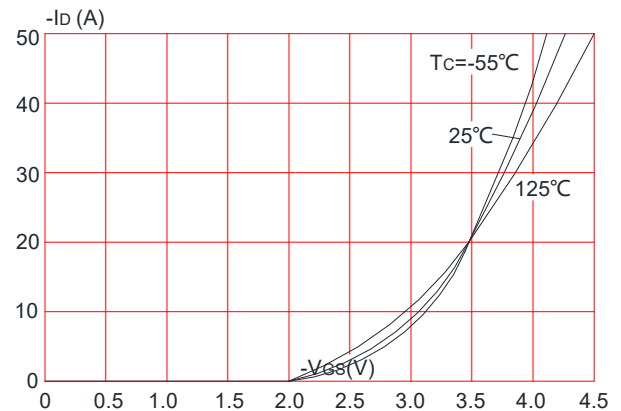


Figure 3: On-resistance vs. Drain Current

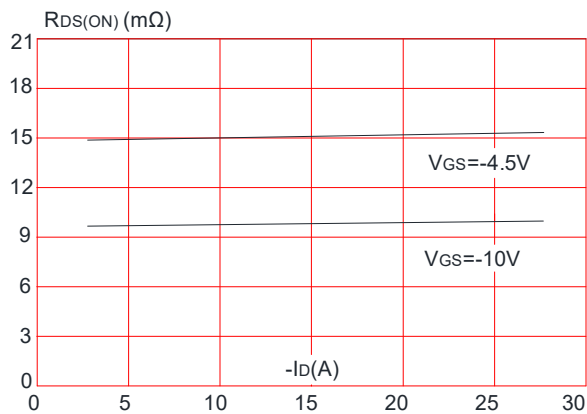


Figure 4: Body Diode Characteristics

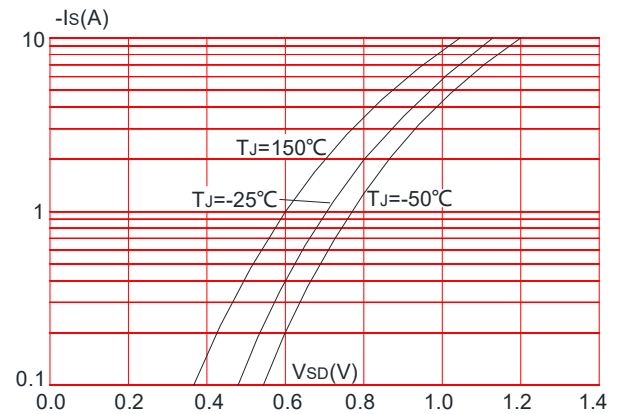


Figure 5: Gate Charge Characteristics

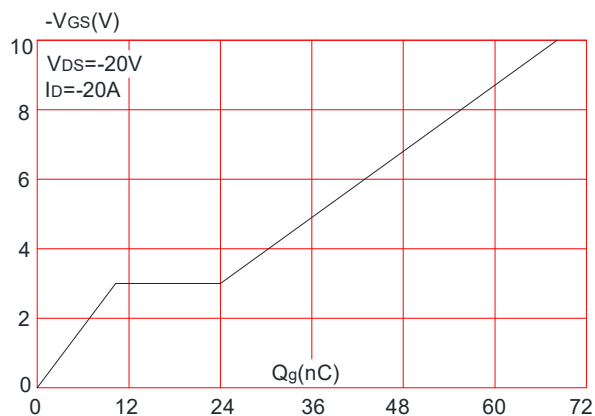


Figure 6: Capacitance Characteristics

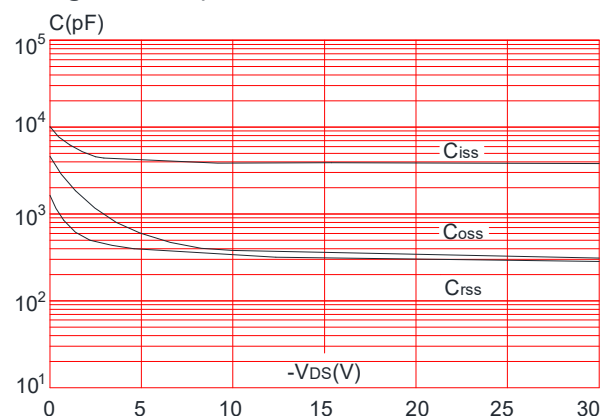


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

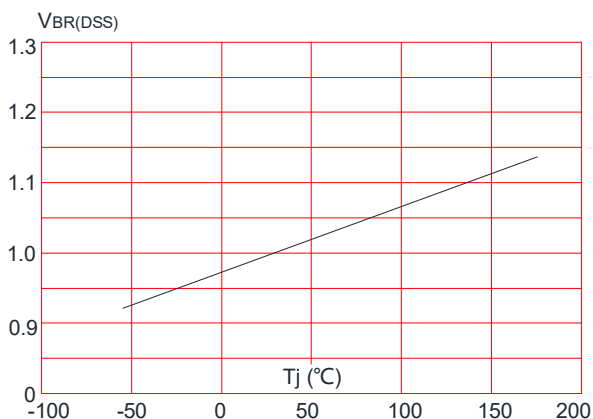


Figure 8: Normalized on Resistance vs. Junction Temperature

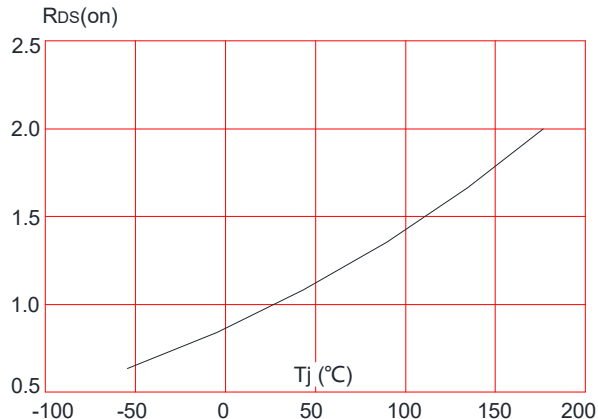


Figure 9: Maximum Safe Operating Area

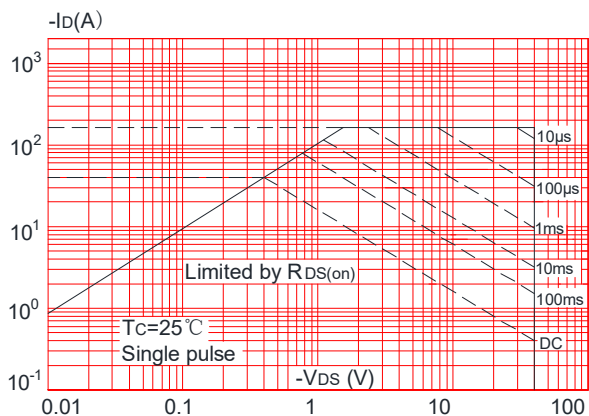


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

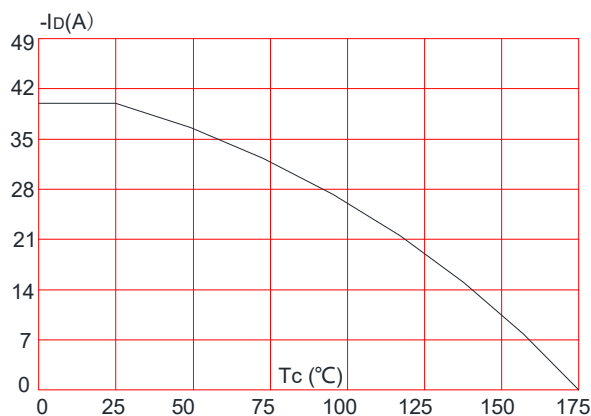
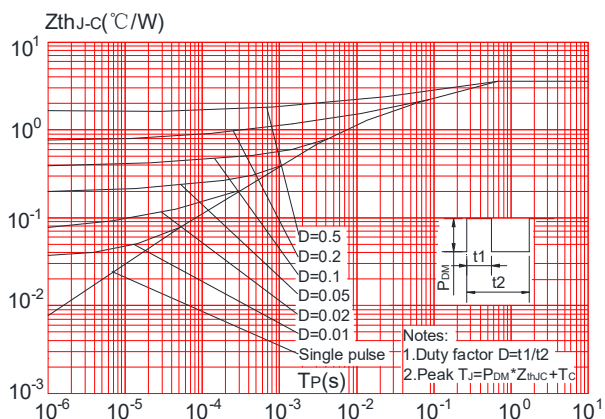
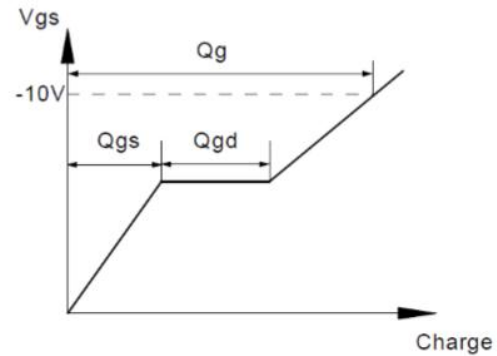
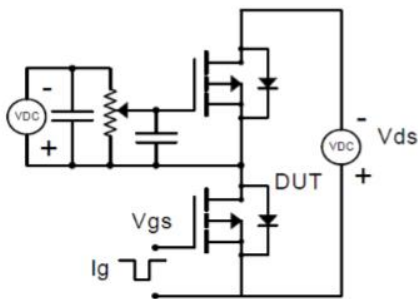


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

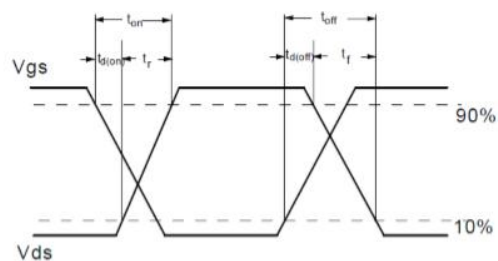
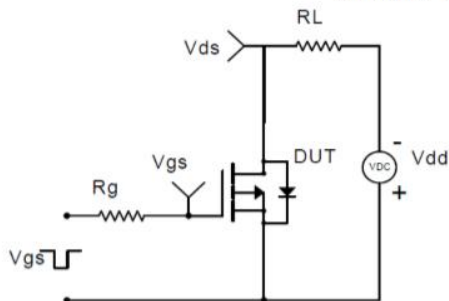


Test Circuit

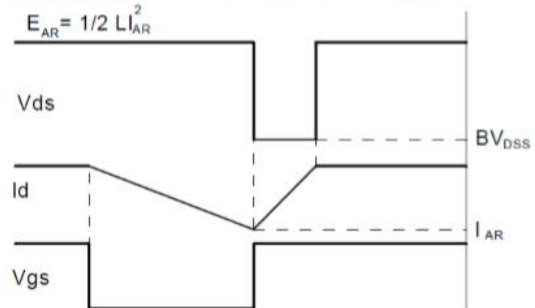
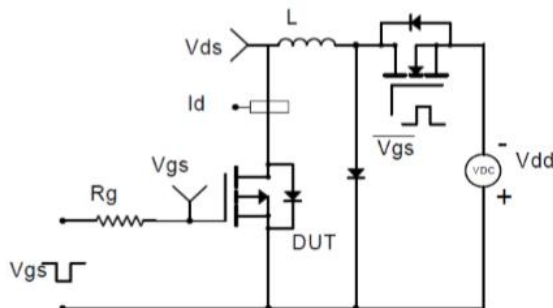
Gate Charge Test Circuit & Waveform



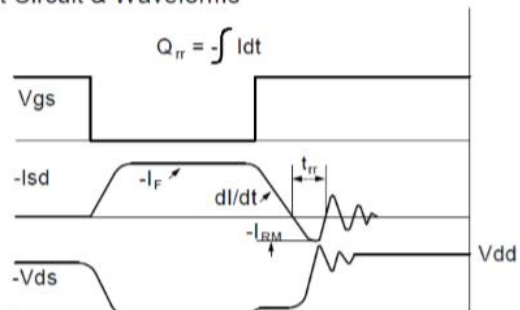
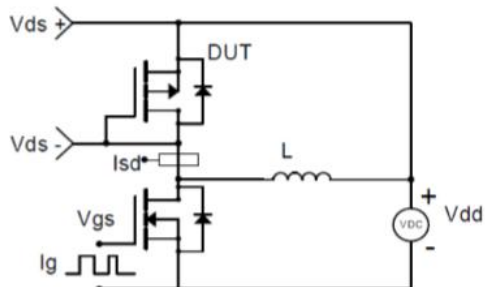
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

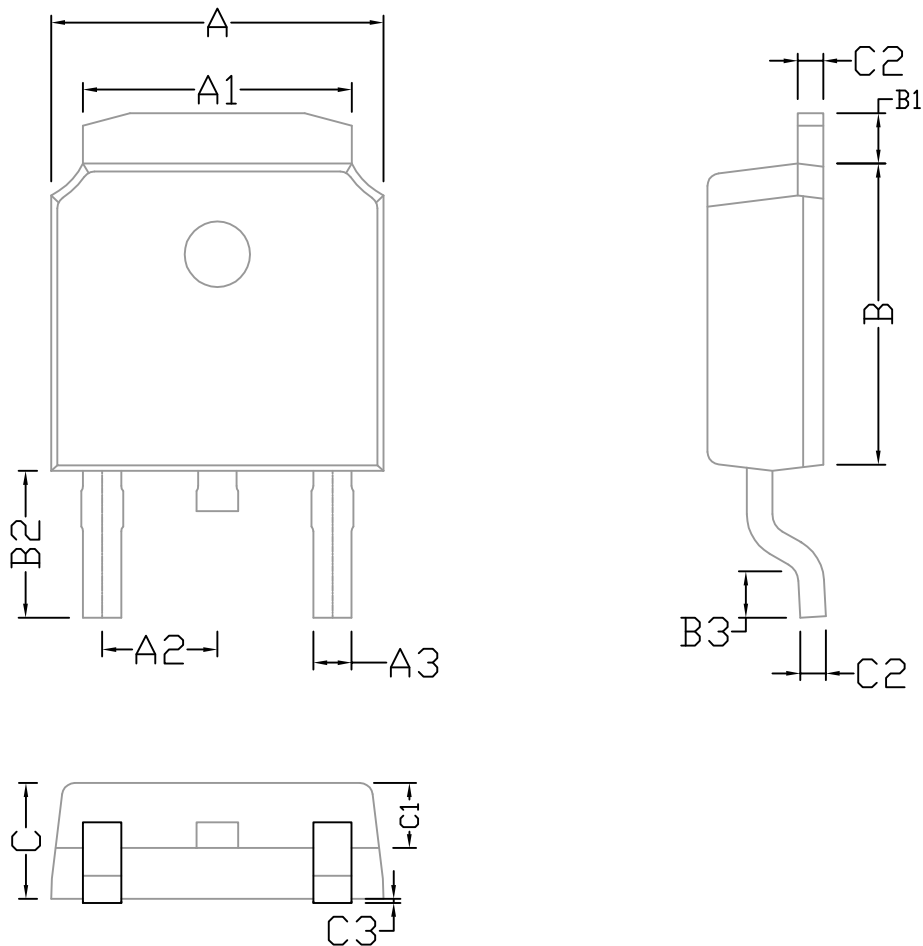




SWD40P04

P-channel Enhancement Mode Power MOSFET

Package Mechanical Data-TO-252-2L



标注	最小	标准	最大	标注	最小	标准	最大	标注	最小	标准	最大
A	6.50	6.60	6.70	B	6.05	6.10	6.15	C	2.25	2.30	2.35
A1	5.28	5.33	5.38	B1	0.95	1.00	1.05	C1	0.76	0.81	0.86
A2	2.23	2.28	2.33	B2	2.85	2.9	2.95	C2	0.45	0.50	0.55
A3	0.70	0.75	0.80	B3	1.45	1.50	1.55	C3	0.01	0.05	0.10