

AW9617 Level Translating Fm+ I²C Bus Repeater

Features

- Two-channel bidirectional I²C buffer
- Support for Standard-Mode, Fast-mode, and Fast-mode+ I²C Operation
- Operating supply voltage range of 0.8V to 5.5V on A Side
- Operating supply voltage range of 2.2V to 5.5V on B-Side
- Voltage-level translation from 0.8V to 5.5V and 2.2V to 5.5V
- Active-High repeater-enable input
- Open-drain I²C I/O
- 5.5V tolerant I²C and enable pins
- Latching free operation
- Powered-off high-impedance I²C bus pins
- Support for clock stretching and multiple master arbitration across the device
- Operation temperature range: -40°C~105°C
- MSOP-8L package

General Description

The AW9617 is a CMOS dual bidirectional buffer intended for I²C bus and SMBus systems. The device provides bidirectional voltage-level translation (up-translation and down-translation) between low voltages (down to 0.8V) and higher voltages (2.2V to 5.5V) in mixed-mode applications. This device enables I²C and similar bus systems to be extended, without degradation of performance even during level shifting.

The AW9617 buffers both the serial data (SDA) and the serial clock (SCL) signals on the I²C bus, allowing two buses of 550pF at 1MHz or up to 4000pF at lower speeds. This device can also be used to separate two halves of a bus for voltage and capacitance.

Applications

- Servers
- Routers (Telecom Switching Equipment)
- Industrial Equipment
- Products with Many I²C Slaves and/or Long PCB Traces

Typical Application Circuit

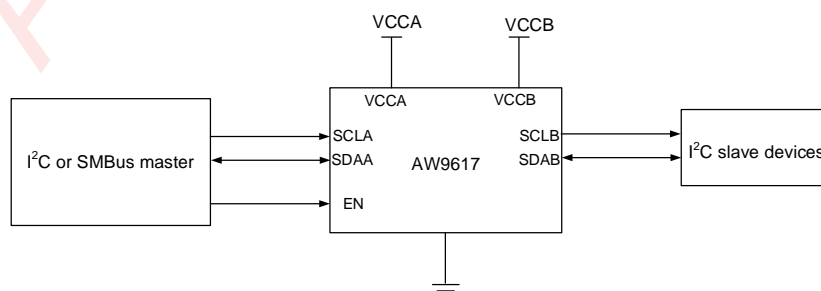


Figure 1 AW9617 Simplified Application Circuit

Pin Configuration And Top Mark

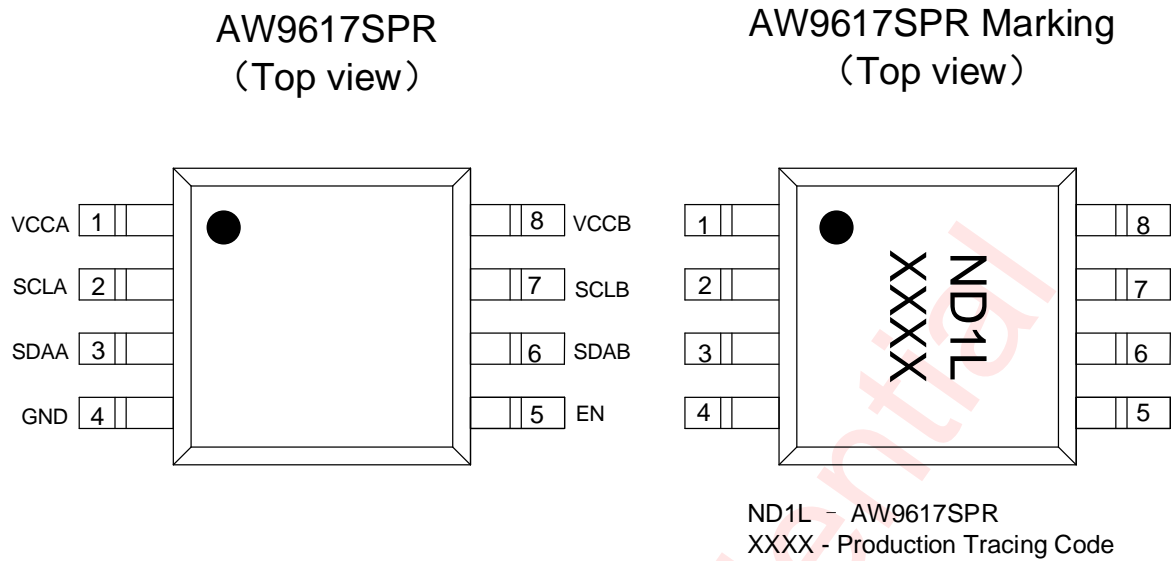


Figure 2 Pin Configuration and Marking

Pin Definition

Pin No.		Description
Name	AW9617	
VCCA	1	Port A supply voltage(0.8V~5.5V)
SCLA	2	Serial clock port A bus
SDAA	3	Serial data port A bus
GND	4	Supply ground
EN	5	Active high repeater enable input
SDAB	6	Serial data port B bus
SCLB	7	Serial clock port B bus
VCCB	8	Port B supply voltage(2.2V~5.5V)

Functional Block Diagram

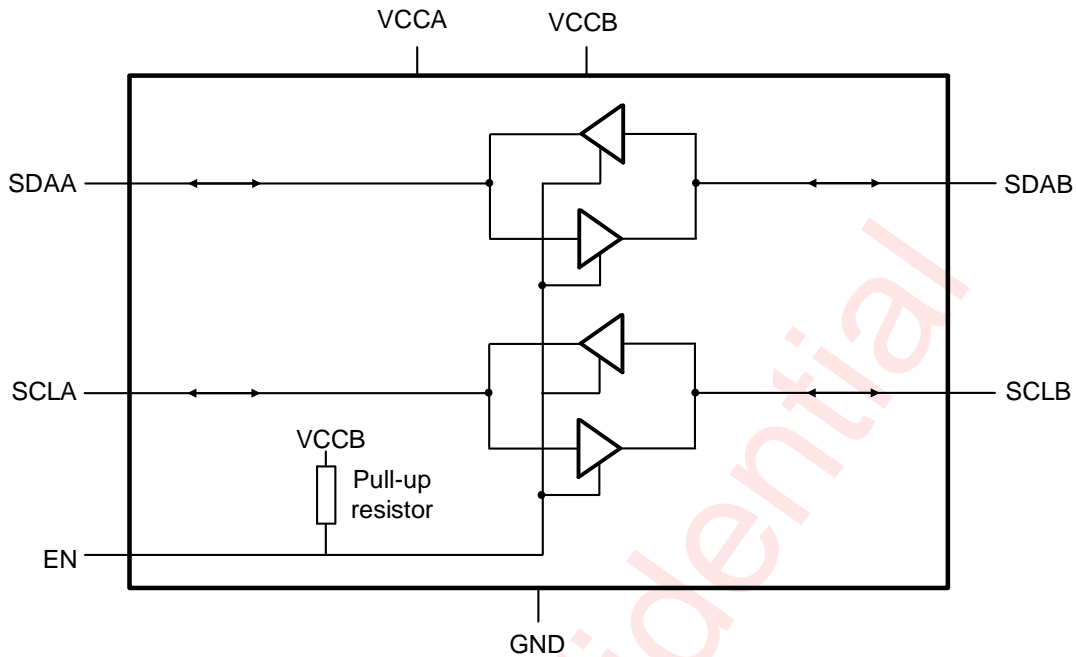


Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW9617SPR	-40°C~105°C	MSOP-8L	ND1L	MSL1	RoHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings^(NOTE1)

Parameter	Description	Range	
V_{CCB}	Supply voltage	-0.5V to 7V	
V_{CCA}	Supply voltage	-0.5V to 7V	
$V_{I/O}$	Voltage on an input/output pin: Port A and port B; enable pin(EN)	-0.5V to 7V	
I_{IK}	Input clamp current SCLA,SDAA,SCLB,SDAB; $V_I < 0$	-50mA	
I_{OK}	Out clamp current SCLA,SDAA,SCLB,SDAB; $V_O < 0$	-50mA	
I_O	Continuous output current	±50mA	
	Continuous current through VCC or GND	±100mA	
T_{stg}	Storage temperature	-65°C to 150°C	
T_J	Max Junction Temperature	$V_{CC} \cong 3.6V$	130°C
		$V_{CC} \cong 5.5V$	90°C

Parameter	Description	Range
ESD(Including CDM HBM)(NOTE2)	HBM	±7kV
	CDM	±1.5kV
Latch-Up	Test condition: JESD78F	+IT: 450mA -IT: -450mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The HBM test method: ESDA/JEDEC JS-001-2023, the CDM test method: ESDA/JEDEC JS-002-2022.

Recommended Operating Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V _{CCA} (NOTE3)	Supply voltage	(NOTE4)	0.8	5.5	V
V _{CCB}	Supply voltage		2.2	5.5	V
V _{IO}	Input/output voltage	SCLA,SDAA,SCLB,SDAB	0	5.5	V
I _{OLA}	Low-level output current	SCLA,SDAA		50	mA
I _{OLB}	Low-level output current	SCLB,SDAB		50	mA
T _A	Operation ambient temperature		-40	105	°C

NOTE3: V_{CCA} may be as high as 5.5V for overvoltage tolerance but $0.4 \times V_{CCA} + 0.8V \leq V_{CCB}$ for the channels to be enabled and functional normally.

NOTE4: For part to function, $0.4 \times V_{CCA}$ must be equal or less than $V_{CCB} - 0.8V$. The voltage on the A port can still be up to 5.5V without damage to the pins.

Electrical Characteristics

VCCA=0.8V to 5.5V; VCCB=2.2V to 5.5V; GND=0V; Tamb=-40°C to +105°C; unless otherwise specified. Typical values measured with VCCA=0.95V and VCCB=2.5V at 25°C, unless otherwise noted.

Parameter		Test Condition	Min.	Typ.	Max.	Unit
Supplies						
V _{CCB}	Supply voltage port B		2.2	-	5.5	V
V _{CCA}	Supply voltage port A		0.8	-	5.5	V
I _{CCA}	Supply current port A	VCCA=0.95V	-	-	8	μA
		VCCA=5.5V	-	-	50	μA
I _{CCHB}	Port B high level supply current	VCCB=5.5V; SDAn=SCLn=VCCn	-	1.2	2.5	mA
I _{CLLB}	Port B low level supply current	VCCB=5.5V; one SDA and one SCL=GND; other SDA and SCL open(with pull-up resistors)	-	1.5	2.9	mA
Input and output SDAB and SCLB						
V _{IH}	HIGH level input voltage		0.7× VCCB	-	5.5	V
V _{IL}	LOW Level input voltage		-0.5	-	0.4	V
V _{IK}	Input clamping voltage	I _I =-18mA	-1.2	-	-0.3	V
I _{LI}	Input leakage current	V _I =5.5V	-1	-	+1	μA
I _{IL}	LOW level input current	SDA: V _I =0.2V; SCL: V _I =0.2V; EN=0V	-	-	10	μA
V _{OL}	LOW level output voltage	I _{OL} =150μA; VCCB=2.2V ^(NOTE5)	0.47	-	-	V
		I _{OL} =13mA; VCCB=2.2V ^(NOTE6)	-	0.54	0.6	V
V _{OL} -V _{IL}	Difference between V _{OL} and V _{IL}	V _{OL} at I _{OL} =1mA; guaranteed by design	60	90	160	mV
C _{io}	Input/output capacitance	V _I =3V or 0V; VCCB=3.3V; EN=0	-	5	10	pF
		V _I =3V or 0V; VCC=0V	-	5	10	pF
Input and output SDAA and SCLA						
V _{IH}	HIGH level input voltage		0.7× VCCA	-	5.5	V
V _{IL}	LOW Level input voltage	(NOTE7)	-0.5	-	0.25× VCCA(NOTE8)	V
V _{IK}	Input clamping voltage	I _I =-18mA	-1.2	-	-0.3	V

Parameter		Test Condition	Min.	Typ.	Max.	Unit
I _{LI}	Input leakage current	V _I =5.5V	-1	-	+1	μA
I _{IL}	LOW level input current	SDA: V _I =0.2V; SCL: V _I =0.2V; EN=0V	-	-	10	μA
V _{OL}	LOW level output voltage	I _{OL} =13mA; V _{CCB} =2.2V	-	0.1	0.2	V
C _{io}	Input/output capacitance	V _I =3V or 0V; V _{CCB} =3.3V; EN=0	-	5	10	pF
		V _I =3V or 0V; V _{CC} =0V	-	5	10	pF
Enable						
V _{IH}	HIGH level input voltage		0.7× V _{CCB}	-	5.5	V
V _{IL}	LOW Level input voltage		-0.5	-	0.3× V _{CCB}	V
I _{IL(EN)}	LOW Level input current on pin EN	EN:V _I =0.2V; V _{CCB} =2.2V	-18	-8	-4	μA
I _{LI}	Input leakage current	V _I =V _{CCB}	-1	-	+1	μA
C _{io}	Input/output capacitance	V _I =V _{CCB}	-	4	-	pF

NOTE5: Pull-up should result in I_{OL}≥150μA.

NOTE6: Guaranteed by design and characterization.

NOTE7: V_{IL} for port A with envelope noise must be below 0.3×V_{CCA} for stable performance.

NOTE8: When V_{CCA} is less than 1V, care is required to make certain that the system ground offset and noise are minimized such that there is reasonable difference between the V_{IL} present at the AW9617 A side input and the 0.25×V_{CCA} input threshold.

Dynamic Characteristic

V_{CCA} = 0.8V to 5.5V^(NOTE9); V_{CCB}=2.2V to 5.5V; GND = 0V; Tamb = -40°C to +105°C; unless otherwise specified. ^(NOTE10)

Parameters		Test Condition	Min.	Typ ^(NOTE11)	Max.	Unit
t _{PLH}	LOW to HIGH propagation delay	Port B to port A	-30	-60	-100	ns
t _{PLH2}	LOW to HIGH propagation delay2	Port B to port A ^(NOTE12)	70	85	130	ns
t _{PHL}	HIGH to LOW propagation delay	Port B to port A	50	75	150	ns
t _{TLH}	LOW to HIGH output transition time	Port A ^(NOTE13)	-	60	-	ns

Parameters		Test Condition	Min.	Typ ^(NOTE11)	Max.	Unit
SR _f	Falling slew rate	Port A: 0.7×VCCA to 0.3×VCCA	0.02	0.04	0.10	V/ns
t _{PLH}	LOW to HIGH propagation delay	Port A to port B ^(NOTE14)	40	60	100	ns
t _{PHL}	HIGH to LOW propagation delay	Port A to port B ^(NOTE14)	55	80	170	ns
t _{TLH}	LOW to HIGH output transition time	Port B ^(NOTE13)	-	60	-	ns
SR _f	Falling slew rate	Port B: 0.7×VCCB to 0.3×VCCB	0.025	0.055	0.09	V/ns
t _{en}	Enable time	Quiescent-0.3V; EN HIGH to enable ^(NOTE15)	-	-	100	ns
t _{dis}	Disable time	Quiescent+0.3V; EN LOW to enable ^(NOTE15)	-	-	100	ns

NOTE9: $0.4 \times VCCA + 0.8 \text{ V} \leq VCCB$ for the channels to be enabled and function normally.

NOTE10: Times are specified with loads of 1.35kΩ pull-up resistance and 50pF load capacitance on port A and port B, and a falling edge slew rate of 0.05V/ns input signals. Pull-up voltages are VCCA on port A and VCCB on port B.

NOTE11: Typical values were measured with VCCA=0.95V, VCCB=2.5V at Tamb=25°C, unless otherwise noted.

NOTE12: The t_{PLH2} delay data from port B to port A is measured at 0.45V on port B to 0.5×VCCA on port A.

NOTE13: The t_{TLH} of the bus is determined by the pull-up resistance (1.35kΩ) and the total capacitance (50pF).

NOTE14: The proportional delay data from port A to port B is measured at 0.5×VCCA on port A to 0.5×VCCB on port B.

NOTE15: The enable pin, EN, should only change state when the global bus and the repeater port are in an idle state.

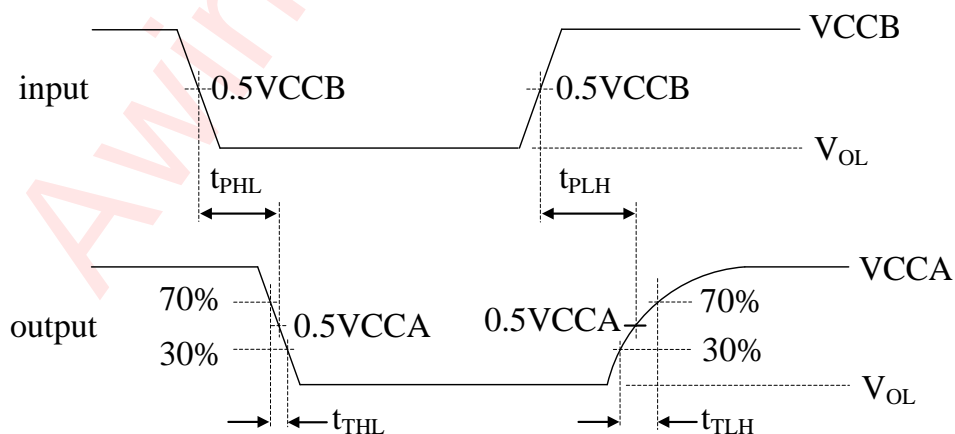


Figure 4 propagation delay and transition times; port B to port A

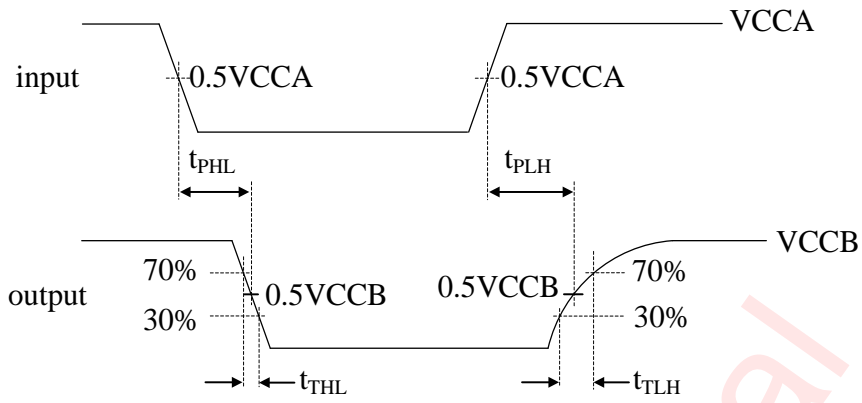


Figure 5 propagation delay and transition times; port A to port B

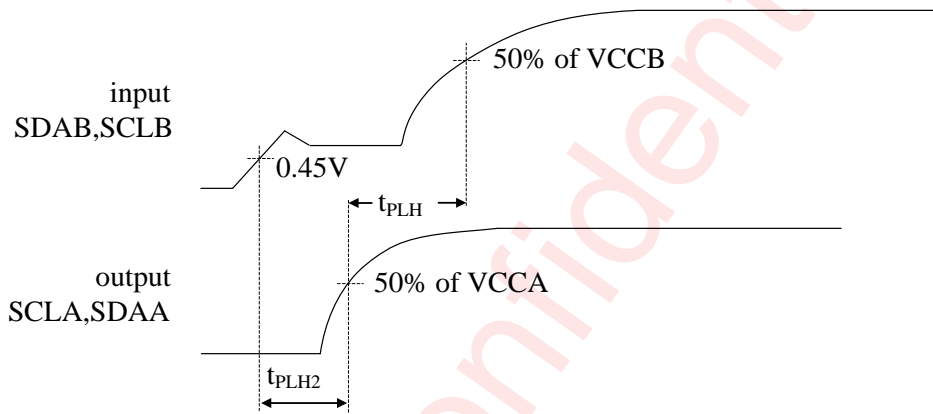


Figure 6 propagation delay

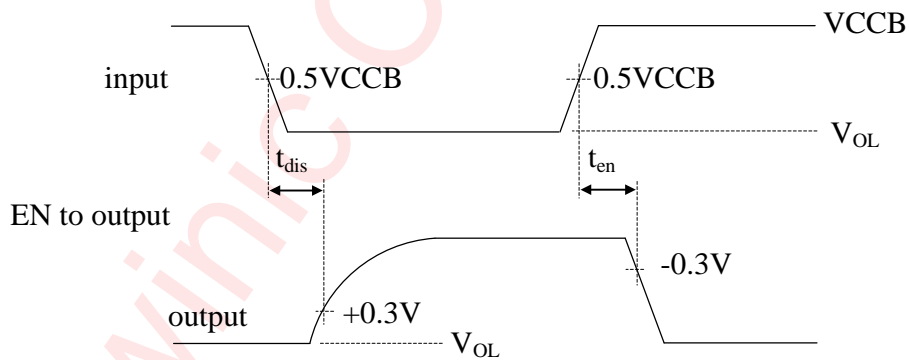
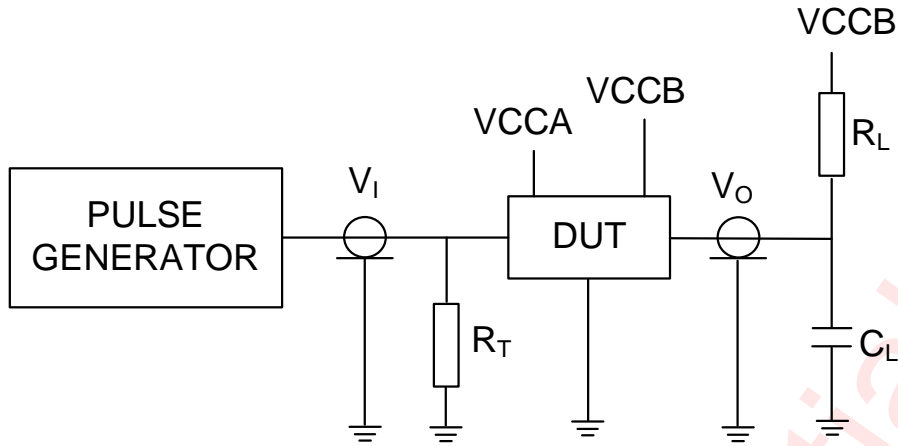


Figure 7 enable and disable times



R_L = load resister; 1.35k Ω on port A and port B.

C_L = load capacitance; 50pF.

R_T = termination resistance should be equal to Z_O of pulse generators.

Figure 8 test circuits for open-drain outputs

Typical Characteristics

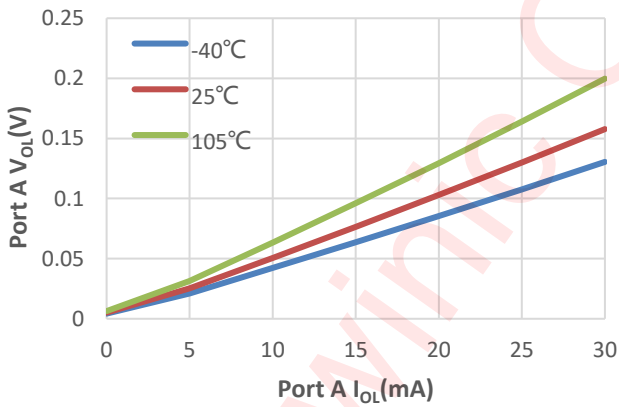


Figure 9 Port A V_{OL} VS I_{OL}

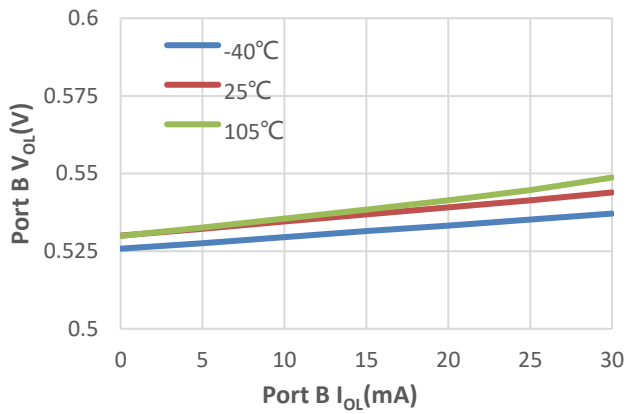


Figure 10 Port B V_{OL} VS I_{OL}

Detailed Functional Description

The AW9617 enables I²C-bus or SMBus translation down to VCCA as low as 0.8V without degradation of system performance. The AW9617 contains two bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage (as low as 0.8V) and the high voltage (as high as 5.5V) I²C-bus or SMBus. All inputs and I/Os are overvoltage tolerant to 5.5V even when the device is unpowered (VCCB and/or VCCA=0V). The AW9617 includes a power-up circuit that keeps the output drivers turned off until VCCB is above 2.2V and until after the internal reference circuits have settled ~400us, and the VCCA is above 0.8V. VCCB and VCCA can be applied in any sequence at power-up. After power-up and with the enable (EN) HIGH, a LOW level on port A (below 0.3VCCA) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to about 0.55V. When port A rises above 0.3VCCA, the port B pull-down driver is turned off and the external pull-up resistor pulls the pin HIGH. When port B falls first and goes below 0.4V, the port A driver is turned on and port A pulls down to ~0V. The port A pull-down is not enabled unless the port B voltage goes below 0.4V. If the port B low voltage goes below 0.4V, the port B pull-down driver is enabled and port B will only be able to rise to 0.55V until port A rises above 0.3VCCA, then port B will continue to rise being pulled up by the external pull-up resistor. The VCCA is only used to provide the 0.35VCCA reference to the port A input comparators and for the power good detect circuit. The AW9617 includes a VCCA overvoltage disable that turns the channel off if $0.4 \times VCCA + 0.8V > VCCB$. The AW9617 logic and all I/Os are powered by the VCCB pin.

Enable

The EN pin is active HIGH with thresholds referenced to VCCB and an internal pull-up to VCCB that maintains the device active unless the user selects to disable the repeater to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I²C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I²C-bus parts being enabled. The enable does not switch the internal reference circuits so the ~400us delay is only seen when VCCB comes up.

The enable pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

I²C-bus systems

As with the standard I²C-bus system, pull-up resistors are required to provide the logic HIGH levels on the buffered bus (standard open-collector configuration of the I²C-bus). The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part designed to work with Standard mode, Fast-mode and Fast-mode Plus I²C-bus devices in addition to SMBus devices. Standard mode and Fast-mode I²C-bus devices only specify 3mA output drive; this limits the termination current to 3mA in a generic I²C-bus system where Standard-mode devices, Fast-mode devices and multiple masters are possible. When only Fast-mode Plus devices are used with 30mA at 5V drive strength, then lower value pull-up resistors can be used. The B-side RC should not be less than 67.5ns because shorter RCs increase the turnaround bounce when the B-side transitions from being externally driven to pulled down by its offset buffer.

Application Information

The AW9617 is 5.5V tolerant, so it does not require any additional circuitry to translate between 0.8V to 5.5V bus voltages and 2.2V to 5.5V bus voltages.

When port A of the AW9617 is pulled LOW by a driver on the I²C-bus, a comparator detects the falling edge when it goes below $0.3V_{CCA}$ and causes the internal driver on port B to turn on, causing port B to pull down to about 0.5V. When port B of the AW9617 falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on port A to turn on and pull the port A pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 11 and Figure 12. If the bus master in Figure 13 were to write to the slave through the AW9617, waveforms shown in Figure 11 would be observed on the A bus. This looks like a normal I²C-bus transmission except that the HIGH level may be as low as 0.8V, and the turn on and turn off of the acknowledge signals are slightly delayed.

The internal comparator requires that $0.4V_{CCA}$ be less than or equal to $V_{CCB}-0.8V$ for the device to operate. Since A port is 5.5V tolerant, the V_{CCA} can be lowered to support device spectrum while still supporting 5 V signals on the A port.

On the B bus side of the AW9617, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the AW9617. After the eighth clock pulse, the data line will be pulled to the V_{OL} of the slave device which is very close to ground in this example. At the end of the acknowledge, the level rises only to the LOW level set by the driver in the AW9617 for a short delay while the A bus side rises above $0.3V_{CCA}$ then it continues HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the B bus side at the input of the AW9617 (V_{IL}) be at or below 0.4V to be recognized by the AW9617 and then transmitted to the A bus side.

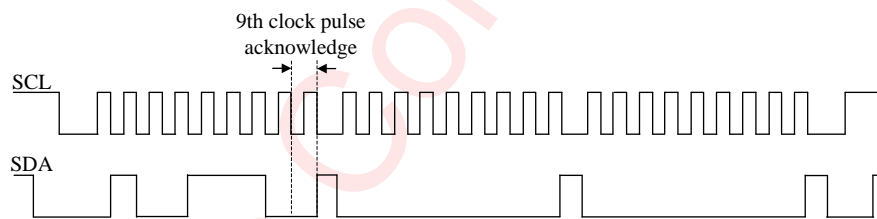


Figure 11 Bus A (0.8 V to 5.5 V bus) waveform

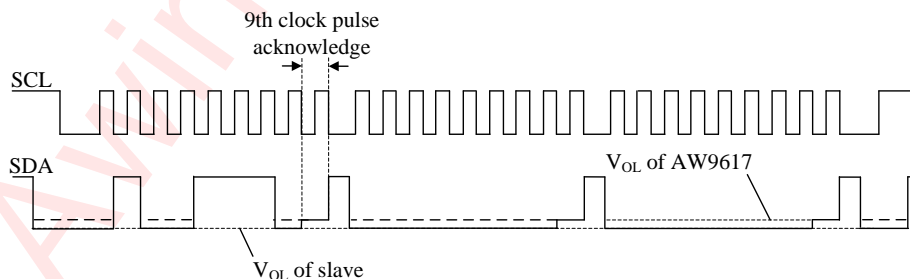


Figure 12 Bus B (2.2 V to 5.5 V) waveform

Standard Application

A typical application of AW9617. In this example, the system master is running on a 3.3V I²C-bus while the slave is connected to a 1.2V bus. Both buses run at 1000kHz. Master devices can be placed on either bus.

The AW9617 is 5.5V tolerant, so it does not require any additional circuitry to translate between 0.8V to 5.5V bus voltages and 2.2V to 5.5V bus voltages.

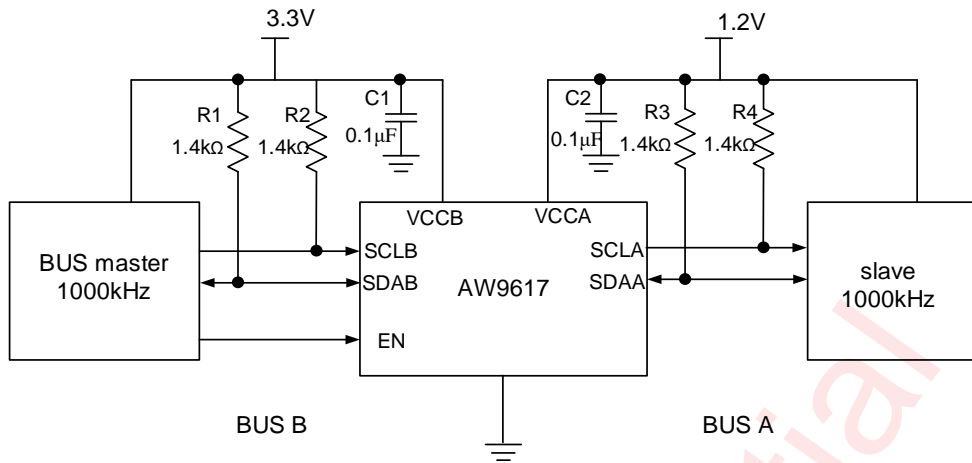


Figure 13 AW9617 Typical Application

Star Application

Multiple AW9617s A sides can be connected in a star configuration, allowing all nodes to communicate with each other.

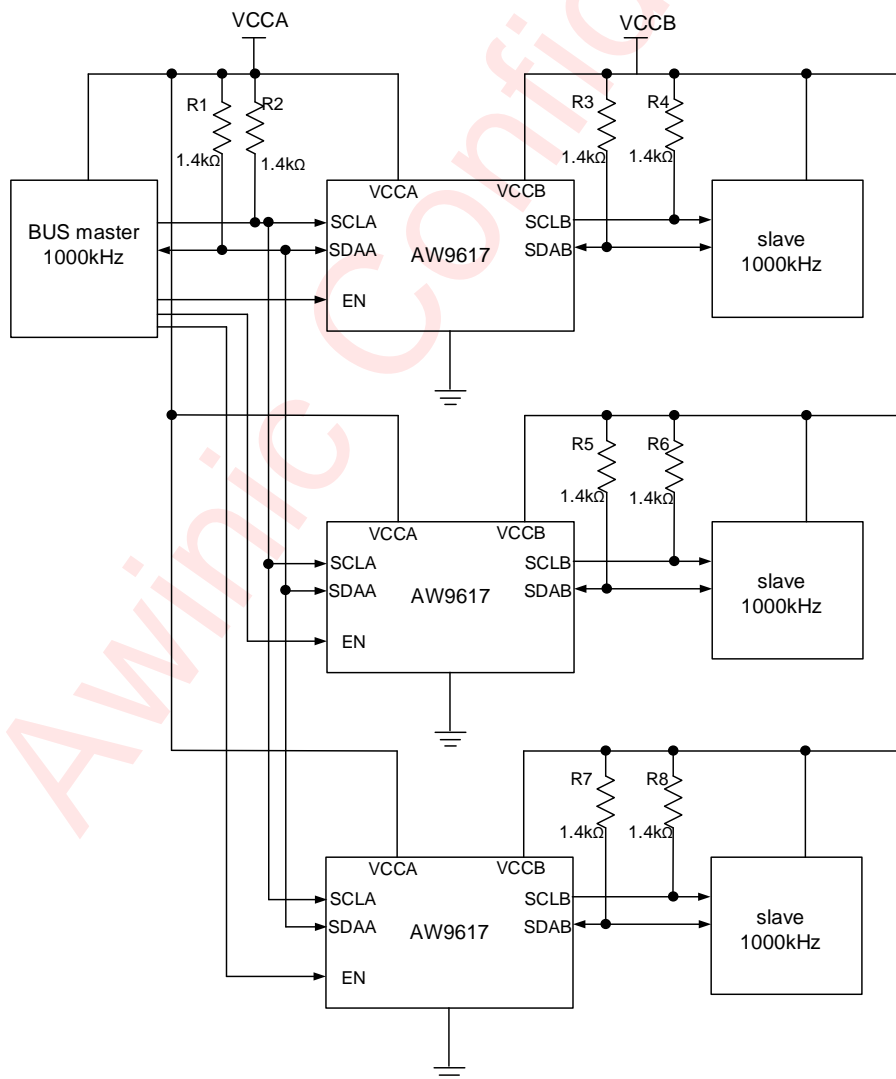


Figure 14 AW9617 Typical Star Application

Series Application

Multiple AW9617s can be connected in series as long as the A side is connected to the B side. I²C bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

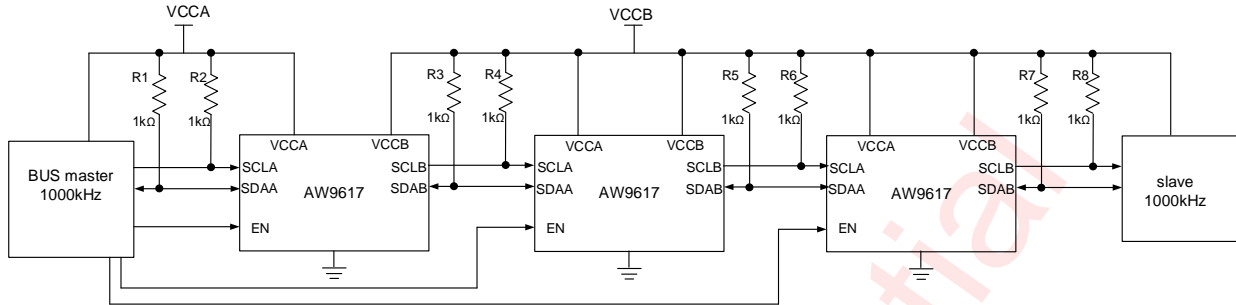


Figure 15 AW9617 Typical Series Application

Power Supply Recommendations

For VCCA, an 0.8V to 5.5V power supply is required. For VCCB, a 2.2V to 5.5V power supply is required. VCCB should always be higher than $0.4 \times V_{CCA} + 0.8V$.

Standard decoupling capacitors are recommended. These capacitors typically range from 0.1μF to 1μF, but the ideal capacitance depends on the amount of noise from the power supply.

PCB Layout Consideration

The recommended decoupling capacitors should be placed as close to the VCCA and VCCB pins of the AW9617 as possible.

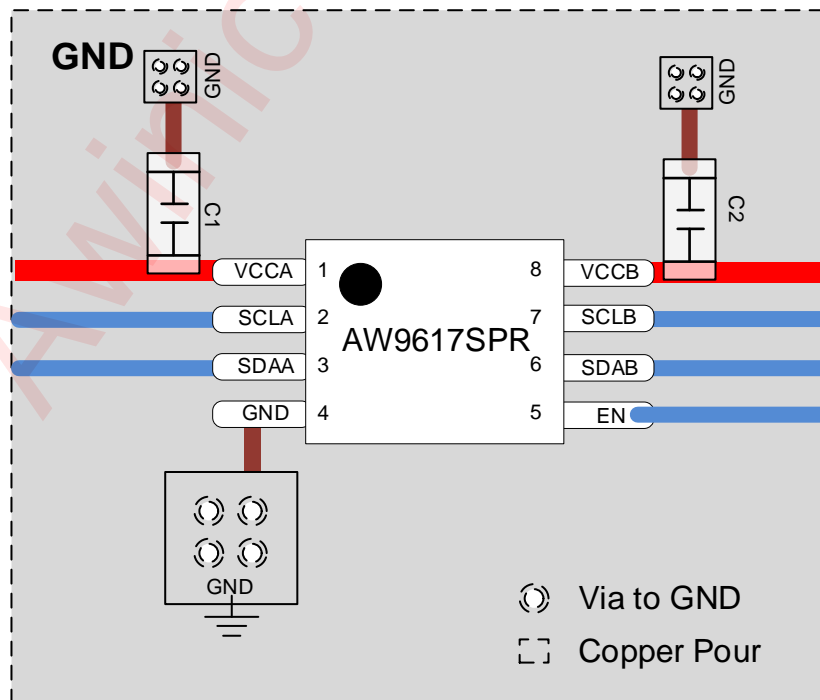
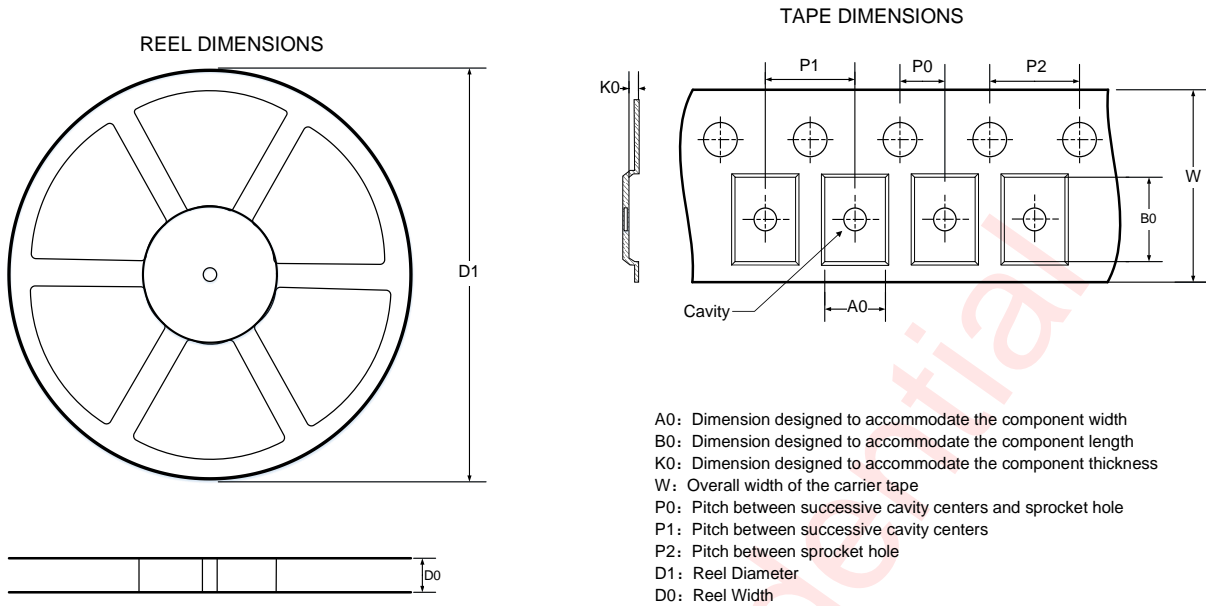
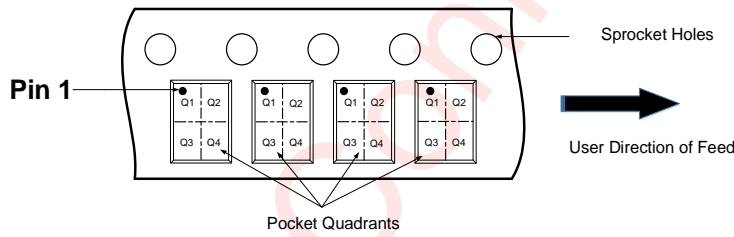


Figure 16 AW9617 Layout Example

Tape And Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



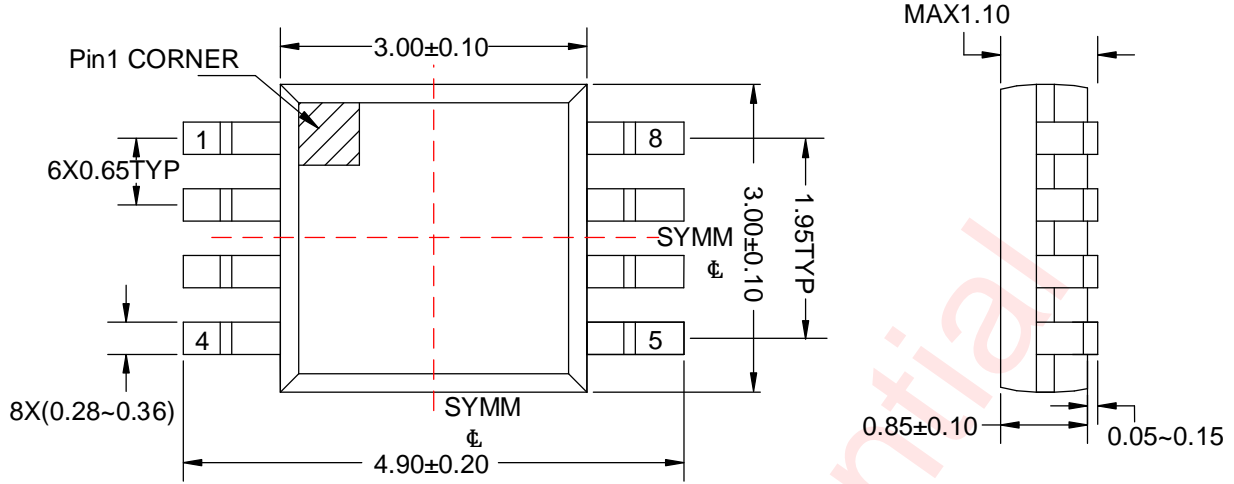
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	5.4	3.4	1.4	2	8	4	12	Q1

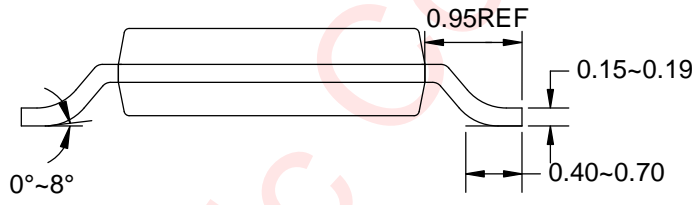
All dimensions are nominal

Package Description



Top View

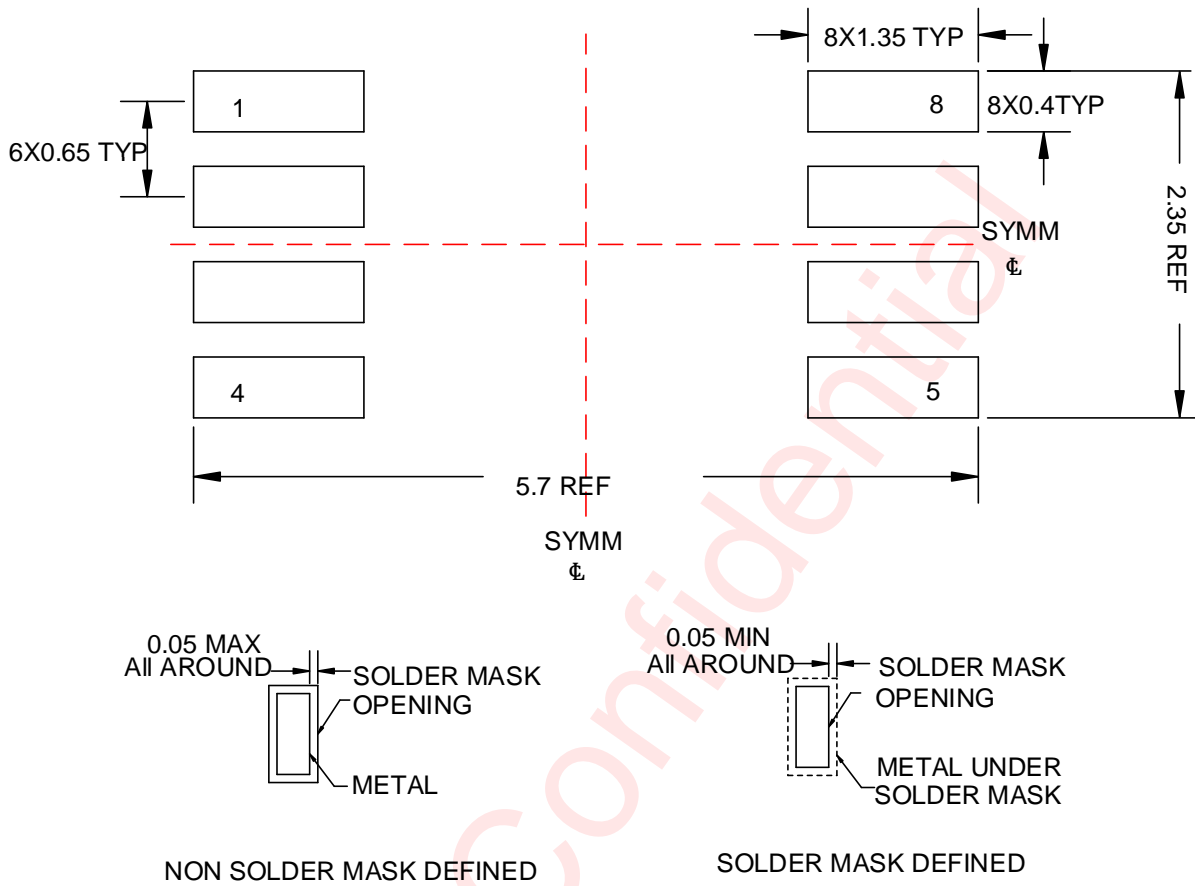
Side View



Side View

Unit: mm

Land Pattern Data



Unit: mm

Revision History

Version	Date	Change Record
V1.0	May. 2024	Officially released
V1.1	Jun. 2024	Update the table of Absolute Maximum Ratings
V1.2	Aug. 2025	Update I _{CCA} test condition

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