DPDT USB Switch With Over Voltage Protection

Features

- USB 2.0 Hi-speed DPDT switch
- Typical -3dB bandwidth: 1GHz
- Over voltage protection: 5.1V typical
- 24V DC protection on D+ and D- Ports
- +35V surge protection on D+ and D-
- Supply voltage range: 2.7V to 5.5V
- 5.9Ω switch on-resistance typical
- C_{ON}: 6pF typical
- I_{CC}: 33μA typical
- QFN 2.0mm X1.5mm X0.55mm-10L package

Applications

- Smart phones
- Tablets
- USB Type-C
- PC/Notebook

General Description

The AW35752G is a Hi-Speed USB 2.0(480Mbps) DPDT(Double Pole Double Throw) switch with integrated protection for USB D+ and D-, it can be configured as a dual 1:2 or 2:1 switch.

The AW35752G protection on the D+/D- pins can tolerate up to 24V DC, when D+ or D- voltage is greater than the OVP(Over-Voltage Protection) threshold, the switch will be automatically shutoff to protect downstream devices.

The device operates over a 2.7V to 5.5V supply range with independent control bits for each switch pair and an on/off enable pin for shutdown mode.

The AW35752G is available in a QFN 2.0mm X1.5mm X0.55mm-10L package.

Typical Application Circuit

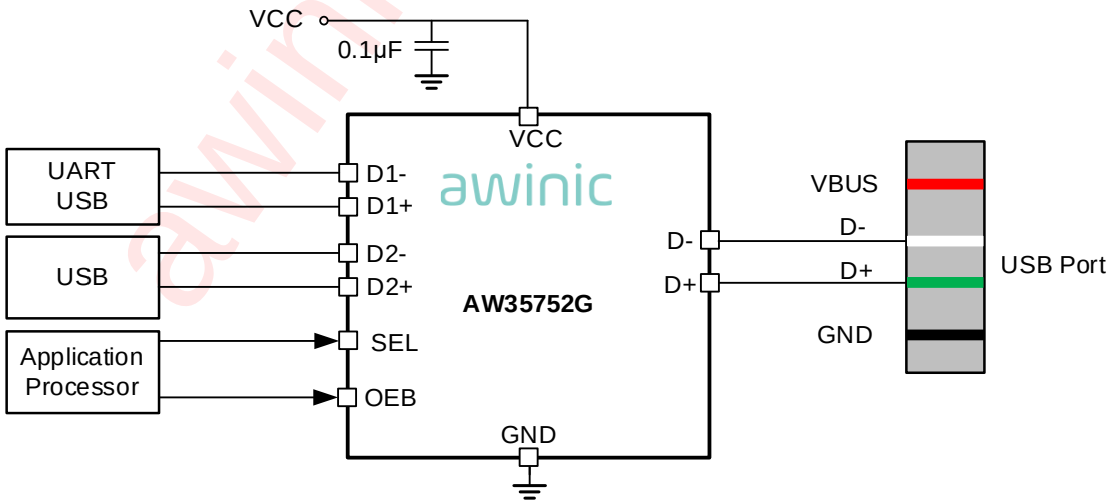

Figure 1 Typical Application Circuit of AW35752G

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Pin Configuration And Top Mark

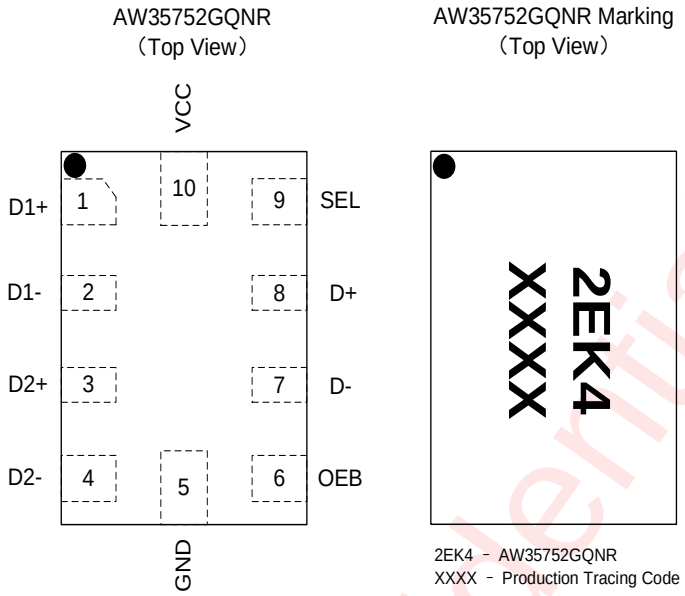


Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	D1+	Multiplexed high speed data port1, differential +
2	D1-	Multiplexed high speed data port1, differential -
3	D2+	Multiplexed high speed data port2, differential +
4	D2-	Multiplexed high speed data port2, differential -
5	GND	Ground
6	OEB	Output enable, active low
7	D-	Common high speed data port, differential -
8	D+	Common high speed data port, differential +
9	SEL	Switch select(logic Low = D+/- to D1+/- ,logic High = D+/- to D2+/-)
10	VCC	Supply voltage

Pin Functions

OEB	SEL	D- CONNECTION	D+ CONNECTION
H	X	High-Z	High-Z
L	L	D- to D1-	D+ to D1+
L	H	D- to D2-	D+ to D2+

Functional Block Diagram

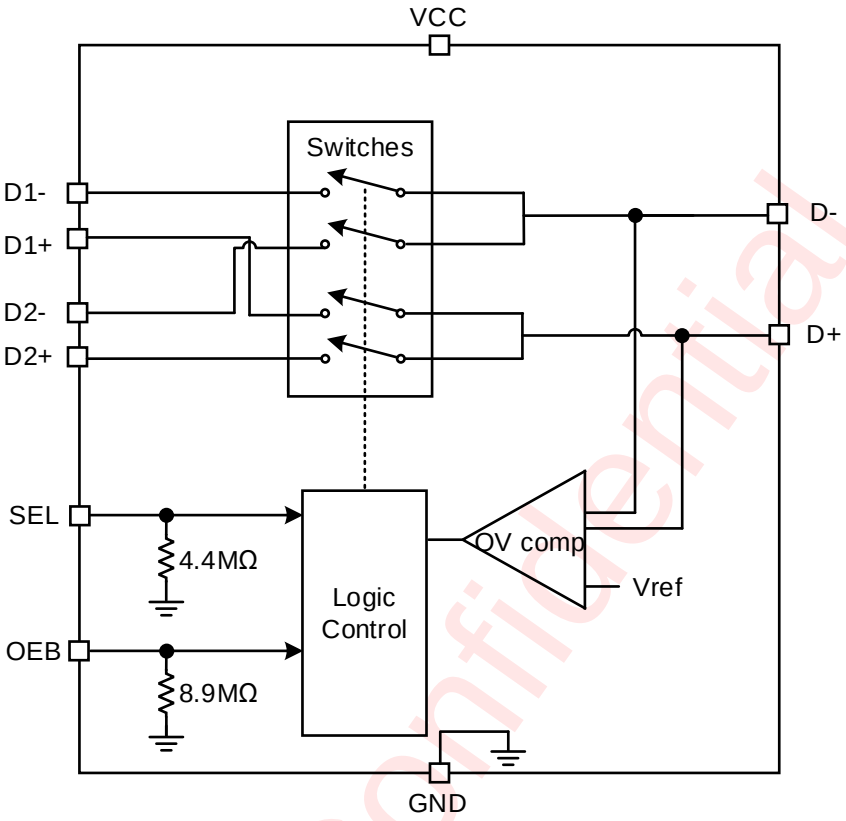


Figure 3 Functional Block Diagram

Typical Application Circuits

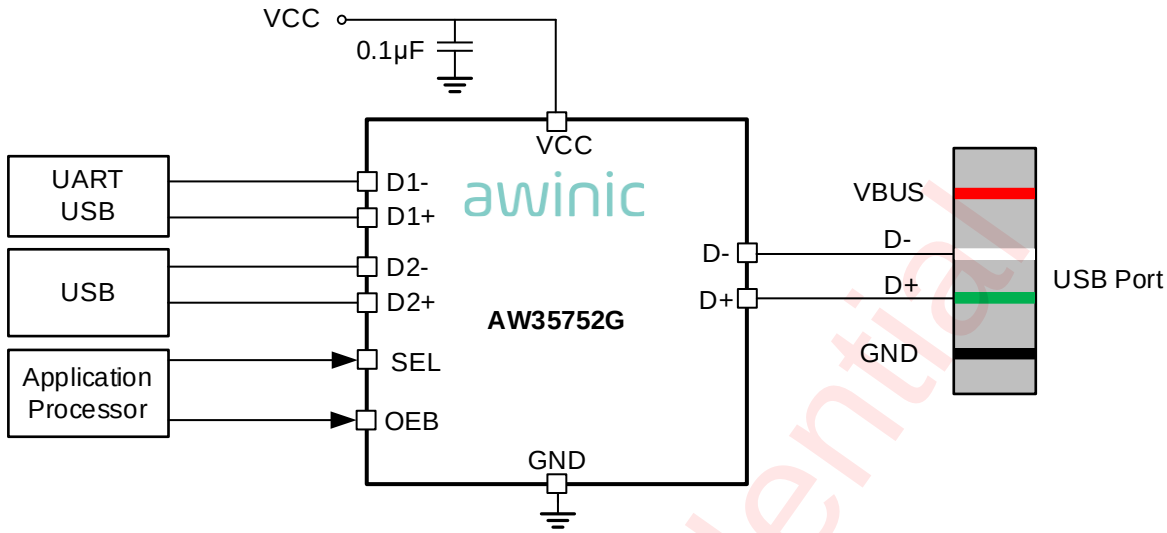


Figure 4 Typical Application Circuit of AW35752G

Notice for Typical Application Circuits:

1. The AW35752G has internal 4.4-MΩ and 8.9-MΩ pull down resistors on SEL and OEB, so no external resistors are required on the logic pins.
2. Internal pull-down resistor on SEL pins ensures the D1+ and D1- channels are selected by default.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW35752GQNR	-40°C~105°C	QFN 2.0mm X1.5mm X0.55mm -10L	2EK4	MSL1	ROHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage range VCC		-0.3V to 6V
Input/Output DC voltage(D+, D-)		-0.3V to 24V
Input/Output DC voltage(D1+, D1-, D2+, D2-)		-0.3V to 6V
Input voltage range	SEL, OEB	-0.3V to 6V
Junction-to-ambient thermal resistance θ_{JA}		132°C/W
Maximum operating junction temperature T_{JMAX}		150°C
Operating free-air temperature range		-40°C to 105°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD		
Human Body Model (All pins, per JEDEC JS-001) (NOTE2)		±4kV
Charged Device Model (All pins, per JEDEC JS-002) (NOTE3)		±1.5kV
Latch-Up		
Test condition: JEDEC 78E		±200mA

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.*

NOTE3: Test method: ESDA/JEDEC JS-002-2018.

Recommended Operating Conditions

PARAMETERS		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	5.5	V
$V_{I/O}$	Analog input/output voltage($D_{\pm}$)	0	20	V
	Analog input/output voltage($Dn_{\pm}$)	0	3.6	V
V_I	Digital input voltage(SEL, OEB)	0	5.5	V
T_A	Operating free-air temperature T_A	-40	105	°C

Electrical Characteristics

V_{CC}=3.3V T_A = 25°C for typical values (unless otherwise noted).

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	5.5	V
I_{CC}	Active supply current	OEB=0V, SEL=0V, 0V<$V_{D\pm}$<3.6V		33	50	μA
I_{CC_PD}	Standby supply current	OEB=V_{CC} SEL=0V		0.1		μA
DC Characteristics						
R_{ON}	On-state resistance	$V_{I/O}$=0.4V, I_{SINK}=8mA		5.9		Ω
ΔR_{ON}	On-state resistance match between channels	$V_{I/O}$=0.4V, I_{SINK}=8mA		0.1		Ω
$R_{ON(FLAT)}$	ON-state resistance flatness	$V_{I/O}$=0V to 0.4V, I_{SINK}=8mA		0.1		Ω
I_{OFF}	I/O pin OFF leakage current on D+/D-	$V_{D\pm}$=0V or 3.6V $V_{D1\pm}$ or $V_{D2\pm}$= 3.6V or 0V		0.4	10	μA
		$V_{D\pm}$=0V or 24V $V_{D1\pm}$ or $V_{D2\pm}$= 0V		356	500	μA
I_{ON}	ON leakage current on D+/D-	$V_{D\pm}$= 0V or 3.6V $V_{D1\pm}$ and $V_{D2\pm}$=high-Z		0.4	10	μA
Digital Characteristics						
V_{IH}	Input logic high	SEL, OEB	0.96			V
V_{IL}	Input logic low	SEL, OEB			0.4	V
R_{OEB}	OEB pull-down resistor			8.9		MΩ
R_{SEL}	SEL pull-down resistor			4.4		MΩ
Protection						
V_{OVP_TH}	OVP threshold	D+/D- rising	4.8	5.1	5.4	V
V_{OVP_HYST}	OVP threshold hysteresis			270		mV
V_{CLAMP_V}	Clamping voltage on $D_{1\pm}$ and $D_{2\pm}$ pins during surge	8/20μs surge test, OEB=0V, R_L=open			9	V
t_{CLAMP}	Clamp time during OVP	8/20μs surge test, OEB=0V, R_L=open		150		ns

Electrical Characteristics (Continued)

V_{CC}=3.3V T_A = 25°C for typical values (unless otherwise noted).

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Dynamic Characteristics						
C_{ON}	IO pins ON capacitance	$V_{D±}$=0V or 3.3V, f=240MHz, switch ON		6		pF
O_{ISO}	Differential off isolation	R_L=50Ω, C_L=5pF f=100kHz, switch OFF		-60		dB
		R_L=50Ω, C_L=5pF f=240MHz, switch OFF		-20		dB
X_{TALK}	Channel to channel crosstalk	R_L=50Ω, C_L=5pF f=100 kHz, switch ON		-60		dB
BW	-3dB bandwidth	R_L=50Ω, switch ON		1.0		GHz
t_{switch}	Switching time between channels (SEL to output)	$V_{D±}$=0.8V, R_L=50Ω, C_L=5pF, V_{CC}=2.7V to 5.5V		1.5	5	μs
t_{on}	Device turn on time (OEB to output)			40		μs
t_{off}	Device turn off time (OEB to output)			55		ns
t_{pd}	Propagation delay	$V_{D±}$=0.4V, R_L=50Ω, C_L=5pF, V_{CC}=2.7V to 5.5V		200		ps

Typical Characteristics

Ambient temperature is 25°C, V_{CC} =3.3V, $V_{D\pm}$=0.4V, unless otherwise noted.

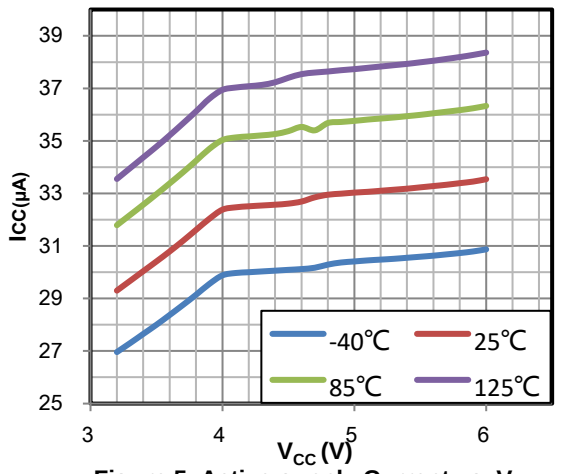


Figure 5 Active supply Current vs. V_{CC}

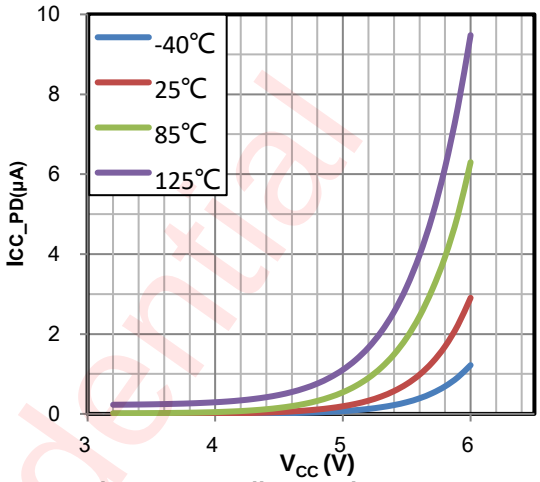


Figure 6 Standby supply Current vs. V_{CC}

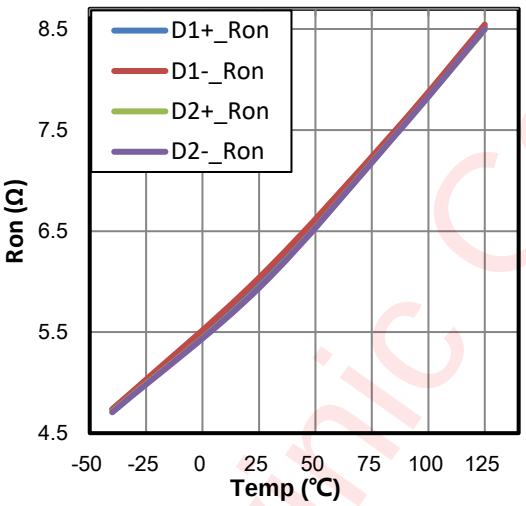


Figure 7 R_{ON} vs. Temperature

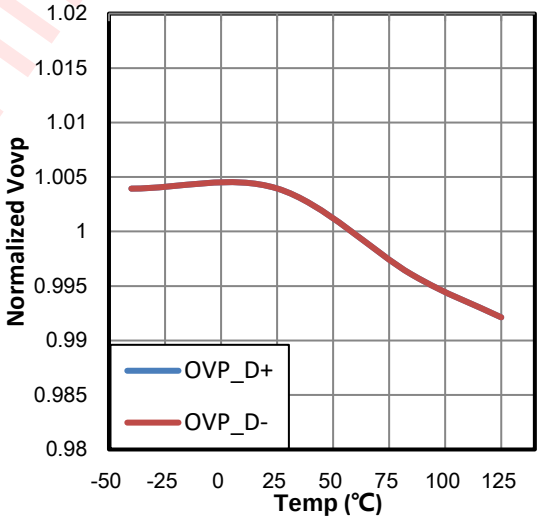


Figure 8 OVP Voltage vs. Temperature

Figure 9 BW of D+ to D1+

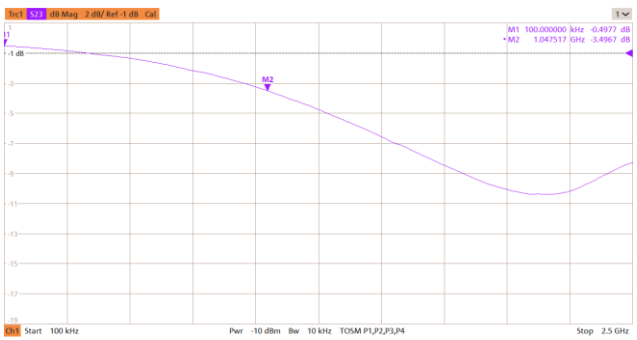


Figure 10 BW of D- to D1-

Typical Characteristics (Continued)

Ambient temperature is 25°C, V_{CC} =3.3V, $V_{D\pm}$=0.4V, unless otherwise noted.

Figure 11 BW of D+ to D2+

Figure 12 BW of D- to D2-

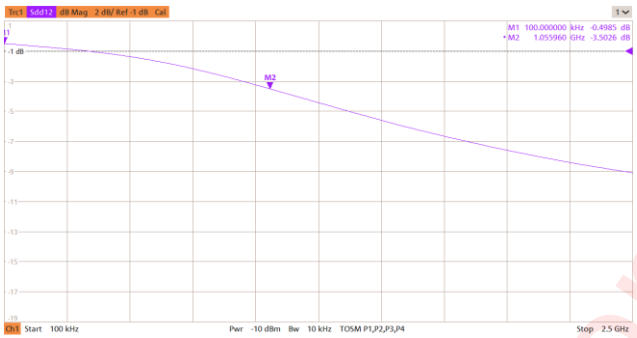


Figure 13 BW of D± to D1±

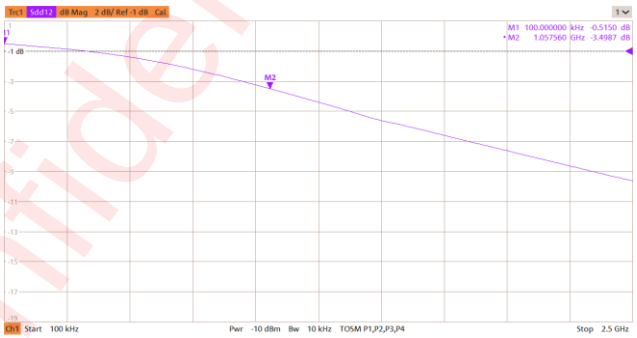


Figure 14 BW of D± to D2±

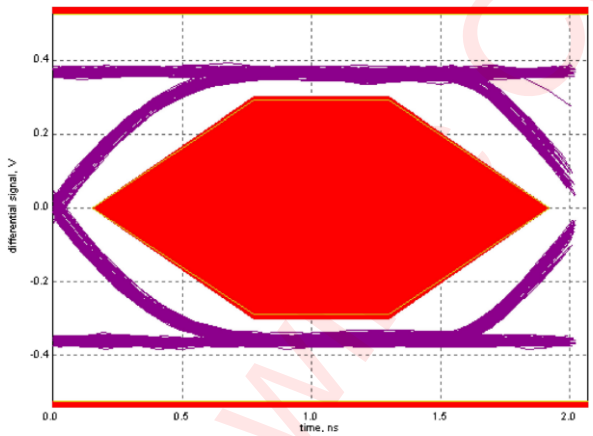


Figure 15 USB 2.0 High Speed Eye Diagram of D± to D1±

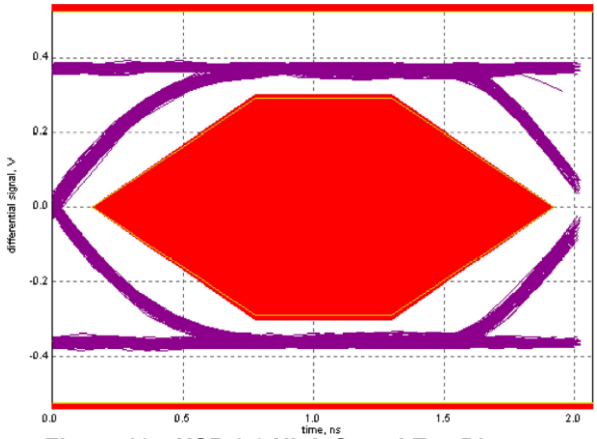


Figure 16 USB 2.0 High Speed Eye Diagram of D± to D2±

Timing Diagram

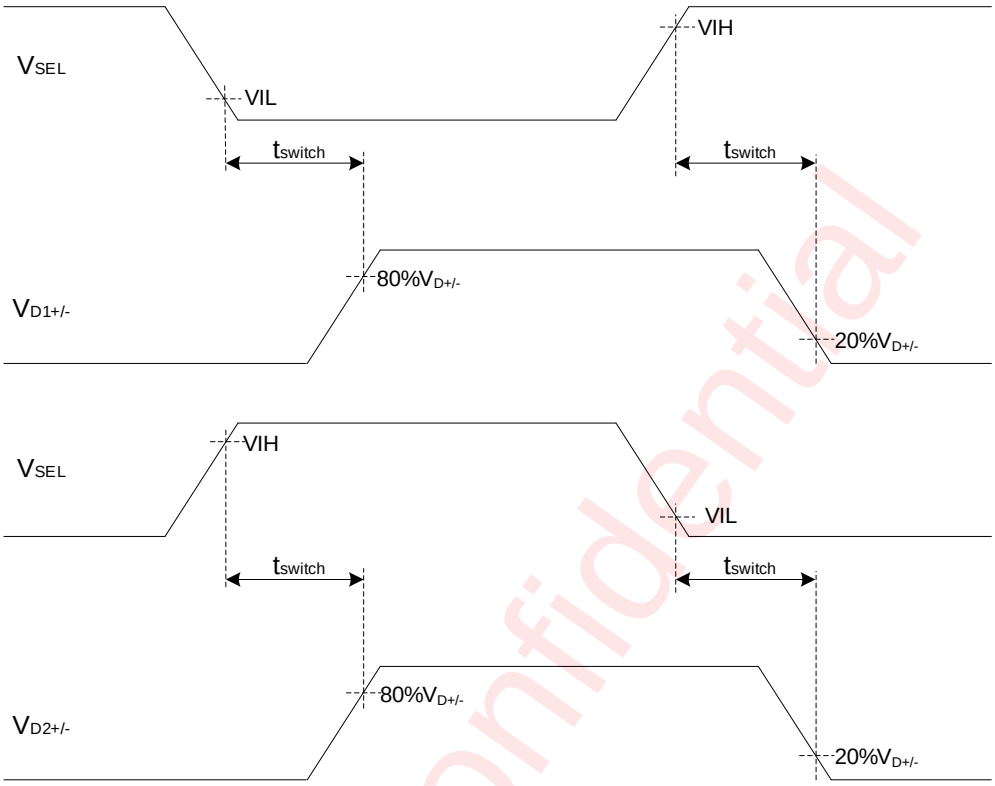


Figure 17 Switching Time Between Channels

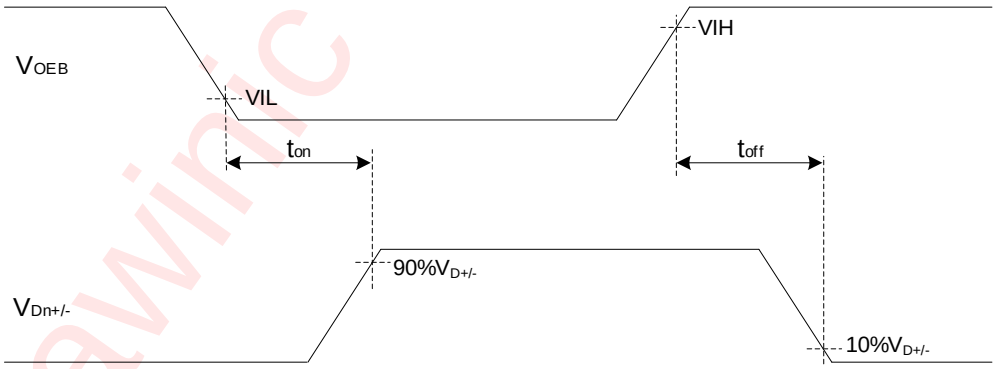


Figure 18 Device Turn On Time

Timing Diagram (Continued)

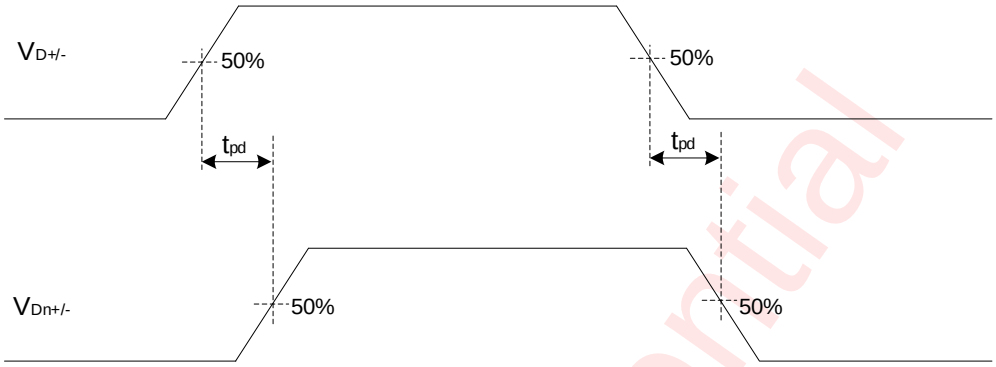


Figure 19 Propagation delay

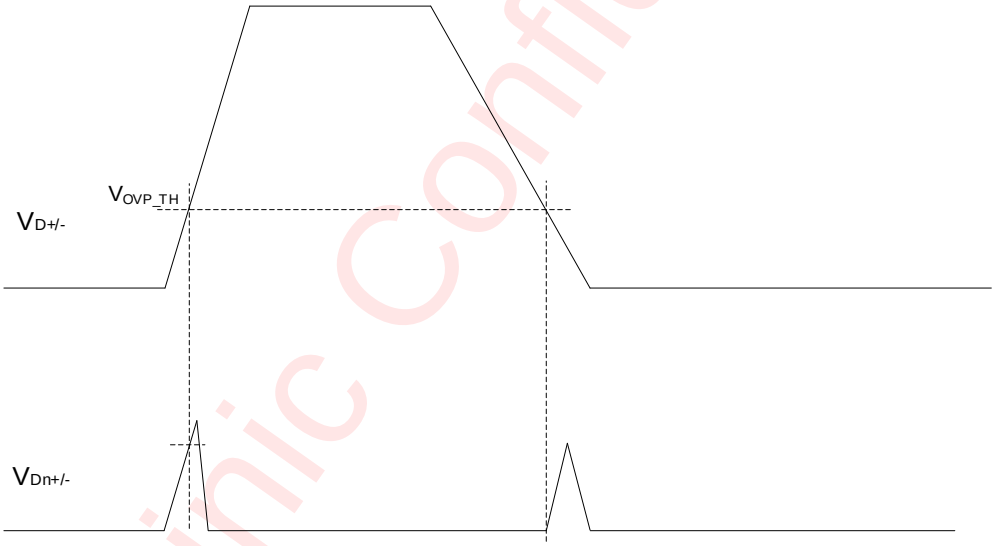


Figure 20 Overvoltage Protection

Application Information

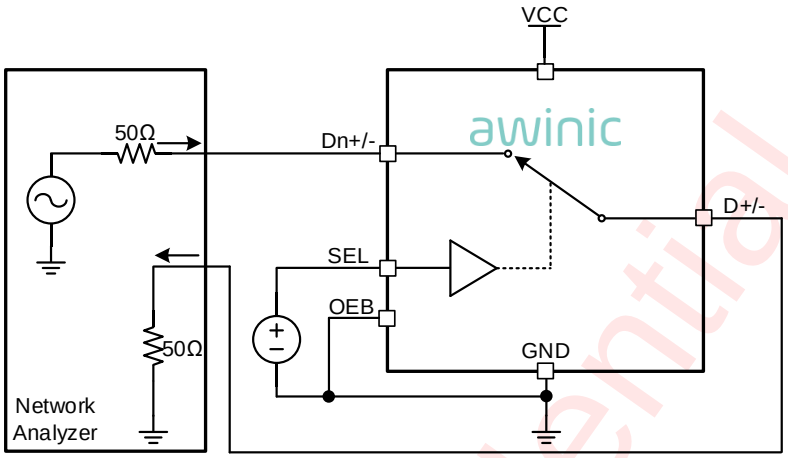


Figure 21 BW and Insertion Loss

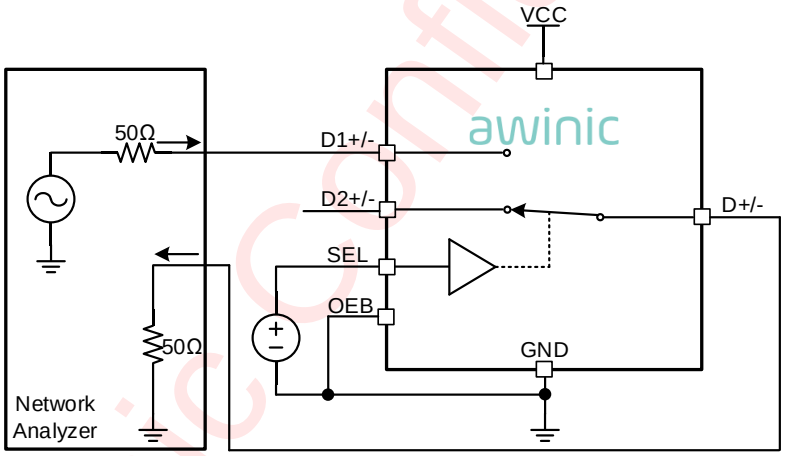


Figure 22 OFF Isolation

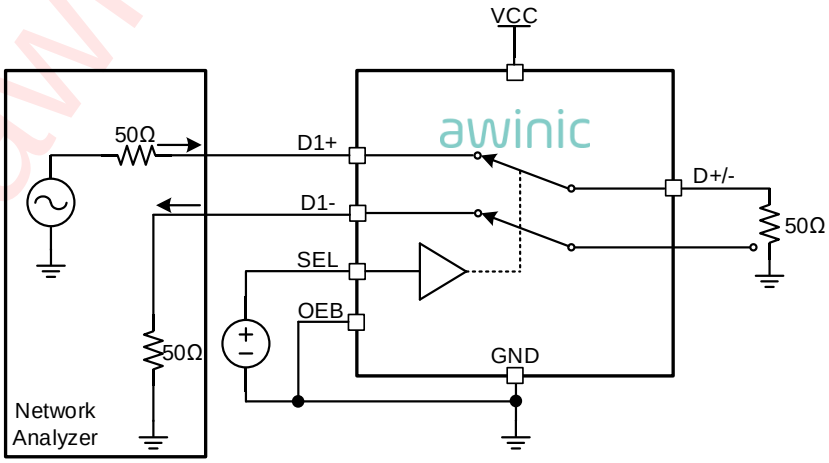


Figure 23 Cross Talk

Detailed Functional Description

The AW35752G is bidirectional low-power dual port, high-speed, USB2.0 analog switch with integrated protection for USB D+ and D-, it can be configured as a dual 1:2 or 2:1 switch. The AW35752G will protect D+ and D- pins when stressed with voltages up to 24V. The device can pass signals with bandwidth 1.0GHz to maintain signal integrity and eye compliance.

Powered-off Protection

When the AW35752G is powered off the I/Os of the device remain in a high-Z state. The crosstalk, off-isolation, and leakage remain within the Electrical Specifications.

Over-Voltage Protection

AW35752G is designed to protect the system from damage. Over-voltage event happens when voltage on D+/D- exceeds 5.1V(typ.), and device will activate OVP to disconnect the switches.

High Impedance Mode

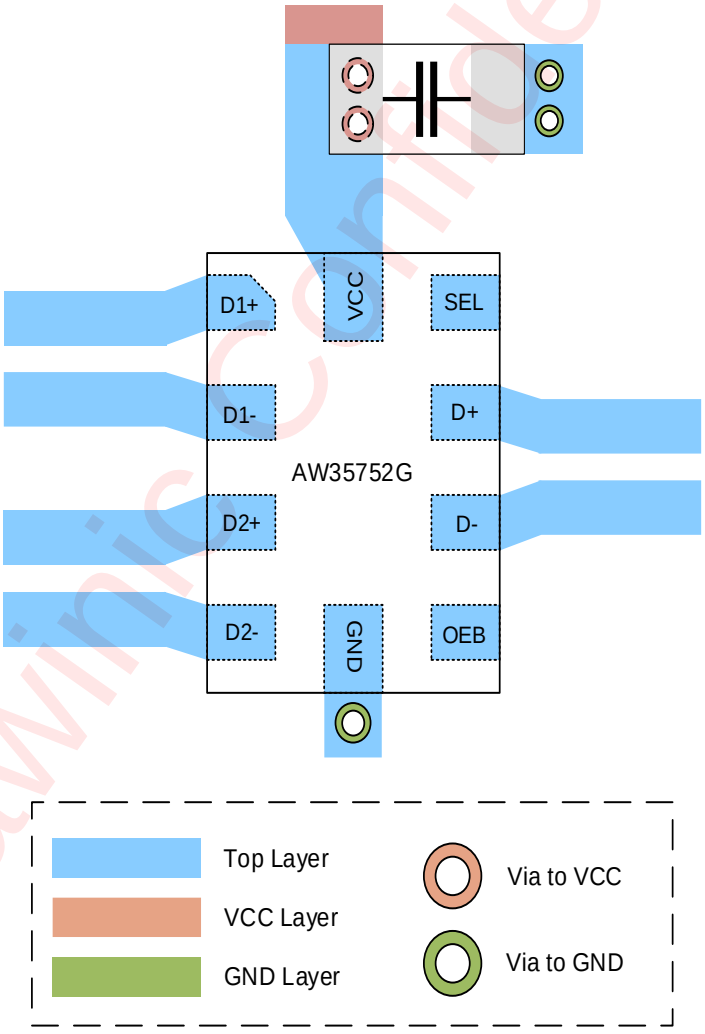
When OEB is logic high, the AW35752G is in high impedance mode, all the signal paths are in Hi-Z state.

OEB	SEL	D- Connection	D+ Connection
H	X	High-Z	High-Z
L	L	D- to D1-	D+ to D1+
L	H	D- to D2-	D+ to D2+

PCB Layout Consideration

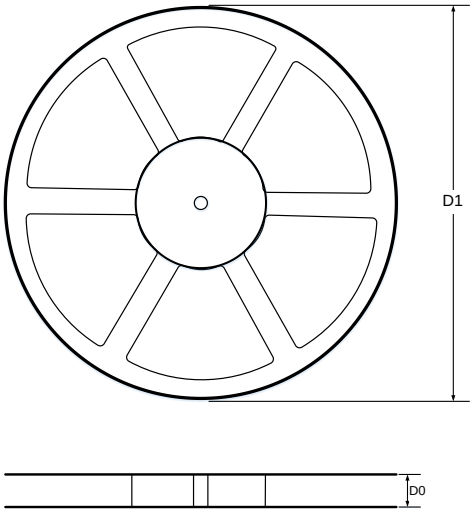
To obtain the optimal performance of AW35752G, PCB layout should be considered carefully. Here are some guidelines:

1. Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass capacitors near the D+/D- traces.
2. The differential characteristic impedance of D+ and D- traces is suggested to be 90Ω, and it's better to shield D+ and D- traces by ground planes.
3. Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes.
4. Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
5. Avoid stubs on the high-speed USB signals because they cause signal reflections.
6. Route all high-speed USB signal traces over continuous GND planes, with no interruptions.

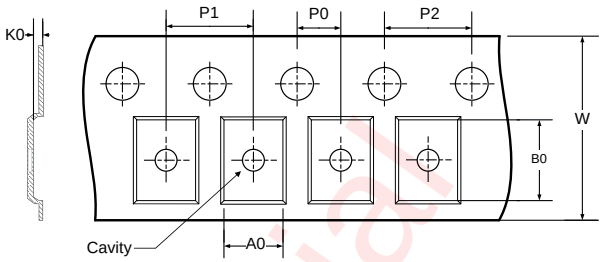


Tape And Reel Information

REEL DIMENSIONS

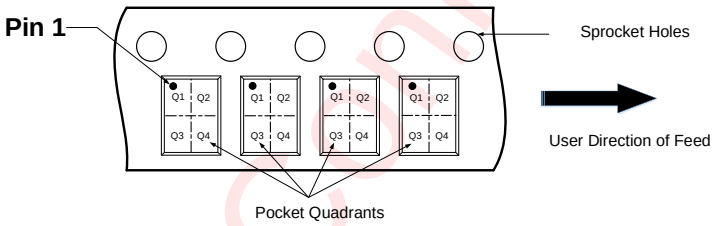


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



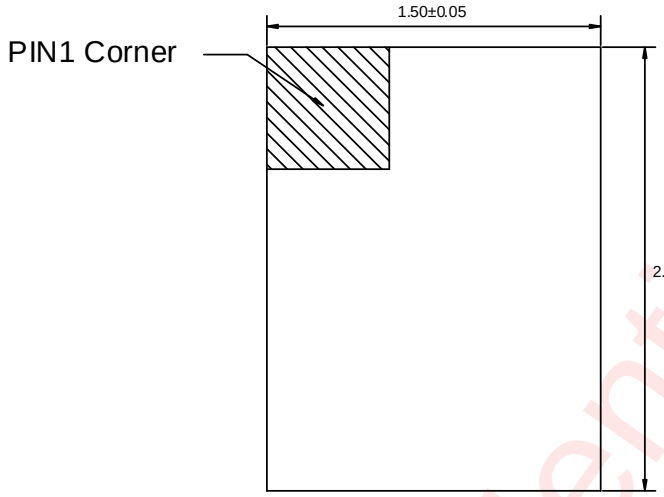
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

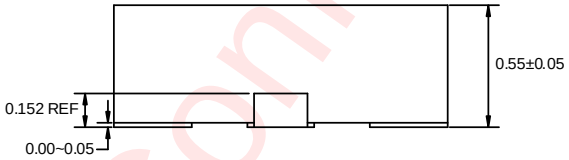
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.75	2.3	0.75	2	4	4	8	Q1

All dimensions are nominal

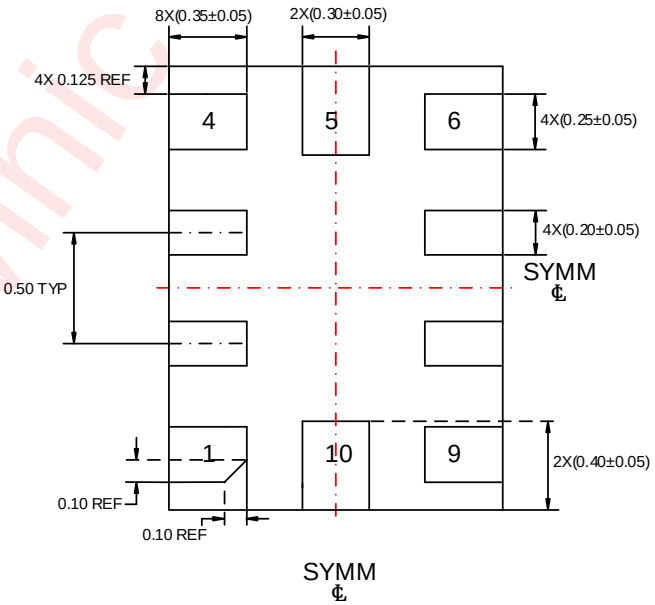
Package Description



Top View



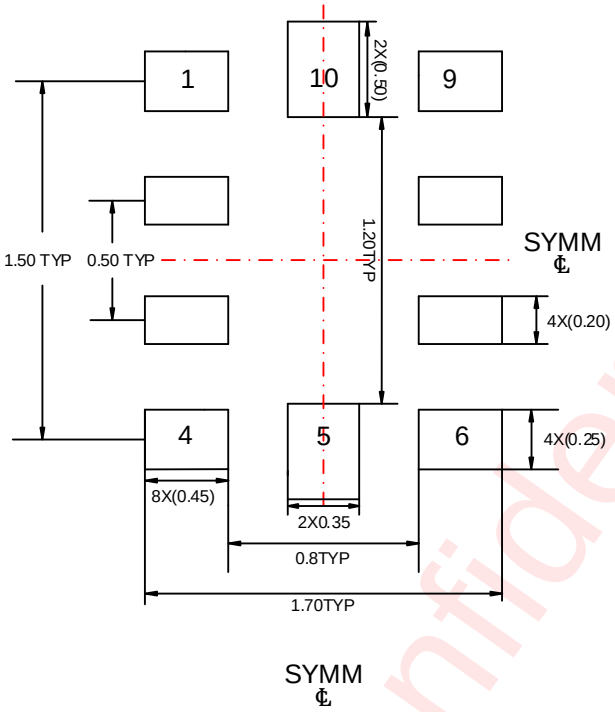
Side View

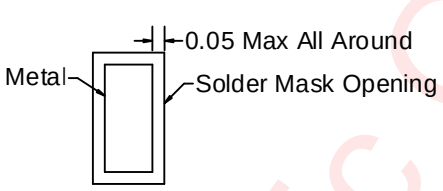


Bottom View

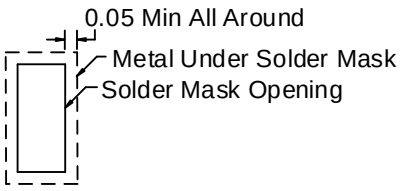
Unit: mm

Land Pattern Data





Non-solder Mask Defined



Solder Mask Defined

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Jun. 2023	Officially released

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