AW9511 Hot Swappable I2C-bus and SMBus Buffer

Features

- Supports bidirectional data transfer of I2C bus signals
- Operating power supply voltage range: 2.3V to 5.5V
- Compatible with I2C-bus Standard-mode, I2C-bus Fast-mode, and SMBus standards
- 0Hz to 400KHz clock frequency
- 1V pre-charge on all SDA and SCL lines prevents corruption during live insertion
- Built-in ΔV/Δt rise time accelerators(RTA) on all SDA and SCL lines (0.6V threshold), Requires the bus pull-up voltage and supply voltage (VCC) to be the same
- Supports clock stretching and multiple master arbitration/synchronization
- Active HIGH ENABLE input
- Active HIGH READY open-drain output
- High-impedance SDA and SCL pins for VCC=0V
- Operation temperature range: -40°C~105°C
- MSOP-8L package

Applications

Servers
Enterprise Switching
Telecom switching equipment
Base stations
Industrial automation equipmen

General Description

AW9511 is a hot swappable I2C-bus and SMBus buffer that supports I/O card insertion into a live backplane without corrupting the data and clock lines. Control circuitry prevents the backplane from being connected to the card until a stop command or bus idle occurs on the backplane without bus contention on the card. When the connection is made, the AW9511 provides bidirectional buffering, keeping the backplane and card capacitances isolated. During insertion, the SDA and SCL lines are pre-charged to 1V to minimize the current required to charge the parasitic capacitance of the device.

The AW9511 rise time accelerator circuitry allows the use of weaker DC pull-up currents while still meeting rise time requirements. When the I2C bus is idle, the AW9511 can be put into shutdown mode by setting the ENABLE pin low, reducing power consumption. When ENABLE pin is pulled high, the AW9511 resumes normal operation. It also includes an open drain READY output pin, which indicates that the backplane and card sides are connected together. When READY is high, the SDAIN and SCLIN are connected to SDAOUT and SCLOUT. When the two sides are disconnected, READY is low.

Typical Application Circuit

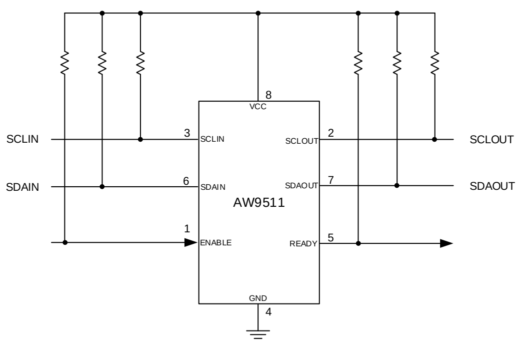
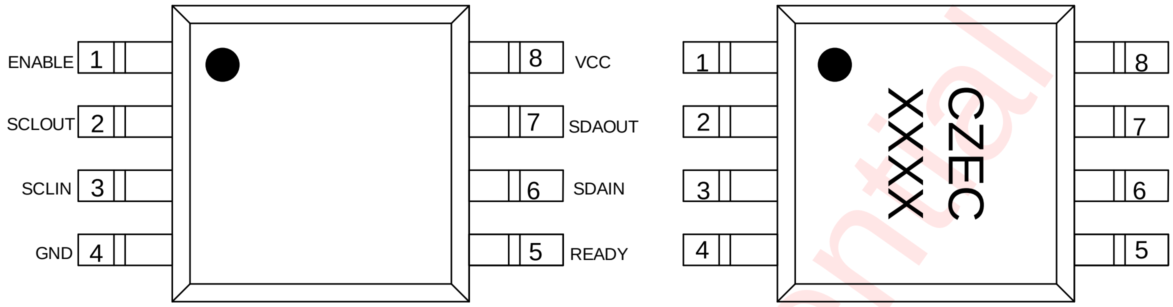


Figure 1 AW9511 Simplified Application Circuit

Pin Configuration And Top Mark

AW9511SPR
（Top view）

AW9511SPR Marking
（Top view）



CZEC - AW9511SPR
XXXX - Production Tracing Code

Figure 2 Pin Configuration and Marking

Pin Definition

NO.	Name	Type	Description
1	ENABLE	Input	Active-high chip enable pin. If ENABLE is low, the chip is in a low current mode. It also disables the rise-time accelerators, disables the bus pre-charge circuitry, drives READY low, isolates SDAIN from SDAOUT and isolates SCLIN from SCLOUT
2	SCLOUT	I/O	Serial clock output to and from the SCL bus on the card
3	SCLIN	I/O	Serial clock input to and from the SCL bus on the backplane
4	GND	-	Supply ground
5	READY	Output	Open-drain output which pulls LOW when SDAIN and SCLIN are disconnected from SDAOUT and SCLOUT, and goes HIGH when the two sides are connected
6	SDAIN	I/O	Serial data input to and from the SDA bus on the backplane
7	SDAOUT	I/O	Serial data output to and from the SDA bus on the card
8	VCC		Supply Power

Functional Block Diagram

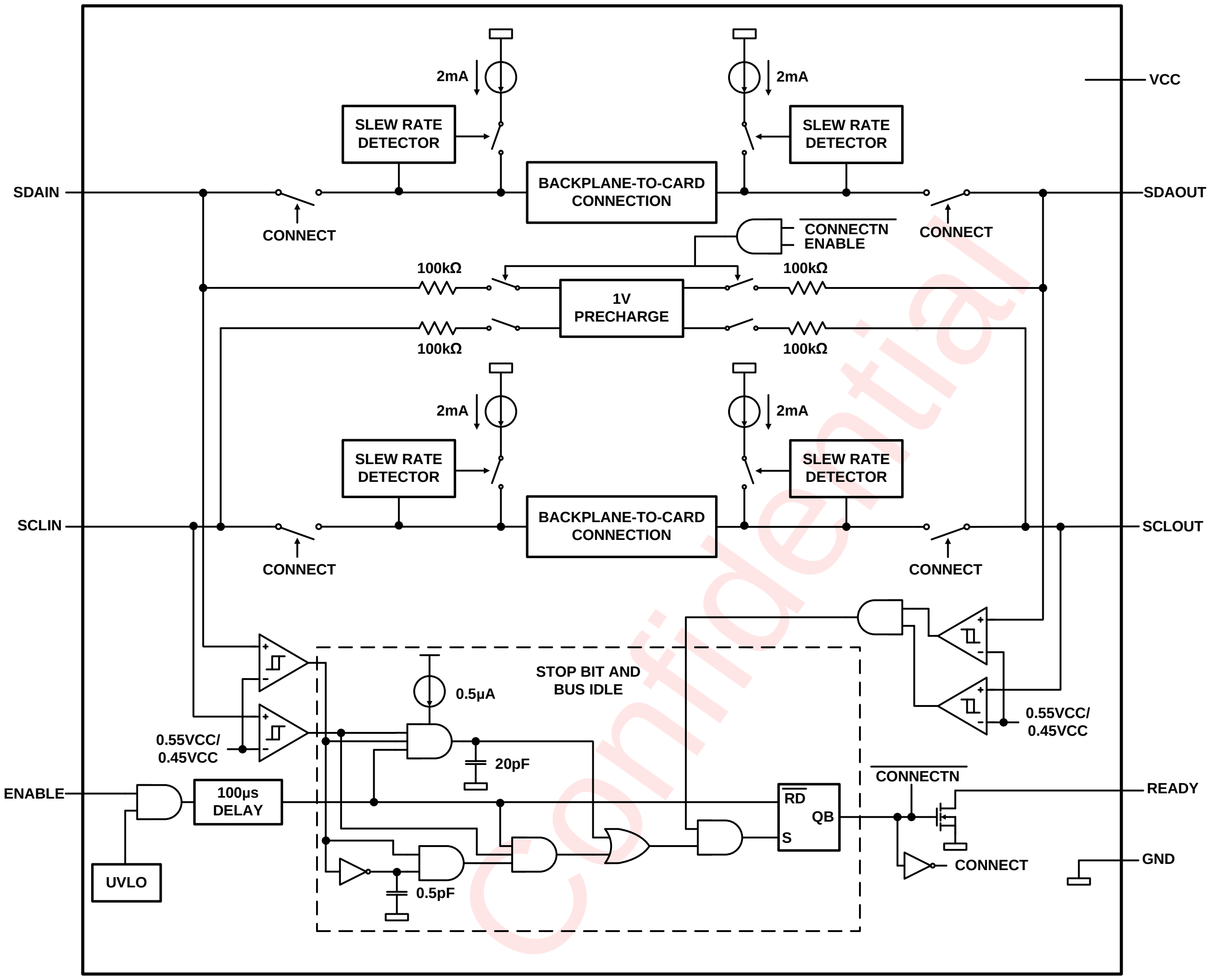


Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW9511SPR	-40°C~105°C	MSOP-8L	CZEC	MSL1	RoHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage, VCC		-0.5V to 7V
Voltage on SDAIN,SCLIN,SDAOUT,SCLOUT,READY or ENABLE, V_n		-0.5V to 7V
Input clamp current, I_{IK}	V_I<0	-50mA

PARAMETERS		RANGE
Output clamp current, I_{oK}	V_o<0	-50mA
Continuous output current, I_O	SDAIN,SDAOUT,SCLIN,SCLOUT, ENABLE,READY	±50mA
Continuous current through VCC or GND, I_{CC}		±100mA
Operating temperature, T_{oper}		-40°C to 105°C
Storage temperature, T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds), T_{Sp}		300°C
Maximum operating junction temperature, T_{JMAX}		130°C
ESD(Including CDM HBM)(NOTE2)		
HBM		±7kV
CDM		±1.5kV
Latch-Up		
Test condition: JESD78F		+IT: 450mA -IT: -450mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The HBM test method: ESDA/JEDEC JS-001-2023, the CDM test method: ESDA/JEDEC JS-002-2022.

Recommended Operating Conditions

Symbol	Parameters		Min.	Typ.	Max.	Unit
VCC	Supply voltage		2.3		5.5	V
V_I	input voltage range	ENABLE	0		5.5	V
V_{IO}	Input/output voltage range	SDAIN, SCLIN, SDAOUT, SCLOUT	0		5.5	V
V_O	output voltage range	READY	0		5.5	V
T_A	Operating free-air temperature		-40		105	°C

Electrical Characteristics

VCC=2.3V to 5.5V, T_A=-40°C to 105°C; unless otherwise specified.

Parameters		Test Condition	Min.	Typ.	Max.	Unit
Power supply						
VCC	Supply voltage		2.3		5.5	V
I_{CC}	Supply current	VCC=5.5V; V_{SDAIN}=V_{SDAIN}=0V; SDAOUT, SCLOUT=10kΩ Rpu		4.2	6.3	mA

Parameters		Test Condition	Min.	Typ.	Max.	Unit
$I_{CC(sd)}$ (NOTE3)	Shut-down mode supply current	V_{ENABLE}=0V; all other pins at VCC or GND; Ready pin=Hi-z		0.04	5	μA
UVLO	Under voltage lockout (rising)	ENABLE=VCC READY=10kΩ to VCC		2.15		V
	Under voltage lockout (falling)			2		V
Start-up circuitry						
V_{PRE}	Pre-charge voltage	SDA, SCL=Hi-Z	0.8	1.15	1.25	V
Rise-time accelerators						
I_{PU} (NOTE4)	RTA pull-up current	Position transition on SDA, SCL $V_{SDA/SCL}$=0.6V, Slew rate=1.25V/μs, VCC=3.3V	1	3		mA
Input-output connection						
I_{LI}	Input pin leakage	SDA/SCL pins=90%VCC, ENABLE=VCC or GND; SDA/SCL pins=10%VCC, ENABLE=GND	-1		-1	μA
V_{OS}	Input-output offset voltage	10kΩ to VCC on SDA, SCL; VCC=3.3V	0	105	175	mV
I_{I_RDY}	Ready pin leakage	ENABLE=VCC, READY=VCC, Bus connected	-1		1	μA
$I_{I(ENABLE)}$	input current on pin ENABLE	V_{ENABLE}=0V to VCC	-1		1	μA
Digital IO threshold						
V_{IH}	High-level input voltage	ENABLE	0.7*VCC		VCC	V
V_{IL}	Low-level input voltage	ENABLE	0		0.3*VCC	V
V_{OL}	Low-level output voltage	SDAIN, SCLIN, SDAOUT, SCLOUT I_{OL}=3mA, V_{IN}=0V			0.4	V
		READY, I_{OL}=3mA			0.4	V
Dynamic characteristics						
$C_{IN(ENABLE)}$	ENABLE input capacitance	V_{ENABLE}=0V or VCC; f=400kHz		4		pF
$C_{IO(READY)}$	READY output capacitance	V_{READY}=0V or VCC; f=400kHz		4		pF
$C_{IO\ (SDA/SCL)}$	SDA/SCL pin capacitance	V_{PIN} =0V or VCC; f=400kHz		8		pF

NOTE3: In shutdown mode there will also be current flowing from VCC through the ready pin as this pin is pulled down to indicate the bus is disconnected.

NOTE4: Determined by design, not tested in production.

Timing Requirements

Parameters		Min.	Nom.	Max.	Unit
f_{SCL}(NOTE5)	SCL clock frequency	0	-	400	kHz
t_{BUF}(NOTE5)	Time between start and stop condition	1.3			μs
$t_{HD:STA}$(NOTE5)	(Repeat-start) START condition hold time	0.6		-	μs
$t_{SU:STA}$(NOTE5)	(Repeat-start) START condition setup time	0.6			μs
$t_{SU:STO}$(NOTE5)	STOP condition setup time	0.6		-	μs
$t_{HD:DAT}$(NOTE5)	Data hold time	0		-	μs
$t_{SU:DAT}$(NOTE5)	Data setup time	0.1		-	μs
t_{LOW}(NOTE5)	Low level width of SCL	1.3		-	μs
t_{HIGH}(NOTE5)	High level width of SCL	0.6		-	μs
t_F(NOTE5)	Falling time of SDA and SCL	20×(VCC/ 5.5V)		300	ns
t_R(NOTE5)	Rising time of SDA and SCL	20×(VCC/ 5.5V)		300	ns

NOTE5: These are system-level timing specs and are dependent upon bus capacitance and pull up resistor value. It is up to the system designer to ensure they are met.

Switching Characteristics

VCC=2.3V to 5.5V, T_A=-40°C to 105°C; unless otherwise specified.

Parameters		Test Condition	Min.	Typ.	Max.	Unit
Start-up circuitry						
$t_{PRE-CHARGE}$	Time from VCC to pre-charge enabled	SDA,SCL=Hi-Z; ENABLE=VCC, GND		75		μs
t_{EN}	Time from EN low to high to digital being ready	ENABLE transition from 0V to VCC; Measured at 0.5×VCC		80		μs
t_{IDLE}	bus idle time to READY active	SDA,SCL=10kΩ to VCC; ENABLE=VCC; Measured at 0.5×VCC	50	100	160	μs
$t_{DISABLE}$	disable time (ENABLE to READY)	SDA,SCL=10kΩ to VCC; READY=10kΩ to VCC; Measured at 0.5×VCC		20		ns
t_{STOP}	SDAIN to READY delay after STOP	SDA,SCL=10kΩ to VCC; READY=10kΩ to VCC; Measured at 0.5×VCC		0.6		μs
t_{READY}	SCLOUT/SDAOUT to READY delay	SDA,SCL=10kΩ to VCC; READY=10kΩ to VCC Measured at 0.5×VCC		0.4		μs
Input-output connection						

Parameters		Test Condition	Min.	Typ.	Max.	Unit
t_{PLH}	LOW to HIGH propagation delay	SCL to SCL and SDA to SDA; 10 kΩ to VCC; CL=100pF each side Measured at 0.5×VCC		0		ns
t_{PHL}	HIGH to LOW propagation delay	SCL to SCL and SDA to SDA; 10kΩ to VCC; CL=100pF each side Measured at 0.5×VCC		70		ns

Parameter Measurement Information

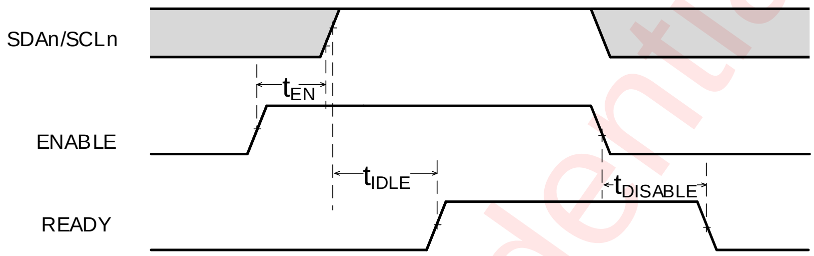


Figure 4 Timing for t_{EN}, t_{IDLE}, and $t_{DISABLE}$

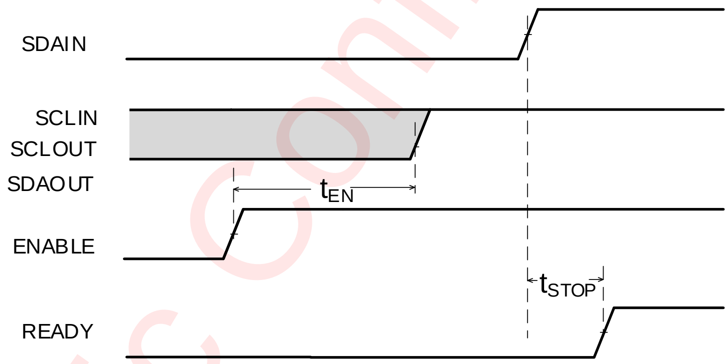


Figure 5 Timing for t_{STOP}

Typical Characteristics

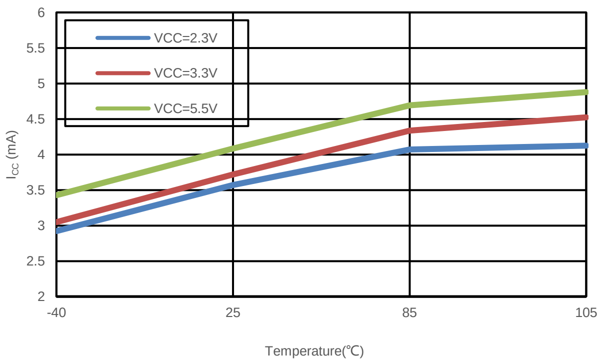


Figure 6 I_{CC} VS Temperature

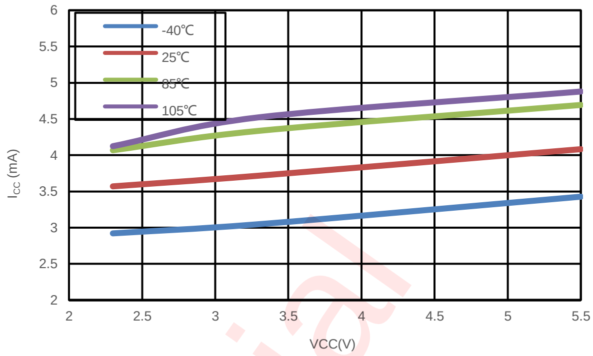


Figure 7 I_{CC} VS VCC

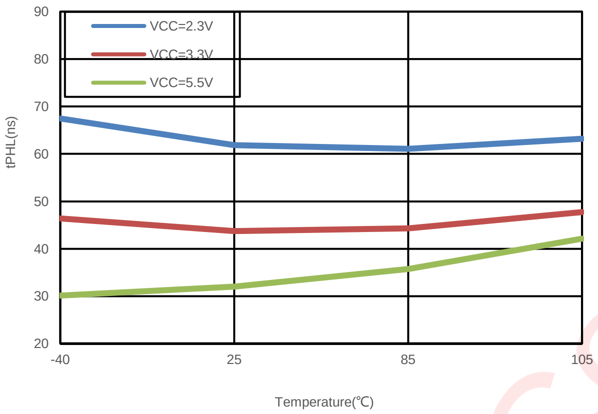


Figure 8 Input/output tPHL VS temperature

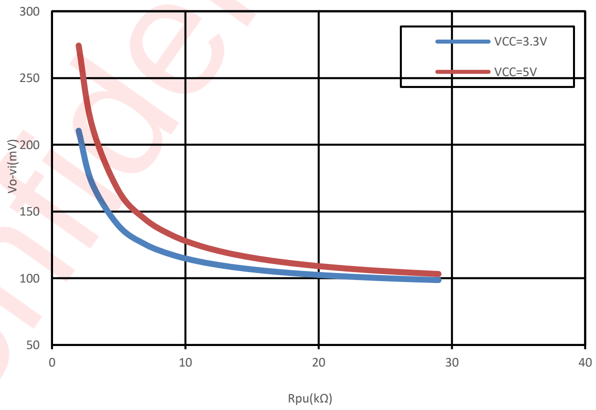


Figure 9 Connection circuitry Vo − Vi

Detailed Functional Description

AW9511 is a hot swappable I2C-bus and SMBus buffer that supports I/O card insertion into a live backplane without corrupting the data and clock lines. Control circuitry prevents the backplane from being connected to the card until a stop command or bus idle occurs on the backplane without bus contention on the card. When the connection is made, the AW9511 provides bidirectional buffering, keeping the backplane and card capacitances isolated. During insertion, the SDA and SCL lines are pre-charged to 1V to minimize the current required to charge the parasitic capacitance of the device.

The AW9511 rise time accelerator circuitry allows the use of weaker DC pull-up currents while still meeting rise time requirements. When the I2C bus is idle, the AW9511 can be put into shutdown mode by setting the ENABLE pin low, reducing power consumption. When ENABLE is pulled high, the AW9511 resumes normal operation. It also includes an open drain READY output pin, which indicates that the backplane and card sides are connected together. When READY is high, the SDAIN and SCLIN are connected to SDAOUT and SCLOUT. When the two sides are disconnected, READY is low.

Start-up And Pre-charge

An undervoltage/initialization circuit holds the parts in a disconnected state which presents high-impedance to all SDA and SCL pins during power-up. A LOW on the ENABLE pin also forces the parts into the low current disconnected state when the I_{CC} is essentially zero. As the power supply is brought up and the ENABLE is HIGH or the part is powered and the ENABLE is taken from LOW to HIGH it enters an initialization state where the internal references are stabilized and the pre-charge circuit is enabled.

At the end of the initialization state the 'Stop Bit And Bus Idle' detect circuit is enabled. With the ENABLE pin HIGH long enough to complete the initialization state (t_{EN}) and remaining HIGH when all the SDA and SCL pins have been HIGH for the bus idle time or when all pins are HIGH and a STOP condition is seen on the SDAIN and SCLIN pins, SDAIN is connected to SDAOUT and SCLIN is connected to SCLOUT. The 1V pre-charge is activated during the initialization and is deactivated when the connection is made. The pre-charge circuitry pulls up the SDA and SCL pins to 1V through individual 100kΩ nominal resistors. This pre-charges the pins to 1V to minimize the worst case disturbances that result from inserting a card into the backplane where the backplane and the card are at opposite logic levels.

Connect Circuitry

Once the connection circuitry is activated, the behavior of SDAIN and SDAOUT as well as SCLIN and SCLOUT become identical with each acting as a bidirectional buffer that isolates the input capacitance from the output bus capacitance while communicating the logic levels. A LOW forced on either SDAIN or SDAOUT will cause the other pin to be driven to a LOW by the part. The same is also true for the SCL pins. Noise between 0.7VCC and VCC is generally ignored because a falling edge is only recognized when it falls below 0.7VCC with a slew rate of at least 1.25V/µs. When a falling edge is seen on one pin, the other pin in the pair turns on a pull-down driver that is referenced to a small voltage above the falling pin. The driver will pull the pin down at a slew rate determined by the driver and the load initially, because it does not start until the first falling pin is below 0.7VCC. The first falling pin may have a fast or slow slew rate, if it is faster than the pull down slew rate then the initial pull-down rate will continue. If the first falling pin has a slow slew rate then the second pin will be pulled down at its initial slew rate only until it is just above the first pin voltage then they will both continue down at the slew rate of the first.

Once both sides are LOW they will remain LOW until all the external drivers have stopped driving LOWs. If both sides are being driven LOW to the same value for instance, 10mV by external drivers, which is the case for clock stretching and is typically the case for acknowledge, and one side external driver stops driving that pin will rise until the internal driver pulls it down to the offset voltage. When the last external driver stops driving a LOW, that pin will rise up and settle out just above the other pin as both rise together with a slew rate determined by the internal slew rate control and the RC time constant. As long as the slew rate is at least

1.25V/μs, when the pin voltage exceeds 0.6V for the AW9511, the rise time accelerator's circuits are turned on and the pull-down driver is turned off.

Propagation Delays

The delay for a rising edge is determined by the combined pull-up current from the bus resistors and the rise time accelerator current source and the effective capacitance on the lines. If the pull-up currents are the same, any difference in rise time is directly proportional to the difference in capacitance between the two sides. The t_{PLH} may be negative if the output capacitance is less than the input capacitance and would be positive if the output capacitance is larger than the input capacitance, when the currents are the same.

The t_{PHL} can never be negative because the output does not start to fall until the input is below 0.7VCC, and the output turn on has a non-zero delay, and the output has a limited maximum slew rate, and even if the input slew rate is slow enough that the output catches up it will still lag the falling voltage of the input by the offset voltage. The maximum t_{PHL} occurs when the input is driven LOW with zero delay and the output is still limited by its turn-on delay and the falling edge slew rate. The output falling edge slew rate is a function of the internal maximum slew rate which is a function of temperature, VCC and process, as well as the load current and the load capacitance.

Rise Time Accelerators

The AW9511 features a rise time accelerator on all I2C pins that during a positive bus transition, switches on a current source to quickly slew the bus pins high. This allows the use of weaker pull-up resistors, which can lower V_{OL} and lower power system level power consumption.

Hot bus insertion

During a hot bus insertion event, the AW9511 keeps the buses disconnected to ensure that no data corruption occurs on either bus. Once the buses are idle or a stop bit on the IN side is detected, the AW9511 connects the buses and READY goes high.

Ready Digital Output

The READY pin is an open drain output that provides an indicator to whether the buses are connected and ready for traffic. This pin is pulled low when the connection between IN/OUT is high impedance. Once the bus is idle or a stop condition on the IN side is detected, and the connection between IN/OUT is made, the READY pin is released and pulled high by an external pull-up resistor.

Enable Low Current Disable

Grounding the ENABLE pin disconnects the backplane side from the card side, disables the rise time accelerators, drives READY LOW, disables the bus pre-charge circuitry, and puts the part in a low current state. When the pin voltage is driven all the way to VCC, the part waits for data transactions on both the backplane and card sides to be complete before reconnecting the two sides.

Powered-off high impedance for I2C and I/O pins

When the supply voltage is below the UVLO threshold, the I2C and digital I/O pins are a high impedance state to prevent leakage currents from flowing through the device. When the ENABLE pin is taken low, the device enters an isolation state, presenting a high impedance on all bus pins and pulling the READY pin low.

Application Information

The typical application is to place the AW9511 on the card that is being inserted or connected to a live bus, rather than being placed on the live bus. The reason for this is to provide maximum benefit by ensuring that the bus stays disconnected until an idle condition or stop condition is seen.

Typical Application

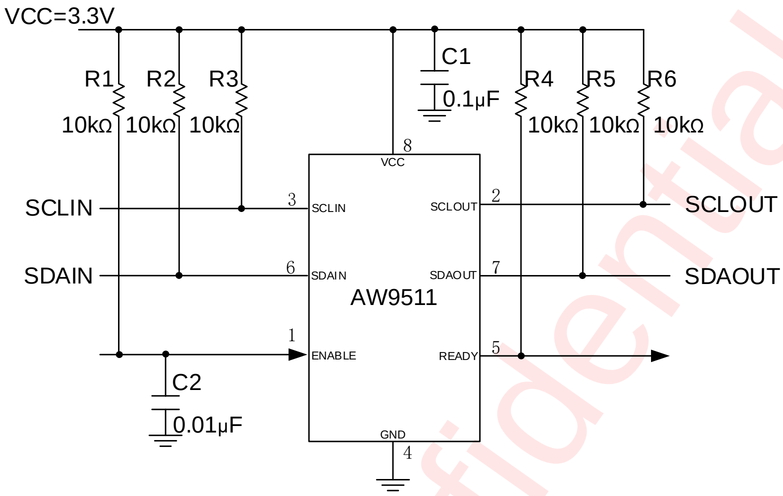


Figure 14 AW9511 General Application Circuit

Series connection

The AW9511 support the application with Series connections, but care must be taken when designing a system.

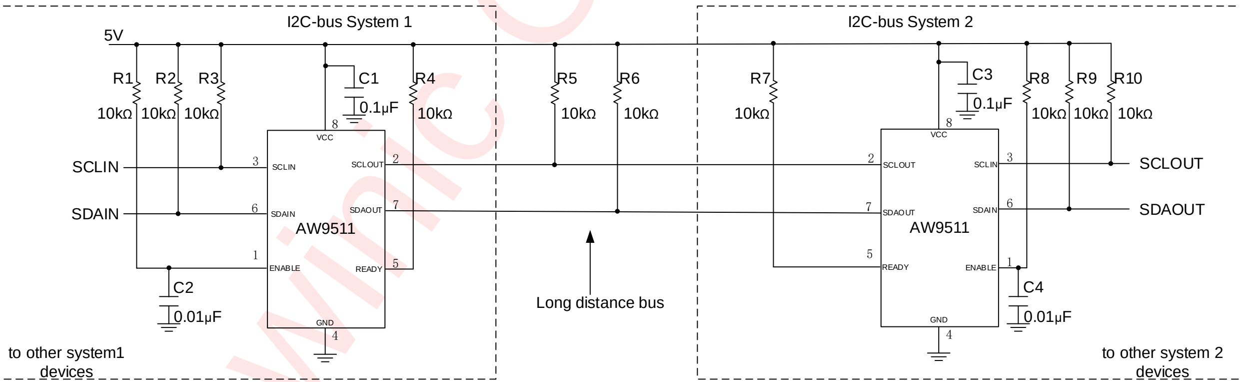


Figure 15 AW9511 Series Application Circuit

Each buffer adds about 0.1V dynamic level offset at 25°C with the offset larger at higher temperatures. The LOW level at the signal origination end (master) is dependent upon the load and the only specification point is that the I2C-bus specification of 3mA will produce VOL<0.4 V, although if lightly loaded the V_{OL} may be ~0.1V. Assuming V_{OL}=0.1V and V_{offset}=0.1V, the level after four buffers would be 0.5V, which is only about 0.1V below the threshold of the rising edge accelerator (about 0.6V). With great care a system with four buffers may work, but as the V_{OL} moves up from 0.1V, noise or bounces on the line will result in firing the rising edge accelerator thus introducing false clock edges. Generally it is recommended to limit the number of buffers in series to two, and to keep the load light to minimize the offset.

Multiple Connections To A Common Node

It is possible to have multiple buffers in connect to a common node, but care must be taken when designing a system.

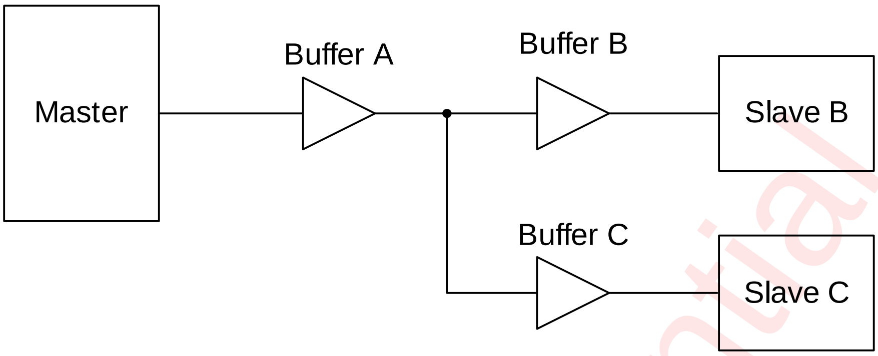


Figure 16 AW9511 Connection to Common Node

It is important to try and avoid common node architectures. The multiple nodes sharing a common node can create glitches if the output voltage from a master slave device plus the offset voltage of the buffer are high enough to trip the RTA. Also keep in mind that the V_{OS} must be crossed in order for a device to begin to regulate the other side.

Consider a system with three buffers connected to a common node and communication between the Master and Slave B that are connected at either end of buffer A and buffer B. Consider if the V_{OL} at the input of buffer A is 0.3V and the V_{OL} of Slave B (when acknowledging) is 0.4V with the direction changing from Master to Slave B and then from Slave B to Master. Before the direction change you would observe V_{IL} at the input of buffer A of 0.3V and its output, the common node, is ~0.4V. The output of buffer B and buffer C would be ~0.5V, but Slave B is driving 0.4V, so the voltage at Slave B is 0.4V. The output of buffer C is ~0.5V. When the Master pull-down turns off, the input of buffer A rises and so does its output, the common node, because it is the only part driving the node. The common node will rise to 0.5V before buffer B's output turns on, if the pull-up is strong the node may bounce. If the bounce goes above the threshold for the rising edge accelerator ~0.6V the accelerators on both buffer A and buffer C will fire contending with the output of buffer B. The node on the input of buffer A will go HIGH as will the input node of buffer C. After the common node voltage is stable for a while the rising edge accelerators will turn off and the common node will return to ~0.5V because the buffer B is still on. The voltage at both the Master and Slave C nodes would then fall to ~0.6V until Slave B turned off. This would not cause a failure on the data line as long as the return to 0.5V on the common node (~0.6V at the Master and Slave C) occurred before the data setup time. If this were the SCL line, the parts on buffer A and buffer C would see a false clock rather than a stretched clock, which would cause a system error.

Typical Application on a Backplane

the AW9511 is used in a backplane connection. The AW9511 is placed on the I/O peripheral card and connects the I2C devices on the card to the backplane safely upon a hot insertion event. Note that if the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise time and fall time requirements difficult to meet. Placing a bus buffer on the edge of each card; however, isolates the card capacitance from the backplane. For a given I/O card, the AW9511 drives the capacitance of everything on the card and the backplane must drive only the capacitance of the bus buffer, which is less than 10pF, the connector, trace, and all additional cards on the backplane.

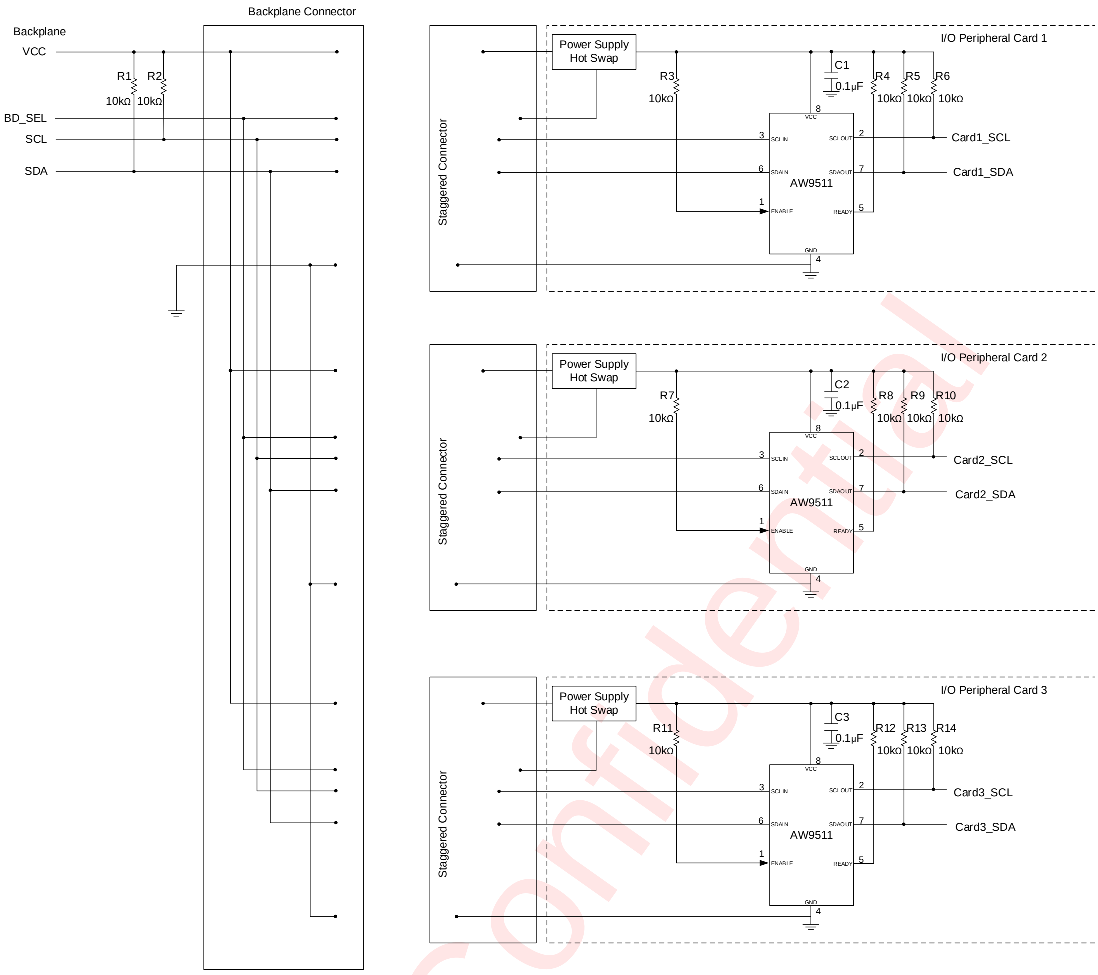


Figure 17 Backplane Application Schematic 1

The AW9511 can be used in any combination depending on the number of rise time accelerators that are needed by the system. Normally only one AW9511 would be required per bus.

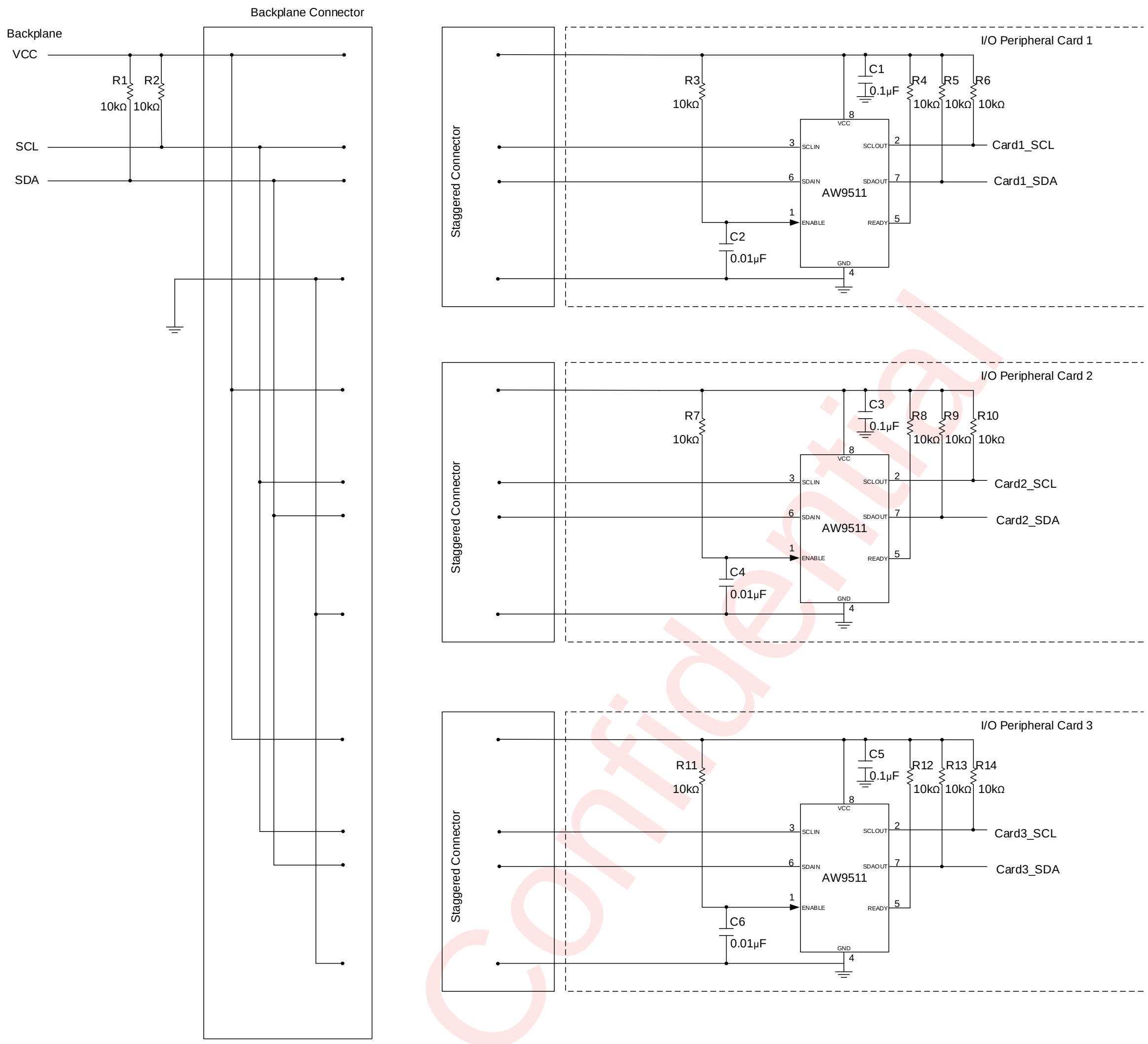


Figure 18 Backplane Application Schematic 2

Pull-up Resistor Calculation

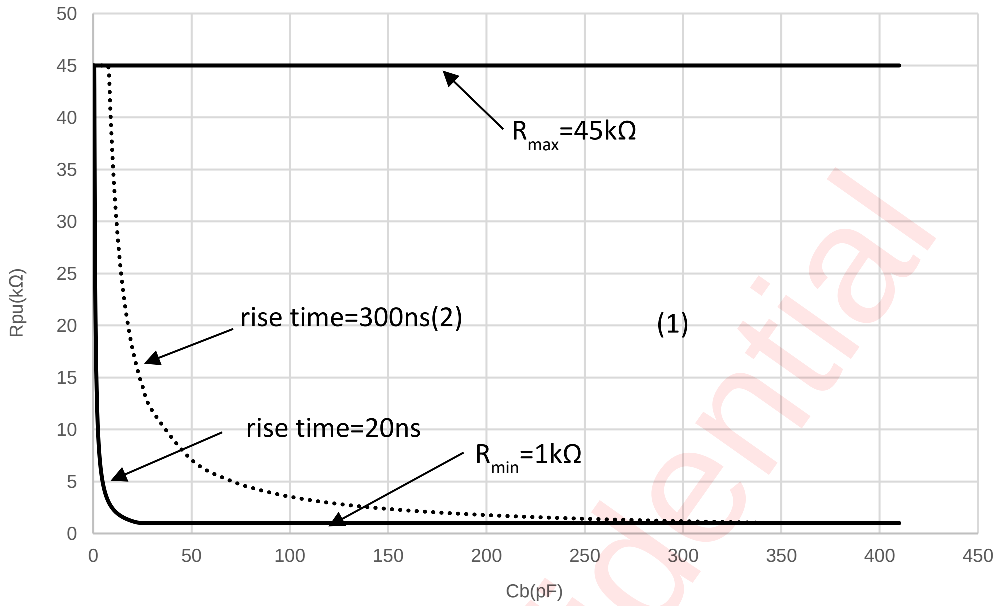
The system pull-up resistors must be strong enough to provide a positive slew rate of 1.25V/μs on the SDA and SCL pins, in order to activate the boost pull-up currents during rising edges. Choose maximum resistor value using the formula given in Equation 1.

$$R \leqslant 800 \times 10^{3} \left(\frac{V_{CC(MIN)}-0.6}{C}\right) \quad (1)$$

Where R is the pull-up resistor value in Ω, $VCC_{(min)}$ is the minimum VCC voltage in volts, and C is the equivalent bus capacitance in picofarads (pF).

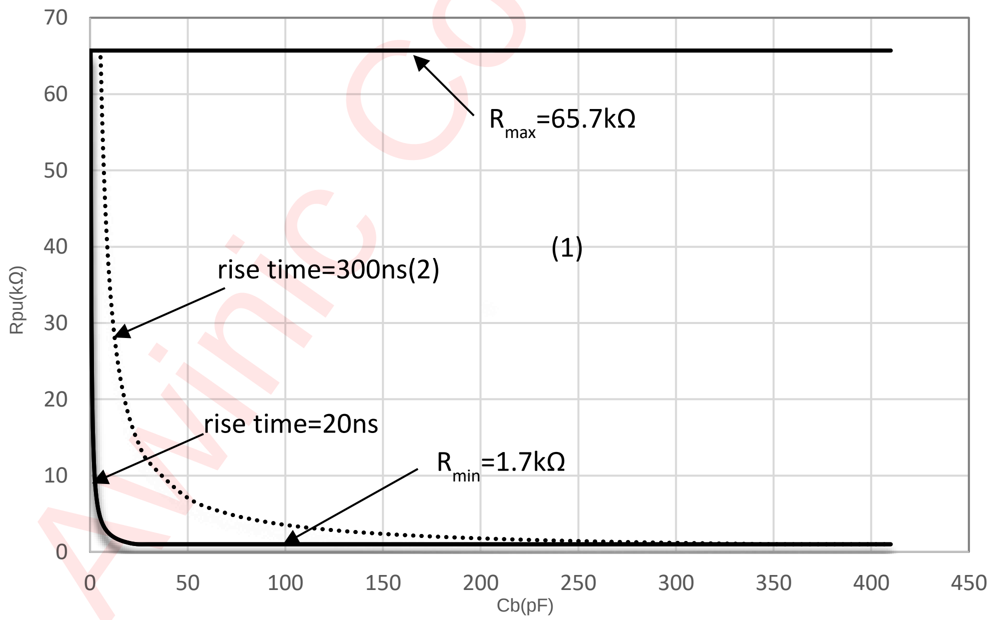
In addition, regardless of the bus capacitance, always choose R_{PU}≤65.7kΩ for VCC=5V, R_{PU}≤45kΩ for VCC=3.3V. The start-up circuitry requires logic HIGH voltages on SDAOUT and SCLOUT to connect the backplane to the card, and these pull-up values are needed to overcome the pre-charge voltage.

Application Curves



(1) Area indicates recommended pull-up, for rise time<300ns, with AW9511.
(2) Rise time without AW9511.

Figure 19 Bus requirements for 3.3V systems



(1) Area indicates recommended pull-up, for rise time<300ns, with AW9511.
(2) Rise time without AW9511.

Figure 20 Bus requirements for 5V systems

PCB Layout Consideration

AW9511 is a hot swappable I2C-bus and SMBus buffer that supports I/O card insertion into a live backplane without corrupting the data and clock lines. To obtain the good thermal performance, PCB layout should be considered carefully. Here are some guidelines:

1. The C1 should be placed as close to the chip as possible.
2. To reduce the total I2C bus capacitance added by PCB parasitics, I2C lines must be as short as possible and the widths of the traces must also be minimized.
3. The wiring of I2C needs to pay attention to impedance matching.

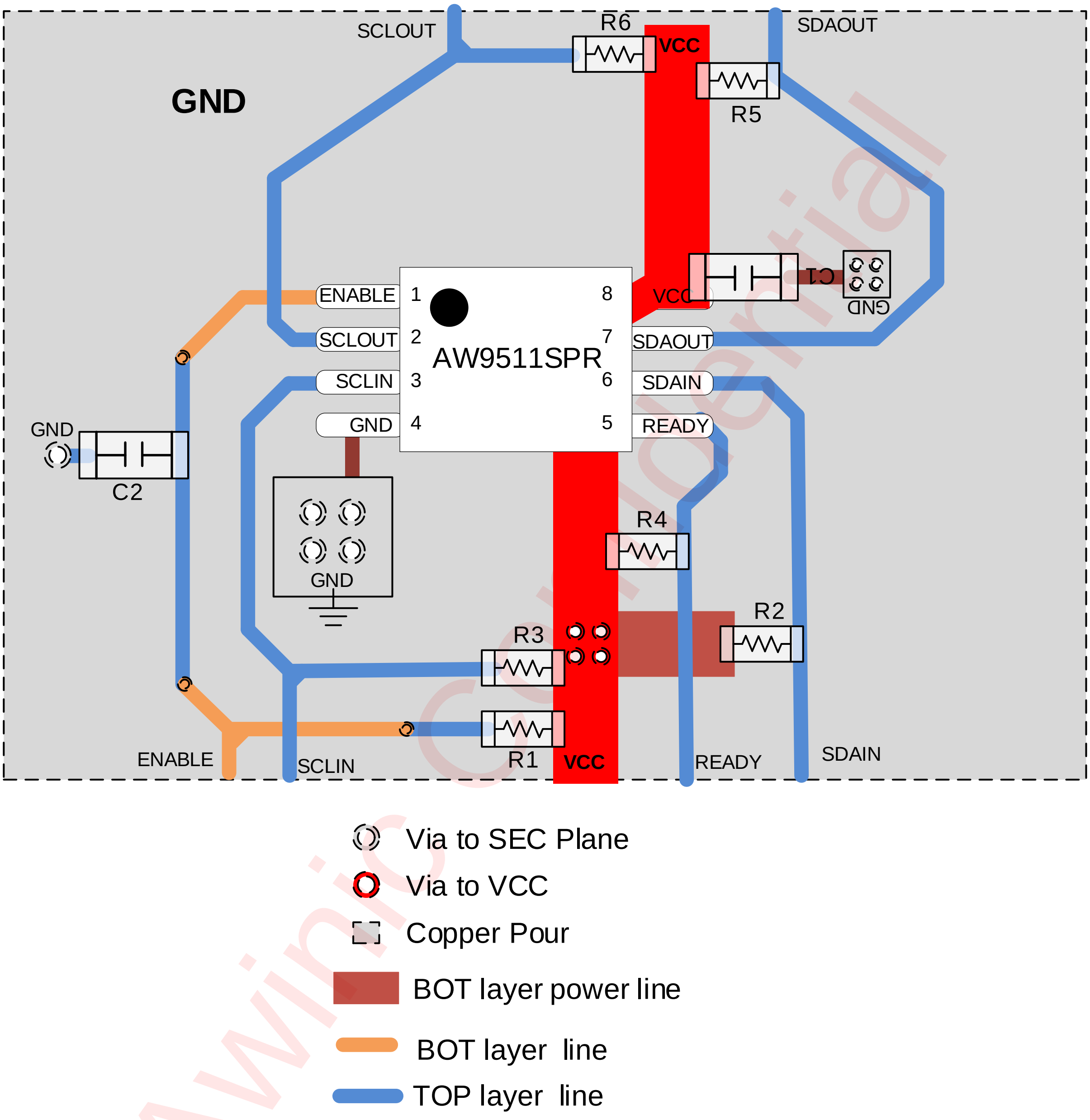
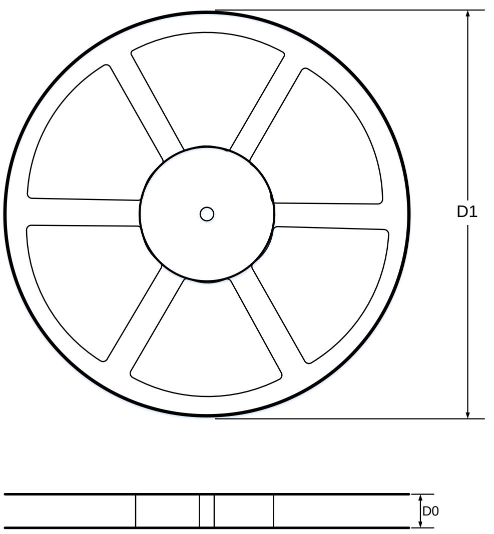


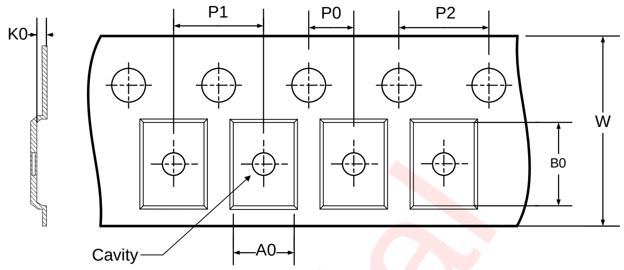
Figure 21 AW9511SPR Layout Example

Tape And Reel Information

REEL DIMENSIONS

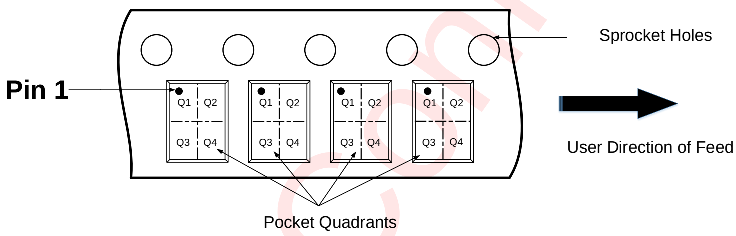


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



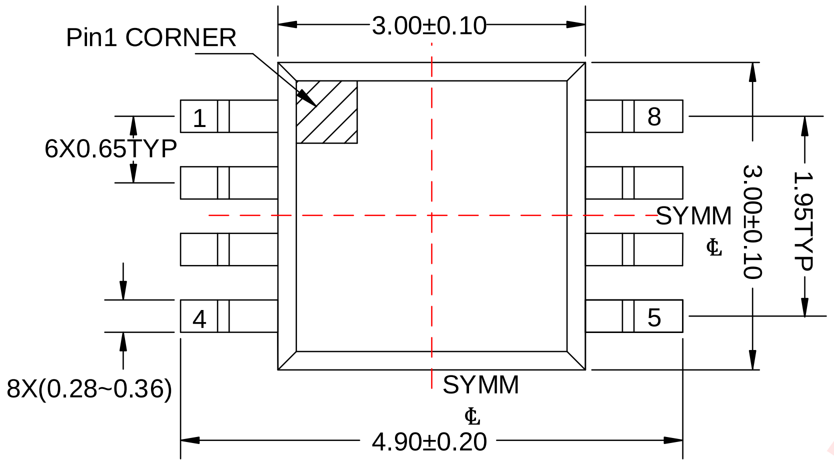
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

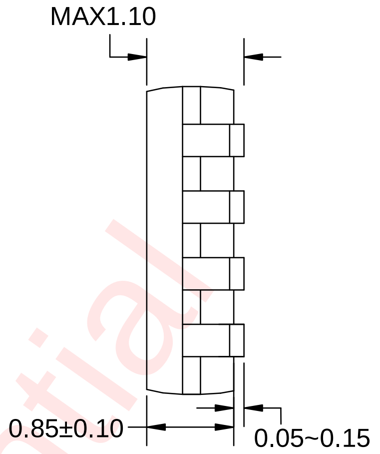
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	5.4	3.4	1.4	2	8	4	12	Q1

All dimensions are nominal

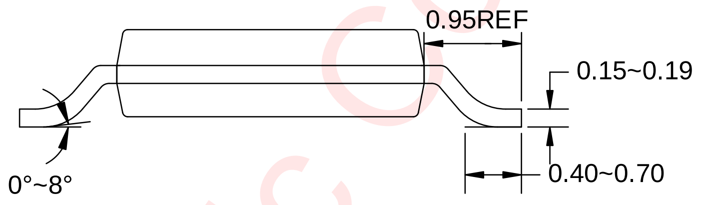
Package Description



Top View



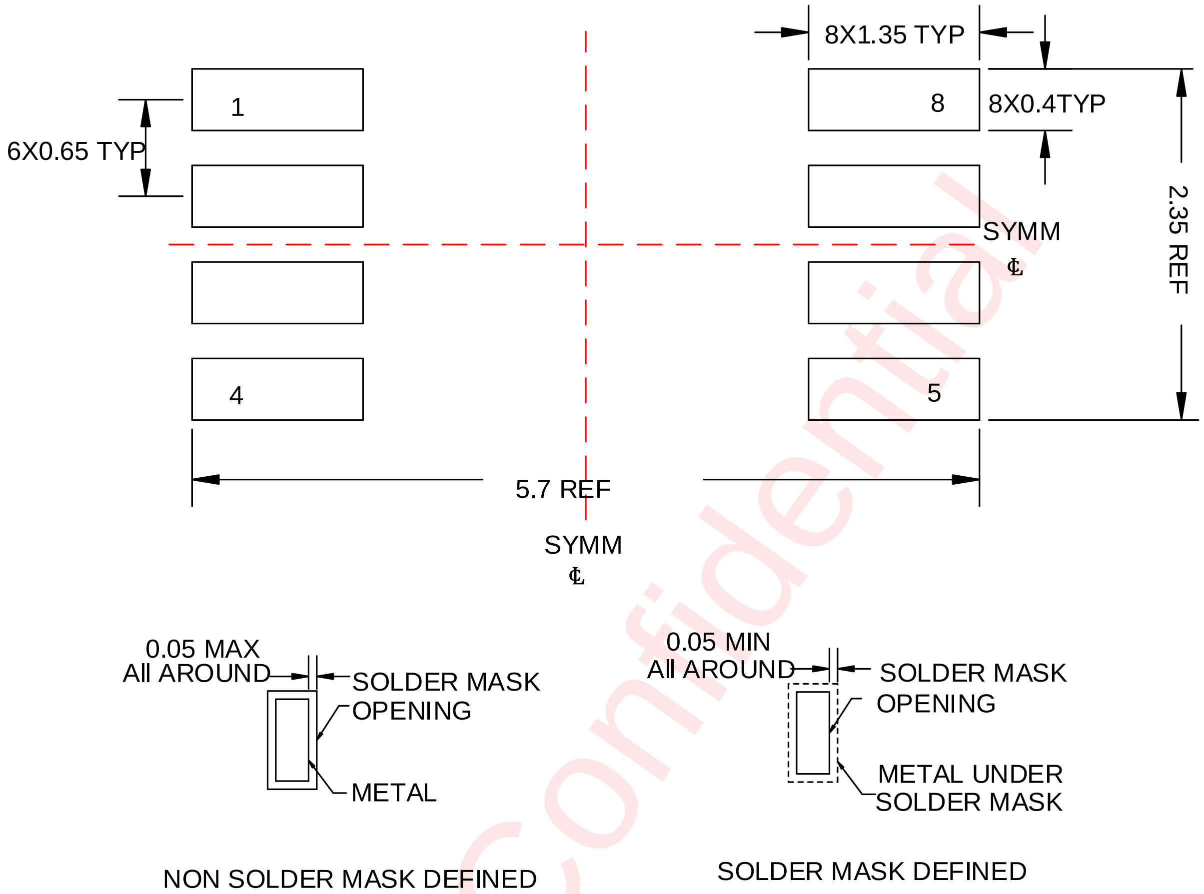
Side View



Side View

Unit: mm

Land Pattern Data



Unit：mm

Revision History

Version	Date	Change Record
V1.0	Apr. 2024	Officially released
V1.1	Jun. 2024	Update the table of Absolute Maximum Ratings

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