High Efficiency, Support 0.3% PWM Dimming Boost WLED Driver

FEATURES

- Support 0.3% PWM dimming
- PWM control input for CABC operation
- 1.1MHz Switching Frequency
- 38V Over-voltage Protection for up to 10 LEDs in Series
- 200mV Reference Voltage
- 2.7V to 5.5V Input Voltage Range
- Over-current and Over-temperature Protection
- Built-in Soft-start Limits Inrush Current
- DFN 2mm X2mm X0.75mm-6L package

APPLICATIONS

- Mobile Phones
- Portable Media Players
- PDAs
- GPS Receivers

GENERAL DESCRIPTION

The AW9962E is a white LED (WLED) driver with integrated boost converter. The boost converter runs at 1.1MHz fixed switching frequency, with an internal 40V, 2A switch FET, the AW9962E can drive one string (up to 10 LEDs) and parallel LED strings.

The full-scale WLED current can be set by the equation 200mV/R_{SET}. R_{SET} should be changed for parallel applications.

The current of WLED can also be set with duty cycle of PWM signal applied to the CTRL pin with 10kHz~100kHz.

AW9962E integrates built-in soft-start function to minimize the power supply inrush current. AW9962E also integrates over-current protection, LED open protection and over temperature protection(OTP) to prevent chip from entering abnormal operating conditions.

TYPICAL APPLICATION CIRCUIT

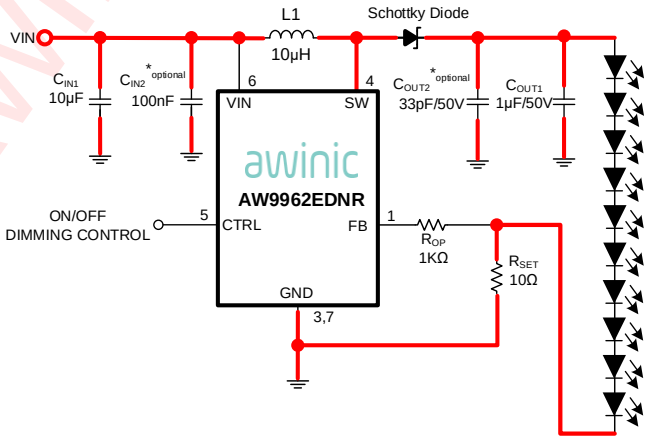
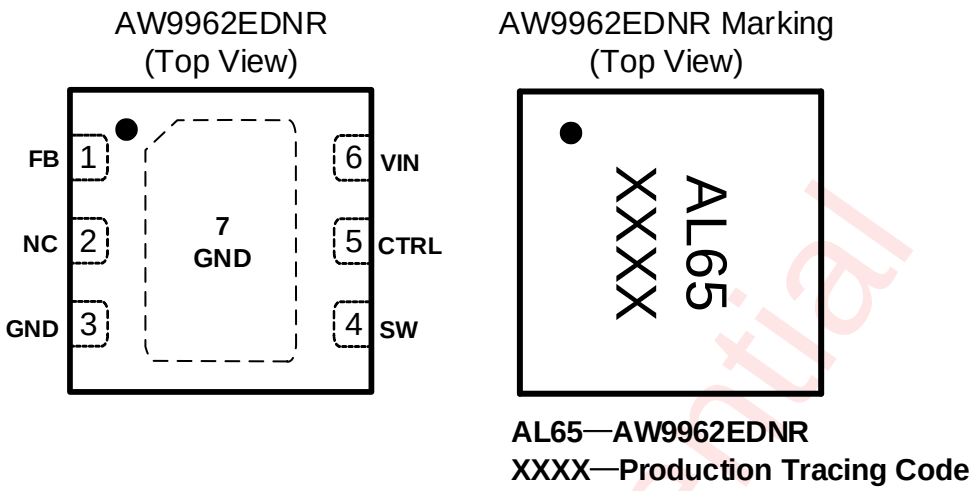


Figure 1 Typical Application Circuit of AW9962E

NOTE: R_{OP} is optional for high ESD protection level condition.

PIN CONFIGURATION AND TOP MARK



AL65—AW9962EDNR
XXXX—Production Tracing Code

Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
1	FB	Feedback pin. Connect R_{SET} from FB to GND.
2	NC	No Connection
3	GND	Ground.
4	SW	Switching node.
5	CTRL	Enable pin. It also can be used for PWM digital dimming.
6	VIN	Power
7	GND	Exposed pad should be soldered to PCB board and Connected to GND.

FUNCTIONAL BLOCK DIAGRAM

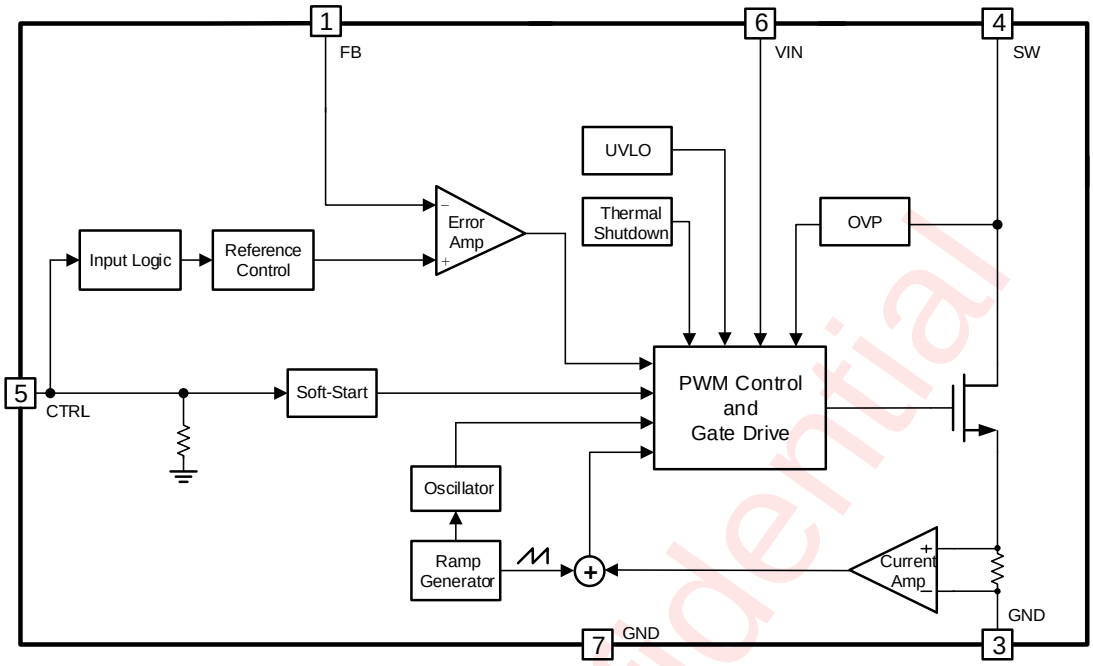


Figure 3 FUNCTIONAL BLOCK DIAGRAM

TYPICAL APPLICATION CIRCUITS

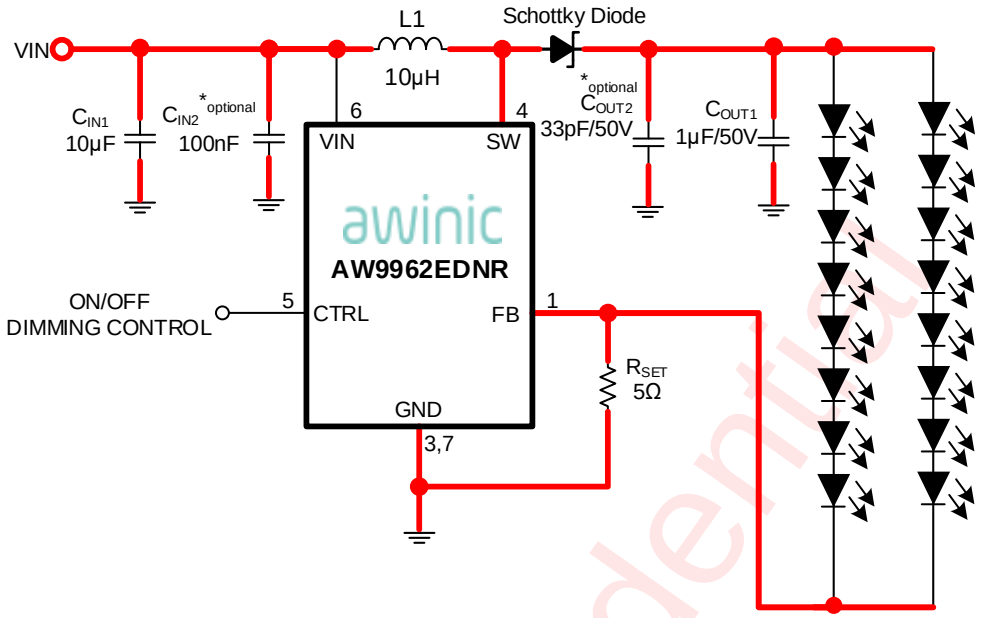


Figure 4 Typical Application of AW9962E

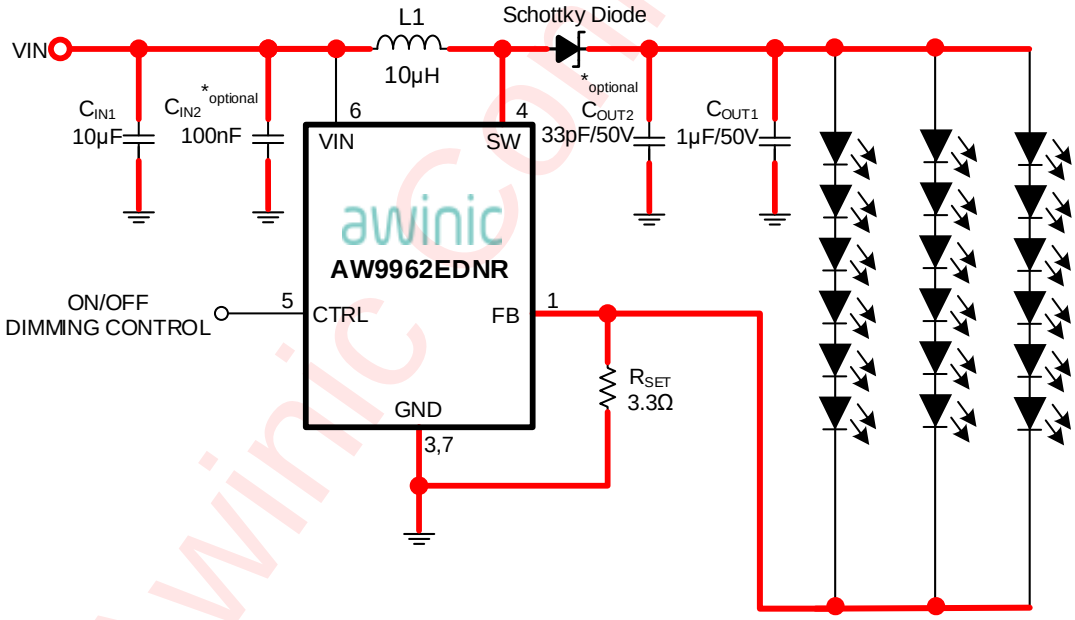


Figure 5 Drive 18 White LEDs for Large Screen Display

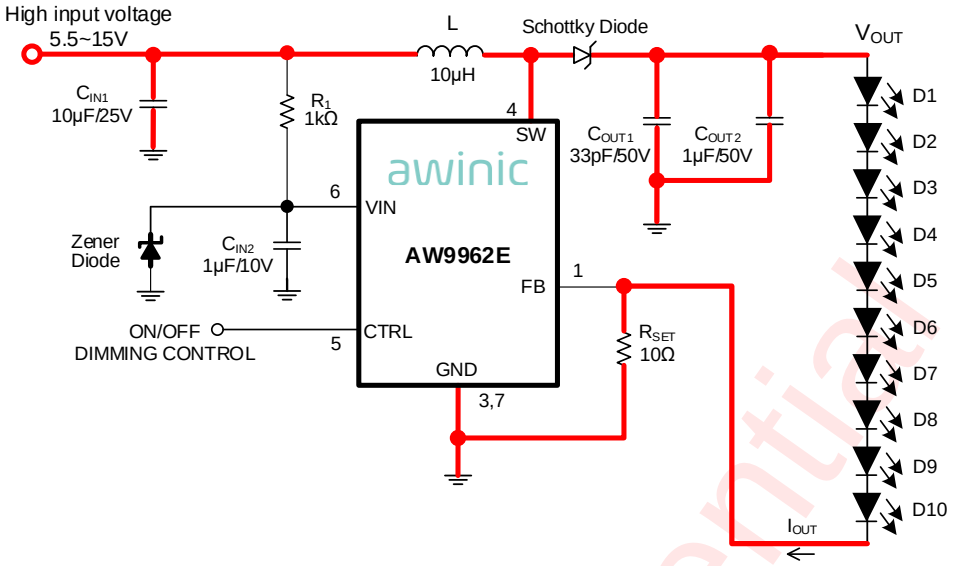


Figure 6 High Input Voltage Application of AW9962E

Notice for Typical Application Circuits:

1：Recommended device for AW9962E:

L: LQH3NPN100NM0

C_{IN1}: Murata GRM188R61C106MA73

C_{IN2}: Murata GRM155R61C104K

C_{OUT1}: Murata GRM21BR71H105KA

C_{OUT2}: Murata GRM1555C1H330GA

Schottky Diode: ONsemi MBR0540

2：C_{IN2} and C_{OUT2} are recommended to use in parallel with the input capacitor and output capacitor to suppress high frequency noise.

3：Red lines are high current paths, reference to the section APPLICATION INFORMATION.

4：The capacitors (C_{IN1}, C_{IN2}, C_{OUT1}, C_{OUT2}) should be placed as close to the pins of the IC as possible.

5：Minimize trace lengths between the IC and the inductor, the Schottky diode and the output capacitor, keep these traces short, direct, and wide.

6：Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize inter-plane coupling.

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW9962EDNR	-40°C~85°C	DFN 2mmx2mm-6L	AL65	MSL1	ROHS+HF	3000 units/ Tape and Reel

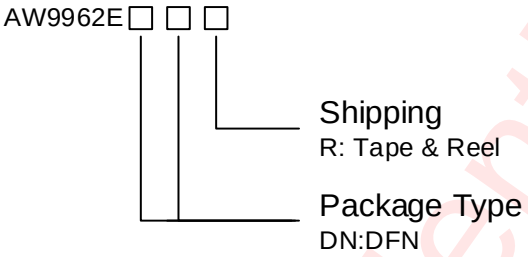


Figure 7 Package Information

ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS	RANGE
Supply voltage range VIN(NOTE 2)	-0.3V to 6V
Voltage on FB,CTRL (NOTE 2)	-0.3V to 6V
Voltage on SW(NOTE 2)	-0.3V to 40V
Junction-to-ambient thermal resistance θ_{JA}	140°C/W
Junction-to-board thermal resistance θ_{JB}	55°C/W
Operating free-air temperature range	-40°C to 85°C
Operating Junction temperature T_J	-40°C to 150°C
Storage temperature T_{STG}	-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)	260°C
ESD(NOTE 3)	
ALL PINS HBM (human body model) (NOTE 4)	±2kV
ALL PINS CDM (charge device model) (NOTE 5)	±1.5kV
Latch-up(NOTE 6)	
Latch-up current maximum rating per JEDEC standard	+IT：200mA -IT：-200mA

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: *All voltage values are with respect to network ground terminal.*

NOTE3: This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. AWINIC recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

NOTE4: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE5: Test Condition: ESDA/JEDEC JS-002-2014.

NOTE6: Test Condition: JEDEC STANDARD NO.78D NOVEMBER 2011.

ELECTRICAL CHARACTERISTICS

Test Condition: T_A = 25°C, V_{IN} = 3.6V, V_{CTRL} = V_{IN} (Unless otherwise specified).

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT						
V_{IN}	Input voltage range		2.7		5.5	V
V_{UVLO}	Under-voltage lockout threshold	V_{IN} falling		2.2	2.39	V
V_{HYS}	Under-voltage lockout hysteresis			100		mV
I_{SD}	Shutdown current	V_{CTRL} = GND, V_{IN}=4.2V		0.1	1	μA
I_Q	Operating quiescent current	V_{FB} = 1V		250		μA
PWM DIMMING CONTROL						
f_{PWM}[1]	Frequency of PWM dimming		10		100	kHz
D_{PWM}	PWM dimming duty cycle		0.3		100	%
t_{MIN_ON}	Minimum on pulse width			50		ns
VOLTAGE AND CURRENT CONTROL						
V_{REF}	Voltage feedback regulation voltage		194	200	205	mV
V_{REF_PWM}	Voltage feedback regulation voltage under brightness control	PWM duty cycle = 1%	1.575	2.25	2.925	mV
		PWM duty cycle = 0.3%		0.8		mV
I_{FB}	Voltage feedback input bias current			0.1	1	μA
BOOST CONVERTER						
$R_{DS(on)}$	N-channel MOSFET on-resistance	VIN = 3.6V		0.4	0.7	Ω
		VIN = 3.0V			0.7	Ω
f_S	Oscillator frequency			1100		kHz
D_{MAX}[1]	Maximum duty cycle		90	93		%
OCP AND OVP						
I_{LIM}	N-channel MOSFET current limit			2		A
V_{OVP}	Open LED overvoltage protection threshold	Measured on the SW pin	36	38	40	V
t_{REF}	VREF filter time constant			480		μs
CTRL INTERFACE						
V_{CTRL_H}	CTRL logic high voltage	VIN = 2.7V to 5.5V	1.4			V
V_{CTRL_L}	CTRL logic low voltage	VIN = 2.7V to 5.5V			0.4	V
R_{CTRL}	CTRL pull down resistor			600		kΩ
t_{OFF}[1]	CTRL pulse width to shutdown	CTRL high to low	2.5			ms

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN						
T_{OTP}	Thermal shutdown threshold			165		°C
T_{HYS}	Thermal shutdown threshold hysteresis			15		°C

Note1：Minimum or maximum limit guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

TYPICAL CHARACTERISTICS

Table 1 TABLE OF FIGURES

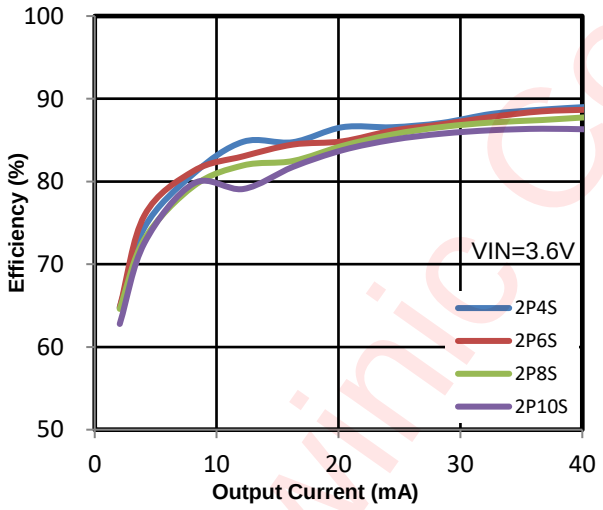


Fig8. EFFICIENCY vs OUTPUT CURRENT

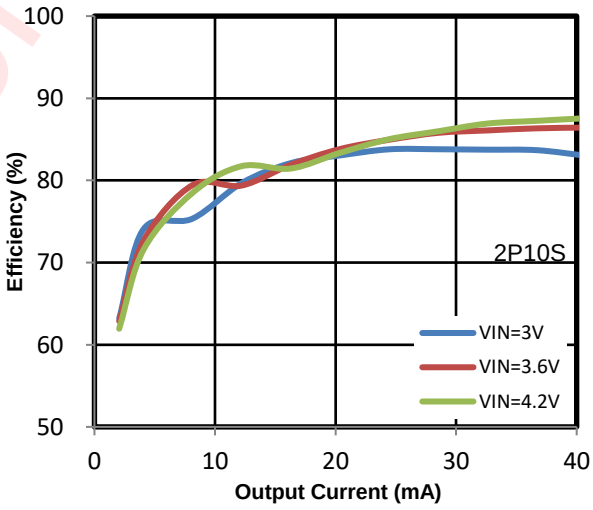


Fig9. EFFICIENCY vs OUTPUT CURRENT

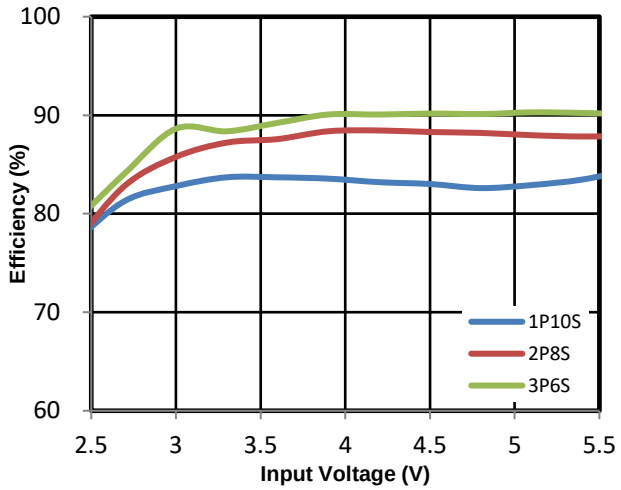


Fig10. EFFICIENCY vs INPUT VOLTAGE

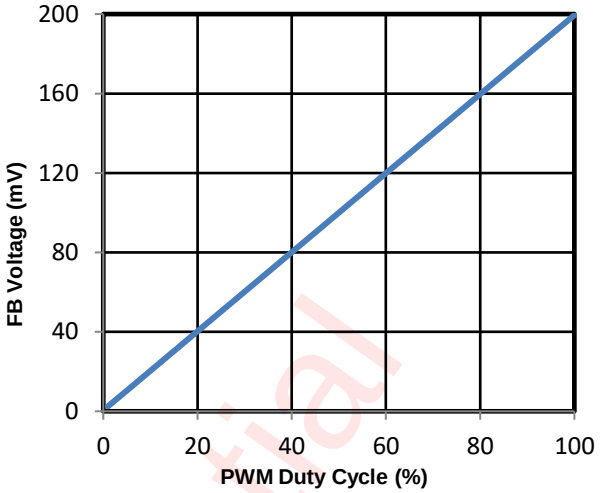


Fig11. FB vs PWM DUTY CYCLE

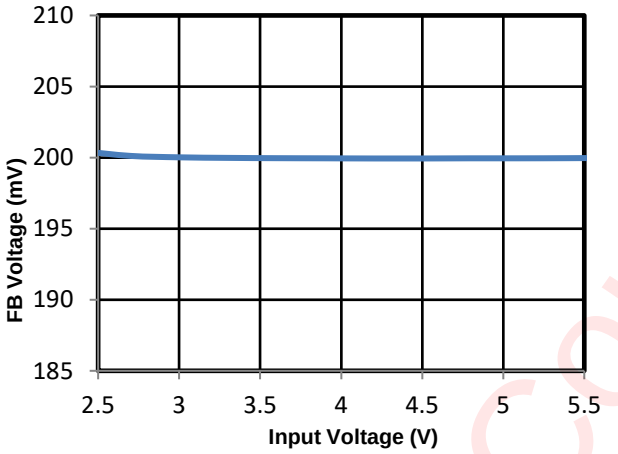


Fig12. FB vs INPUT VOLTAGE

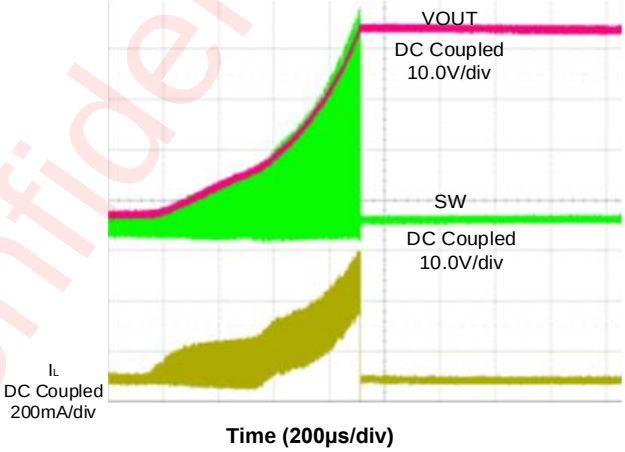


Fig13. OPEN LED PROTECTION

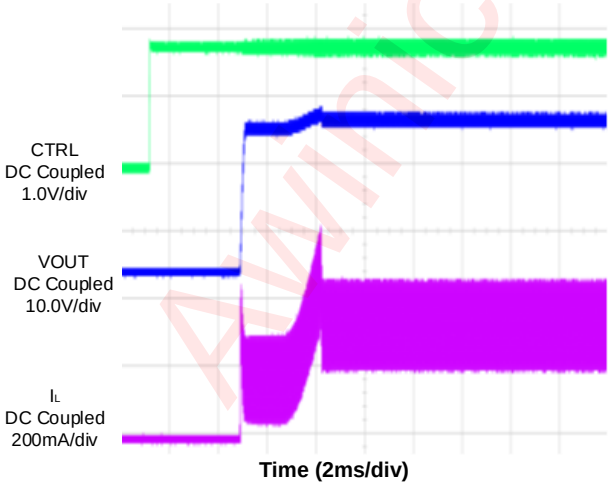


Fig 14. SOFT-START WAVEFORM

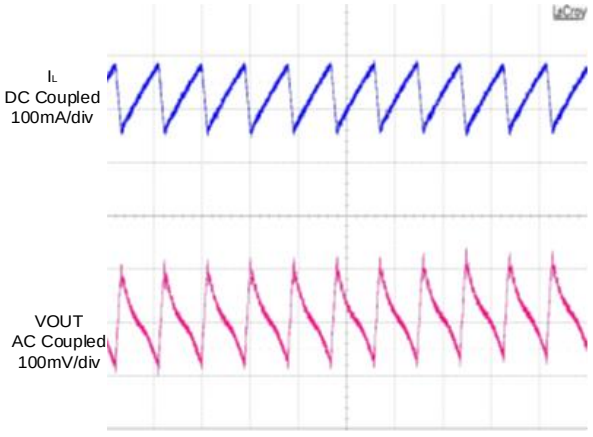


Fig 15. SWITCHING WAVEFORM

DETAILED FUNCTIONAL DESCRIPTION

The AW9962E is a white LED backlight driver IC, which operates in pulse width modulation (PWM) mode with 1.1MHz constant switching frequency and integrates 40V/2.0A switch FET. The duty cycle of boost regulator is set by the error amplifier output and the inductor current signal applied to the PWM comparator. When duty cycle exceeds 50%, slope compensation is added to the current signal for current loop stableness .

SOFT START

When the device is enabled, the error amplifier output ramps up to the target voltage in a specific time. This ensures that the output voltage rises slowly to reduce the input inrush current.

OPEN LED OVER-VOLTAGE PROTECTION

The over-voltage protection function monitors the output voltage via the SW pin voltage. The OVP threshold voltage is 38V typically. Once the LED is open, the output voltage reaches the OVP threshold, the driver will be shut down. During detect process, output voltage will keep stepping up for 8 clock cycles.

SHUTDOWN

The CTRL pin is used for enable device and PWM dimming. When the CTRL voltage is logic low for more than 2.5ms, the driver will be shut down.

UNDER-VOLTAGE LOCKOUT

When the input voltage is lower than the UVLO threshold (2.2V typ.), the driver will turn off. If the input voltage rises by under-voltage lockout hysteresis, the IC restarts.

CURRENT PROGRAM

The LED current is programmed externally using a resistor in series with the LED string. The value of the R_{SET} can be calculated by the following equation:

$$I_{LED} = \frac{V_{FB}}{R_{SET}} \quad (1)$$

Where:

I_{LED} = output current of LEDs

V_{FB} = regulated voltage of FB

R_{SET} = current sense resistor

PWM BRIGHTNESS DIMMING

When the CTRL pin is constantly high, the FB voltage is regulated to 200mV typically. However, the CTRL pin allows a PWM signal to reduce this regulation voltage, it achieves LED brightness dimming. The relationship between the duty cycle and the FB voltage is given by the following equation:

$$V_{FB} = Duty \times 200mV + 0.2mV \quad (2)$$

Where:

Duty = duty cycle of the PWM signal

200mV = internal reference voltage

As shown in the FIGURE 15, the IC chops up the internal 200mV reference voltage at the duty cycle of the PWM signal. The pulse signal is then filtered by an internal low pass filter. The output of the filter is connected to the error amplifier as the reference voltage for the FB pin regulation. Therefore, although a PWM signal is used for brightness dimming, only the WLED DC current is modulated, which is often referred as analog dimming. This eliminates the audible noise which often occurs when the LED current is pulsed in replica of the frequency and duty cycle of PWM control. Unlike other scheme which filters the PWM signal for analog dimming, AW9962E regulation voltage is independent of the PWM logic voltage level which often has large variations.

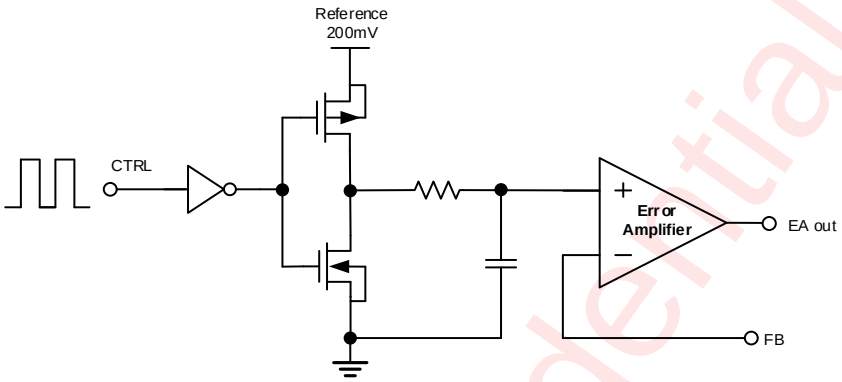


Figure 16 Block Diagram of Programmable FB Voltage Using PWM Signal

THERMAL SHUTDOWN

An internal thermal shutdown turns off the device when the typical junction temperature exceed 165°C. The device will restart when the junction temperature decreases by 15°C.

APPLICATION INFORMATION

INDUCTOR SELECTION

Because the selection of inductor affects power supply's steady state operation, transient behavior, loop stability and the boost converter efficiency, the inductor is one of the most important components in switching power regulator design. There are three important inductor specifications, inductor value, DC resistance and saturation current.

The inductor DC current can be calculated as:

$$I_{IN\_DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (3)$$

The inductor current peak to peak ripple can be calculated as

$$I_{PP} = \frac{1}{L \times F_S \times \left(\frac{1}{V_{OUT}+V_F-V_{IN}} + \frac{1}{V_{IN}}\right)} \quad (4)$$

Therefore, the peak current I_P seen by the inductor is calculated as

$$I_P = I_{IN\_DC} + \frac{I_{PP}}{2} \quad (5)$$

The inductor saturation current rating should be considered to cover the inductor peak current. Smaller size and better efficiency are the major concerns for portable devices. The inductor should have low core loss at 1100kHz and low DCR for better efficiency. For these reasons, a 4.7μH to 10μH inductor value range is recommended. A 10μH inductor optimized the efficiency for most application while maintaining low inductor peak to peak ripple. TABLE 2 lists the recommended inductor for the AW9962E. When recommending inductor value, the factory has considered –40% and +20% tolerance from its nominal value.

Table 2 Recommended Inductors for AW9962E

Part Number	L (μH)	DCR Max (Ω)	Saturation Current (mA)	Size (L x W x H mm)	Vendor
MRSC252A10-100M-N	10	0.5	900	2.5 x 2 x 1	Chilisin
LQH3NPN100NM0	10	0.3	750	3 x 3 x 1.5	Murata
CDH3809/SLD	10	0.3	570	4 x 4 x 1.0	Sumida
LPS4018-472ML	4.7	0.125	1900	4 x 4 x 1.8	Coilcraft

SCHOTTKY DIODE SELECTION

To optimize the efficiency, a high-speed and low reverse-recovery current Schottky diode are recommended. Make sure the diode's average and peak current ratings exceed the output average LED current and the peak inductor current. In addition, the diode's break-down voltage rating must exceed the maximum voltage across the diode. Usually, unexpected high-frequency voltage spikes can be seen across the diode when the diode turns off. Therefore, leaving some voltage rating margin is always needed to guarantee normal long-term operation when selecting a diode. The MBR0540 and the NSR05F40 are recommended for AW9962E.

INPUT AND OUTPUT CAPACITORS SELECTION

The output capacitor keeps the output voltage ripple small and ensures feedback loop stability. This ripple

voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming ESR of a capacitor is zero, the minimum capacitance needed for a given ripple can be calculated by:

$$C_{OUT} = \frac{(V_{OUT} - V_{IN}) \times I_{OUT}}{V_{OUT} \times F_S \times V_{ripple}} \quad (6)$$

Where, V_{ripple} represents peak-to-peak output ripple. The additional output ripple caused by ESR can be calculated as:

$$V_{ripple\_ESR} = I_{OUT} \times R_{ESR} \quad (7)$$

V_{ripple_ESR} can be neglected for ceramic capacitors due to its low ESR, but must be considered if tantalum or electrolytic capacitors are used.

Note that the ceramic capacitance is dependent on the voltage rating. With a DC bias voltage, the capacitance can lose as much as 50% of its value at its rated voltage rating. Leave a large enough voltage rating margin when selecting the component. Therefore, leave enough margin on the voltage rating to ensure adequate capacitance at the required output voltage.

An X5R or X7R capacitor of 10μF is recommended for input side. The output requires a X5R or X7R capacitor in the range of 0.47μF to 4.7μF. A 100nF capacitor and a 33 pF capacitor are recommended to use in parallel with the input capacitor and the output capacitor to suppress high frequency noise.

The output capacitor affects the loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable.

Note that capacitor degradation increases the ripple much. Select the capacitor with 50V rated voltage to reduce the degradation at the output voltage. If the output ripple is too large, change a capacitor with less degradation effect or with higher rated voltage could be helpful.

POWER DISSIPATION

The maximum IC junction temperature should not be exceed 125°C under normal operating conditions. This restriction limits the power dissipation of the AW9962E. It is recommended to keep the actual dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined by using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{\theta_{ja}} \quad (8)$$

Where, T_{Jmax} is the Maximum Junction Temperature, T_A is the maximum ambient temperature for the application. θ_{ja} is the thermal resistance junction-to-ambient given in Power Dissipation Table.

The θ_{ja} of the DFN package greatly depends on the PCB layout and thermal pad connection. The thermal pad must be soldered directly to the analog ground on the PCB. After soldering, the PCB can be used as a heat sink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane, or alternatively, can be attached to a special heat sink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit(IC).

Using thermal vias underneath the thermal pad as illustrated in the layout example.

PCB LAYOUT CONSIDERATION

PCB layout is an important design step for those high frequency, high current switching power regulators in order to minimize noise and keep loop stable.

1. To reduce switching losses, it is better to make the SW pin rise and fall times as short as possible. Minimizing the length and area of all traces connected to the SW pin and using a ground plane under the switching regulator are strongly recommended to minimize inter-plane coupling.
2. The input and the output bypass capacitors should be placed as close to the IC as possible to get the best decoupling. The input and the output capacitor must not only be close to the VIN pin, but also to the GND pin in order to reduce the device supply ripple and keep loop stable.
3. Recommended to place IC, inductor, schottky diode, the input and output capacitor on the same layer.
4. The path of the inductor, schottky diode, the input and output capacitor should be kept as short as possible to minimize noise and ringing. Minimize trace lengths between the IC and the inductor, the diode, the input and the output capacitor; keep these traces short, direct, and wide.
5. FB is a sensitive node and it should be kept separate from the SW pin in the PCB layout.
6. Connect the exposed paddle to the PCB ground plane using at least two vias.

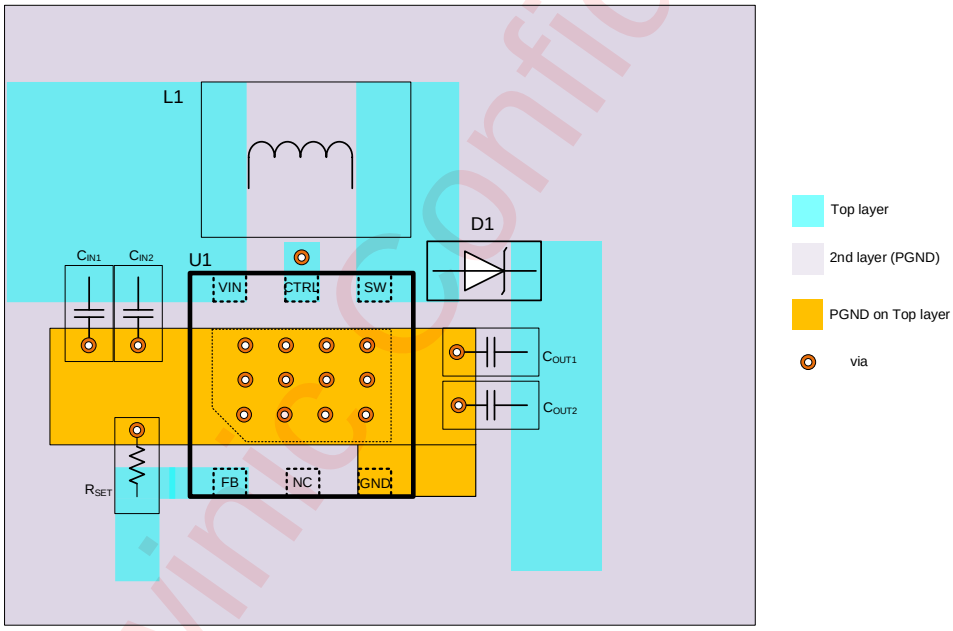
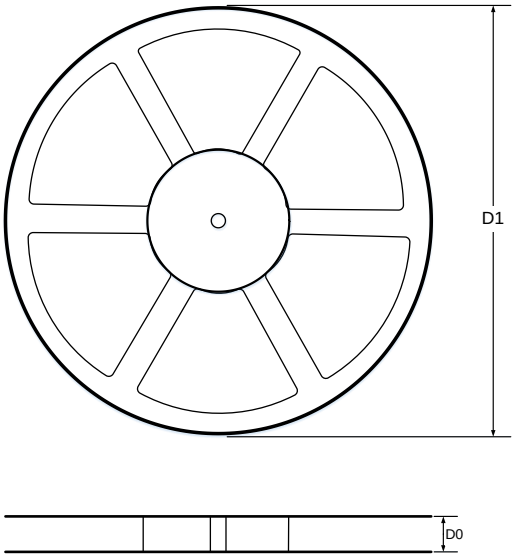


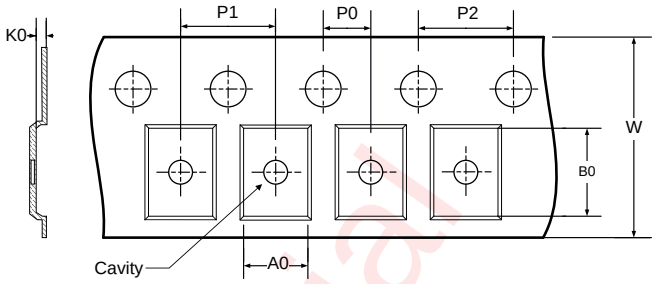
Figure 17 PCB Layout Reference

TAPE AND REEL INFORMATION

REEL DIMENSIONS

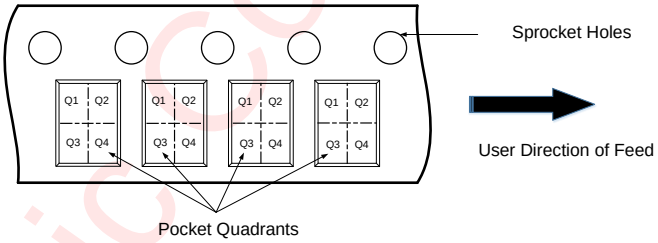


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D0：Reel width
D1：Reel diameter

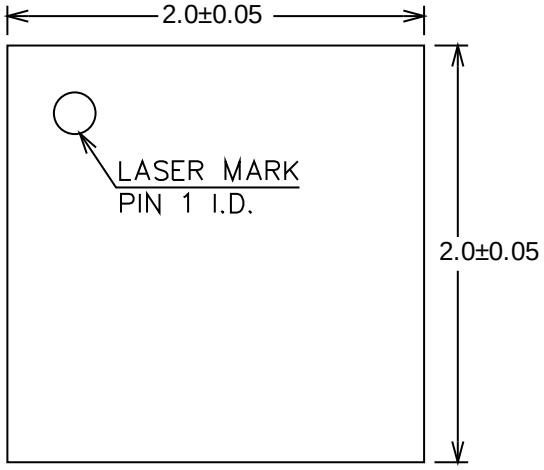
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All dimensions are nominal

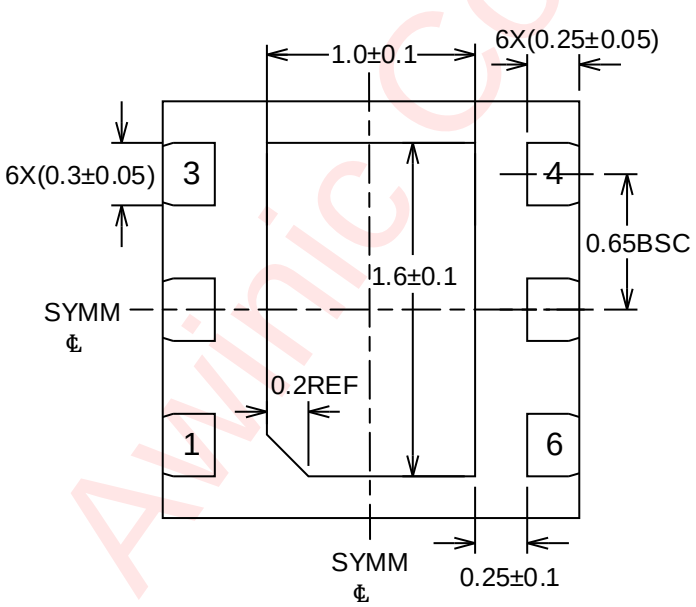
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2.3	2.3	1	2	4	4	8	Q1

PACKAGE DESCRIPTION

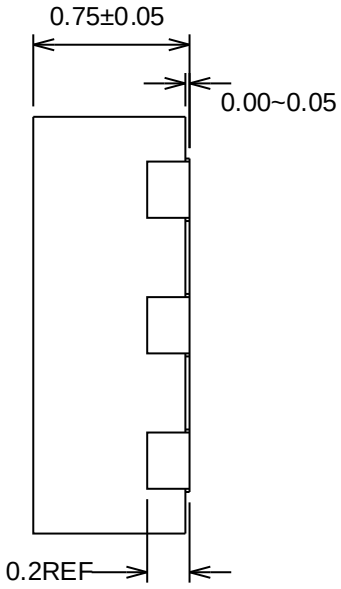


TOP VIEW

SIDE VIEW



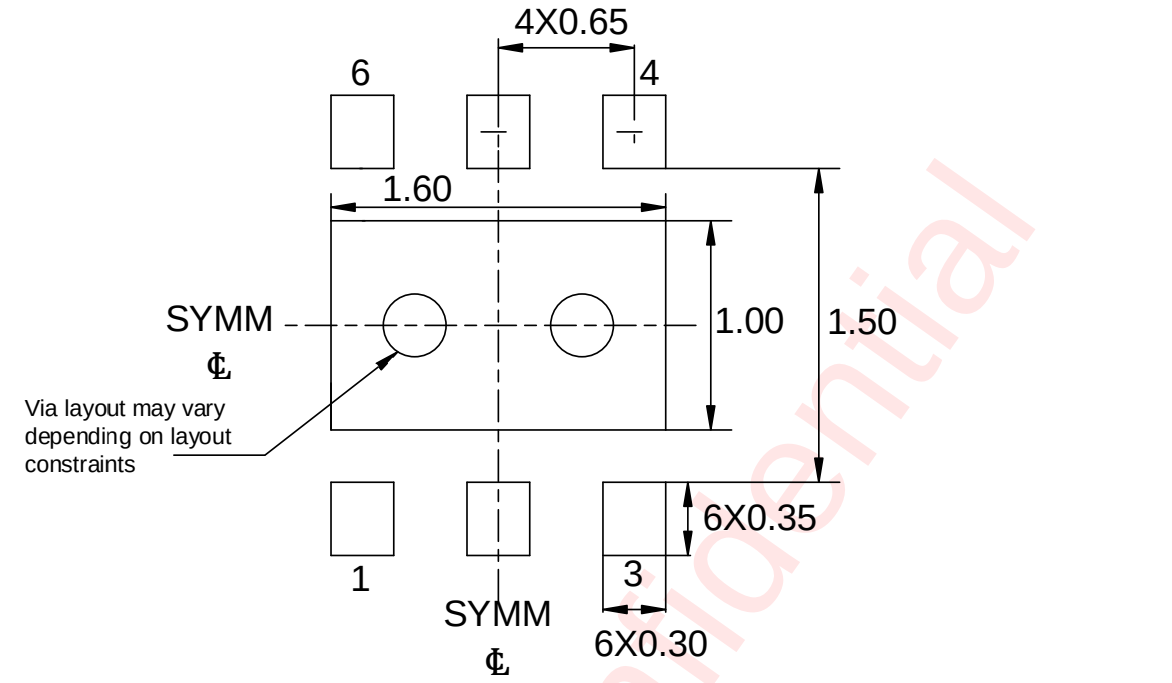
BOTTOM VIEW

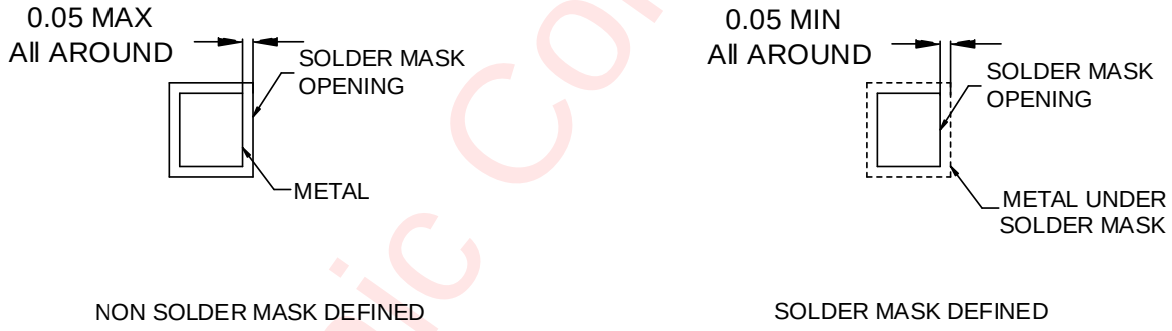


SIDE VIEW

Dimensions are all in millimeters

LAND PATTERN DATA





NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

Dimensions are all in millimeters

REVISION HISTORY

Vision	Date	Change Record
V1.0	Nov. 2017	Datasheet V1.0 Released
V1.1	Jun. 2018	Correct some mistake of description.
V1.2	Jan. 2019	Correct some mistake of description.
V1.3	Sep. 2020	Correct thermal resistance θ_{JA} and add thermal resistance θ_{JB}.
V1.4	Jul. 2023	Correct the formula of V_{FB} (Page 12).
V1.5	Nov. 2023	Update allowable error of PACKAGE DESCRIPTION (Page 18).
V1.6	Dec. 2023	1. Add High Input Voltage Application of AW9962E (Page 5); 2. Correct the description in PCB Layout Consideration (Page 16); 3. Add PCB Layout Reference (Page 16).
V1.7	Dec. 2024	1. Optimize General Description(Page 1). 2. Add optional component 'R_{OP}' to application circuit(Page 1)
V1.8	Feb. 2025	1. Revise typical value of V_{REF_PWM} under PWM=0.3% from 0.6 to 0.8 (Page 8)

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