



钜地半导体
Tudi Semiconductor

Product Specification

TL2842BP-TUDI

HIGH-PERFORMANCE CURRENT-MODE PWM CONTROLLERS

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**semiconductor device
manufacturer**

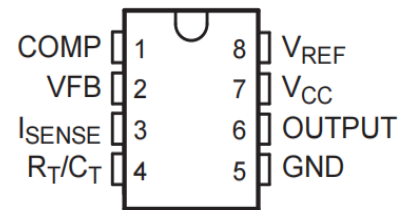
- Design
- research and development
- production
- and sales



FEATURES

- Low Start-Up Current ($<0.5\text{ mA}$)
- Trimmed Oscillator Discharge Current
- Current Mode Operation to 500 kHz
- Automatic Feed-Forward Compensation
- Latching PWM for Cycle-by-Cycle Current Limiting
- Internally Trimmed Reference With Undervoltage Lockout
- High-Current Totem-Pole Output Undervoltage Lockout With Hysteresis
- Double-Pulse Suppression

D (SOIC) OR P (PDIP) PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

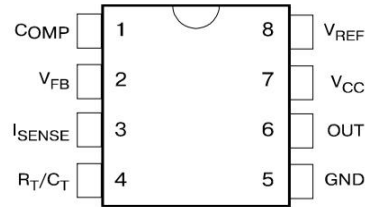
The TL284xB and TL384xB series of control integrated circuits provide the features that are necessary to implement off-line or dc-to-dc fixed-frequency current-mode control schemes, with a minimum number of external components. Internally implemented circuits include an undervoltage lockout (UVLO) and a precision reference that is trimmed for accuracy at the error amplifier input. Other internal circuits include logic to ensure latched operation, a pulse-width modulation (PWM) comparator that also provides current-limit control, and a totem-pole output stage designed to source or sink high-peak current. The output stage, suitable for driving n -channel MOSFETs, is low when it is in the off state.

The TL284xB and TL384xB series are pin compatible with the standard TL284x and TL384x with the following improvements.

Major differences between members of these series are the UVLO thresholds and maximum duty-cycle ranges. The TLx842B and TLx843B devices can operate to duty cycles approaching 100%. A duty-cycle range of 0% to 50% is obtained by the TLx844B and TLx845B by the addition of an internal toggle p-flop, which blanks the output off every other clock cycle. The TL284xB-series devices are characterized for operation from -40°C to 85°C . The TL384xB-series devices are characterized for operation from 0°C to 70°C .



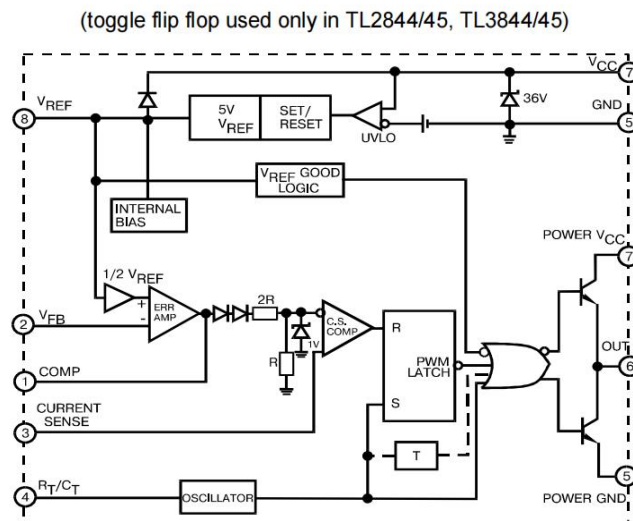
PIN CONNECTION (TOP VIEW)



PIN FUNCTION

N	FUNCTION	DESCRIPTION
1	COMP	This pin is the Error Amplifier output and is made for loop compensation.
2	V _{FB}	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	I _{SENSE}	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R _T /C _T	The oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R _T to V _{ref} and capacitor C _T to ground.
5	GROUND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sink by this pin.
7	V _{CC}	This pin is the positive supply of the integrated circuit.
8	V _{ref}	This is the reference output. It provides charging current for capacitor C _T through resistor R _T .

BLOCK DIAGRAM



Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Supply Voltage (low impedance source)	V _{CC}	30	V
Output Current	I _O	±1	A
Input Voltage (Analog Inputs pins 2,3)	V _I	-0.3 to 5.5	V
Error Amp Output Sink Current	I _{SINK (EA)}	10	mA
Power Dissipation (T _A =25°C)	P _O	1	W
Storage Temperature Range	T _{stg}	-65 to 150	°C
Lead Temperature (soldering 5 sec.)	T _L	260	°C



Electrical characteristics (* $V_{CC}=15V$, $R_T=10k\Omega$, $C_T=3.3nF$, $T_A=0^\circ C$ to $+70^\circ C$, unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Section						
Reference Output Voltage	V _{REF}	T _J = 25°C, I _{REF} = 1 mA	4.9	5.0	5.1	V
Line Regulation	ΔV _{REF}	12V ≤ V _{CC} ≤ 25 V		6.0	20	mV
Load Regulation	ΔV _{REF}	1 mA ≤ I _{REF} ≤ 20mA		6.0	25	
Short Circuit Output Current	I _{SC}	T _A = 25°C		-100	-180	mA
Oscillator Section						
Oscillation Frequency	f	T _J = 25°C	47	52	57	KHz
Frequency Change with Voltage	Δf/ΔV _{CC}	12V ≤ V _{CC} ≤ 25 V		0.05	1.0	%
Oscillator Amplitude	V _(OSC)	(peak to peak)		1.6		V
Error Amplifier Section						
Input Bias Current	I _{BIAS}	V _{FB} =3V		-0.1	-2	μA
Input Voltage	V _{I(EA)}	V _{pin1} = 2.5V	2.42	2.5	2.58	V
Open Loop Voltage Gain	A _{VOL}	2V ≤ V ₀ ≤ 4V	65	90		dB
Unity Gain Bandwidth	UGBW	T _J =25 ⁰ C, Note 3	0.5	0.6		MHz
Power Supply Rejection Ratio	PSRR	12V ≤ V _{CC} ≤ 25 V	60	70		dB
Output Sink Current	I _{SINK}	V _{pin2} = 2.7V, V _{pin1} = 1.1V	2	7		mA
Output Source Current	I _{SOURCE}	V _{pin2} = 2.3V, V _{pin1} = 5V	-0.5	-1.0		mA
High Output Voltage	V _{OH}	V _{pin2} = 2.3V, R _L = 15KΩ to GND	5.0	6.0		V
Low Output Voltage	V _{OL}	V _{pin2} = 2.7V, R _L = 15KΩ to PIN 8		0.8	1.1	
Current Sense Section						
Gain	G _V	(Note 1 & 2)	2.85	3.0	3.15	V/V
Maximum Input Signal	V _{I(MAX)}	V _{pin1} = 5V (Note1)	0.9	1.0	1.1	V
Supply Voltage Rejection	SVR	12V ≤ V _{CC} ≤ 25 V (Note 1)		70		dB
Input Bias Current	I _{BIAS}	V _{pin3} = 3V		-3.0	-10	μA
Output Section						
Low Output Voltage	V _{OL}	I _{SINK} = 20 mA		0.08	0.4	V
		I _{SINK} = 200 mA		1.4	2.2	
High Output Voltage	V _{OH}	I _{SINK} = 20 mA	13	13.5		
		I _{SINK} = 200 mA	12	13.0		
Rise Time	t _R	T _J = 25°C, C _L = 1nF (Note 3)		45	150	nS
Fall Time	t _F	T _J = 25°C, C _L = 1nF (Note 3)		35	150	
Undervoltage Lockout Section						
Start Theshold	V _{TH(ST)}	TL2842/44,TL3842/44	14.5	16.0	17.5	V
		TL2843/45,TL3843/45	7.8	8.4	9.0	
Min. Operating Voltage (After Turn On)	V _{OPR(min)}	TL2842/44,TL3842/44	8.5	10	11.5	V
		TL2843/45,TL3843/45	7.0	7.6	8.2	
PWM Section						
Max. Duty Cycle	D _(MAX)	TL2842/43,TL3842/43	95	97	100	%
		TL2844/45,TL3844/45	47	48	50	
Min. Duty Cycle	D _(MAX)				0	
Total Standby Current						
Start-Up Current	I _{ST}	TL3842/43/44/45		0.17	0.3	mA
Operating Supply Current	I _{CC (OPR)}	V _{pin3} = V _{pin2} = 0V		13	17	
Zener Voltage	V _Z	I _{CC} =25 mA	30	38		V

* Adjust V_{CC} above the start threshold before setting it to 15V.

Note 1: Parameter measured at trip point of latch with $V_{pin2}=0$.

Note 2: Gain defined as $A=\Delta V_{pin1}/\Delta V_{pin3}$; $0 \leq V_{pin3} \leq 0.8V$.

Note 3: These parameters, although guaranteed, are not 100% tested in production.



APPLICATION INFORMATION

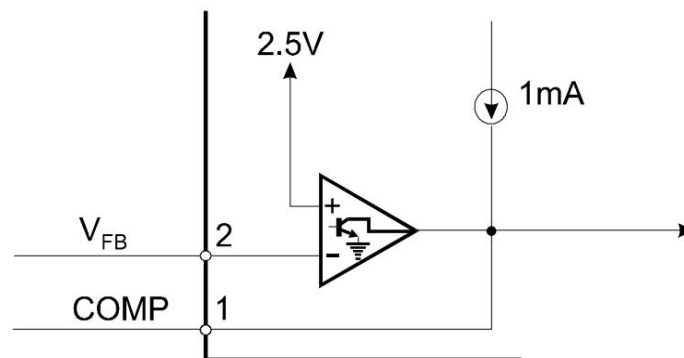
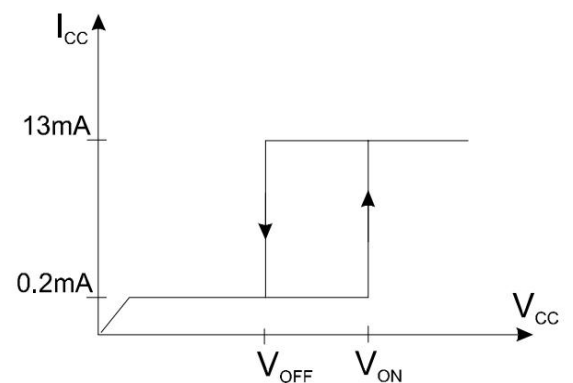
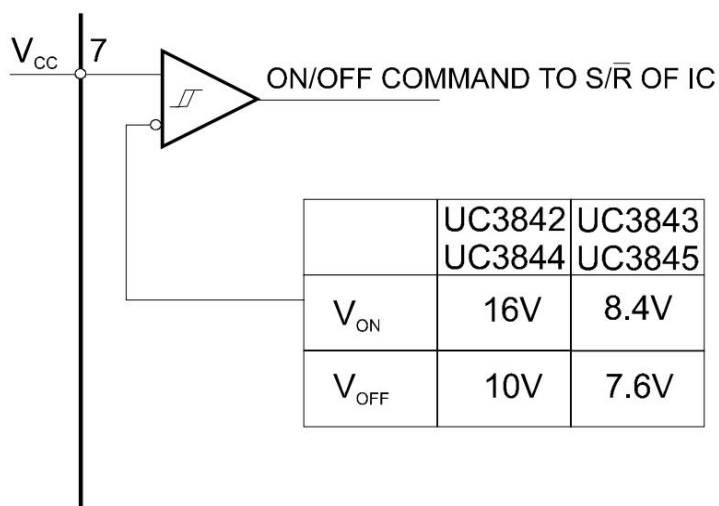
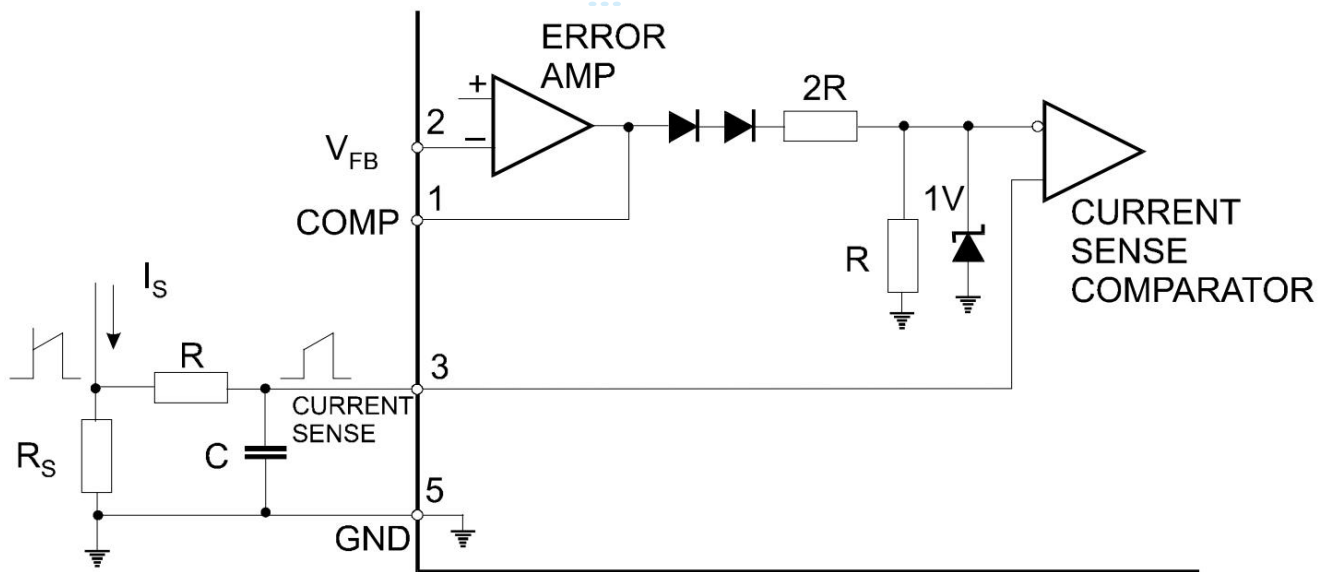


Figure 1. Error Amp Configuration



During UVLO, the Output is low

Figure 2. Under voltage Lockout



Peak current is determined by $I_{S \max} \approx \frac{1.0V}{R_S}$

Figure 3. Current Sense Circuit

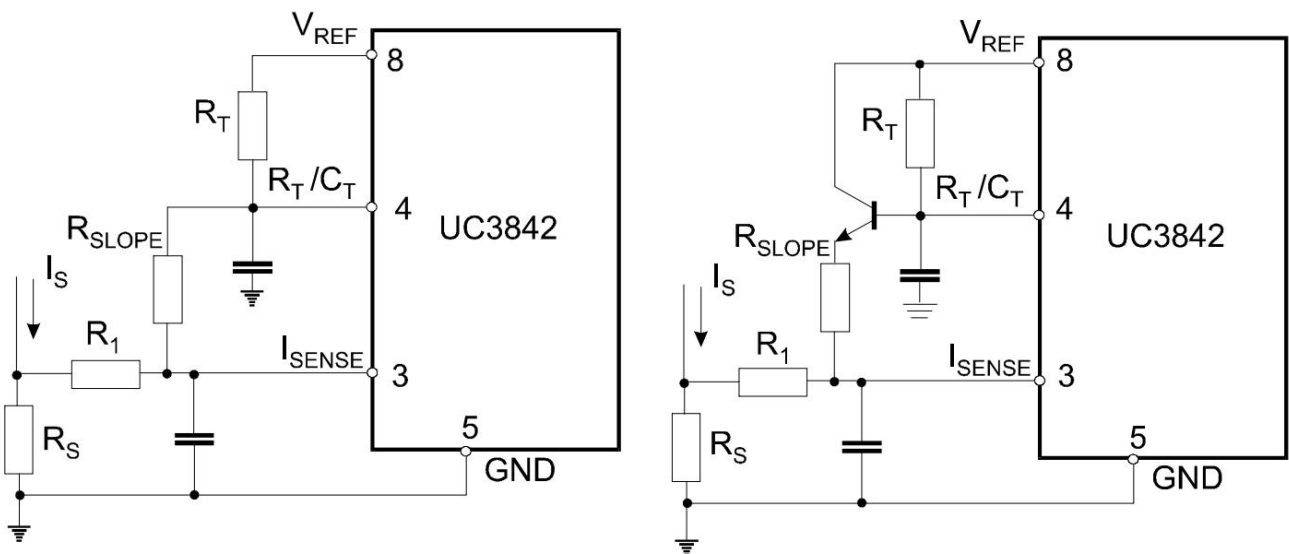
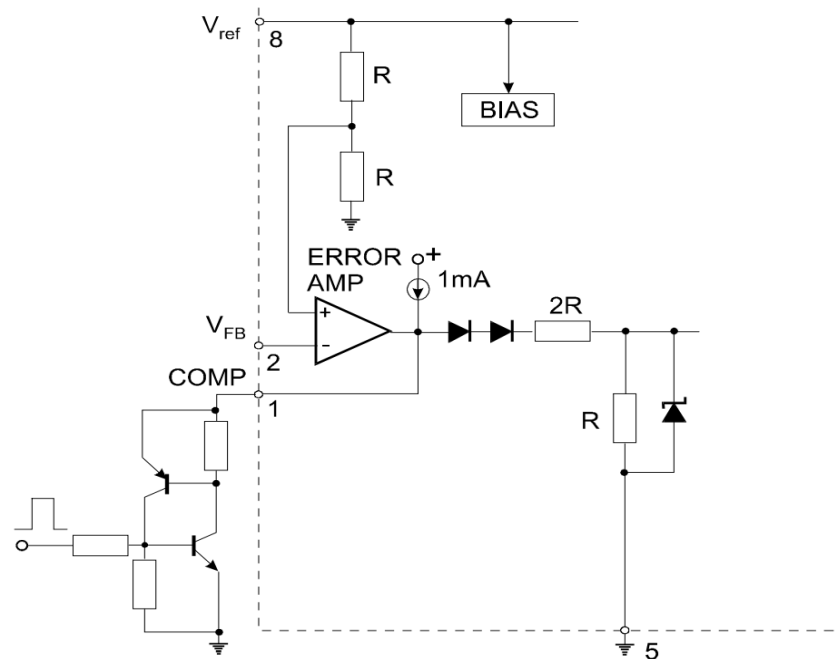
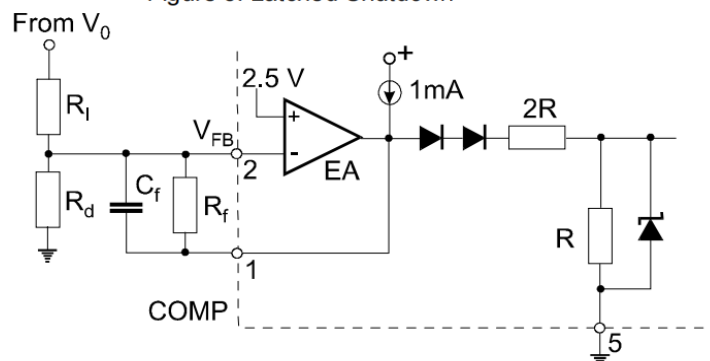


Figure 4. Slope Compensation Techniques

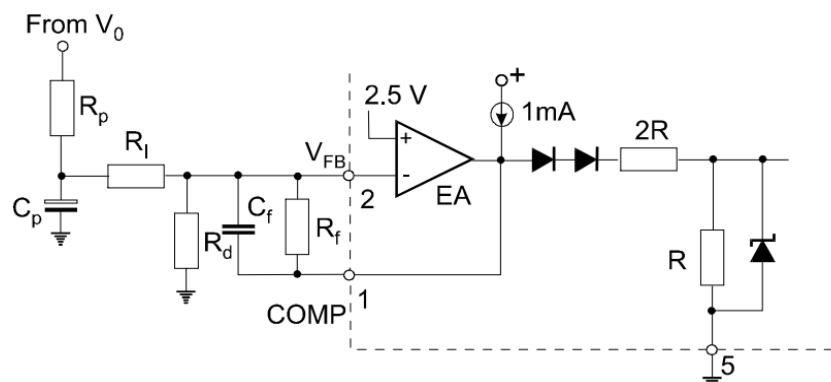


SCR must be selected for a holding current of less than 0.5mA.
The simple two transistor circuit can be used in place of the SCR as shown.

Figure 5. Latched Shutdown



Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

Figure 6. Error Amplifier Compensation

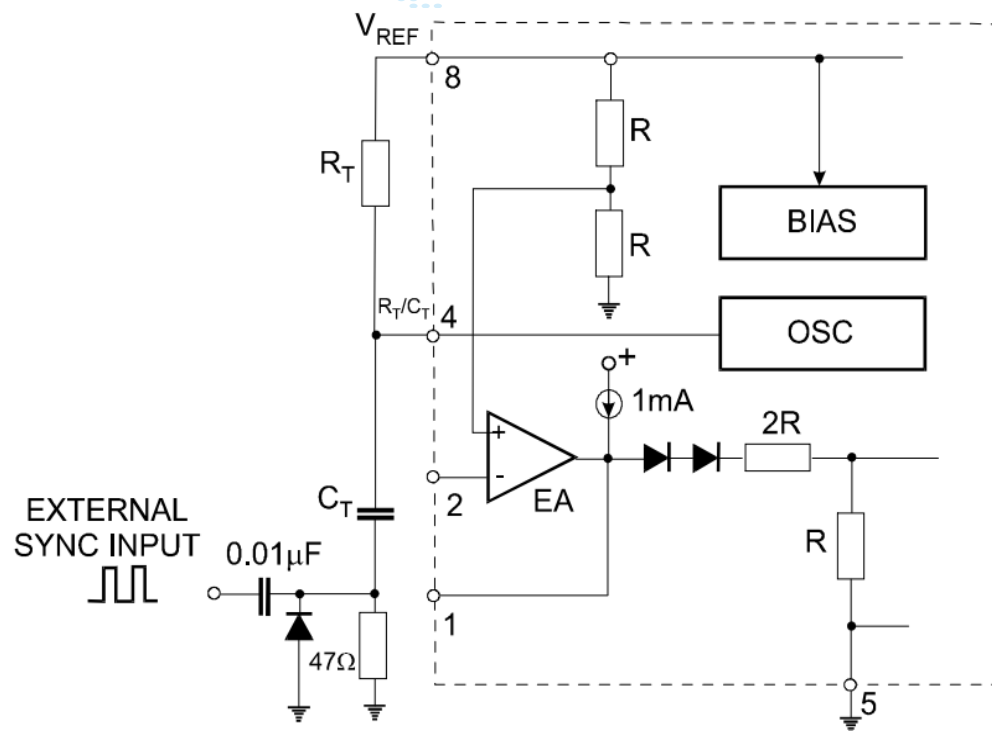


Figure 7. External Clock Synchronization

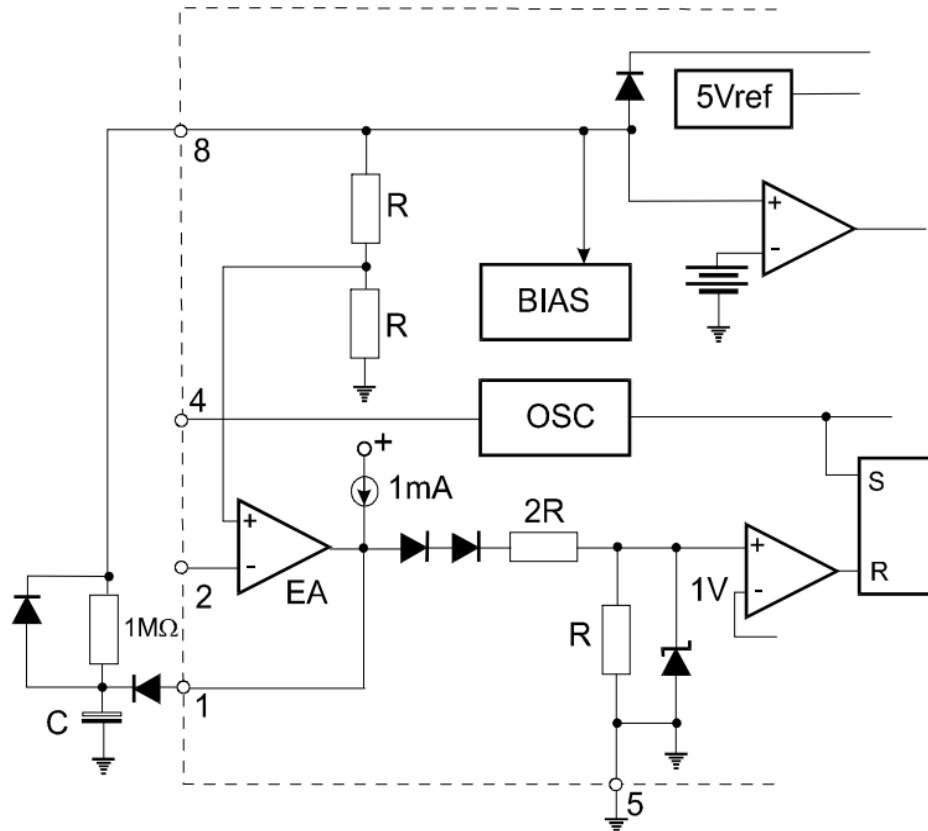


Figure 8. Soft-Start Circuit



TYPICAL PERFORMANCE CHARACTERISTICS

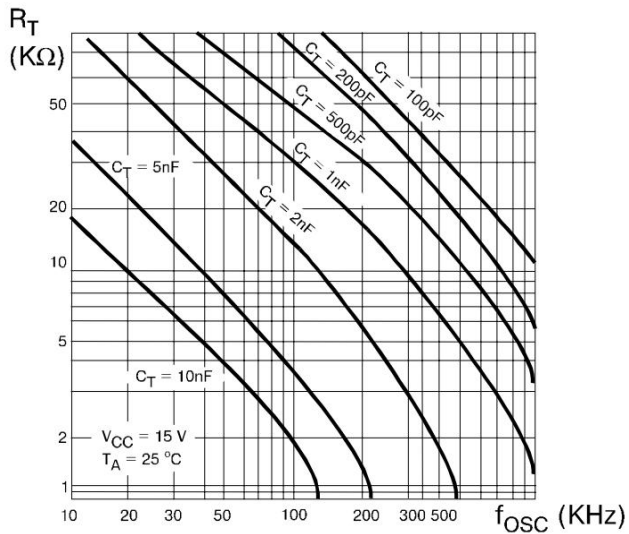


Figure 1. Timing Resistor vs. Oscillator Frequency

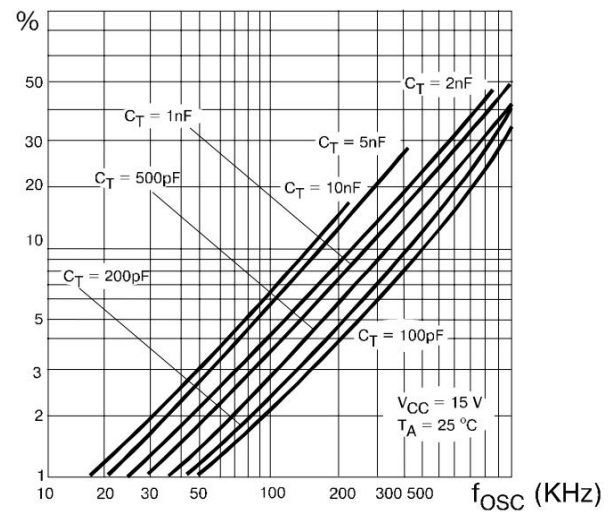


Figure 2. Output Dead-Time vs. Oscillator Frequency

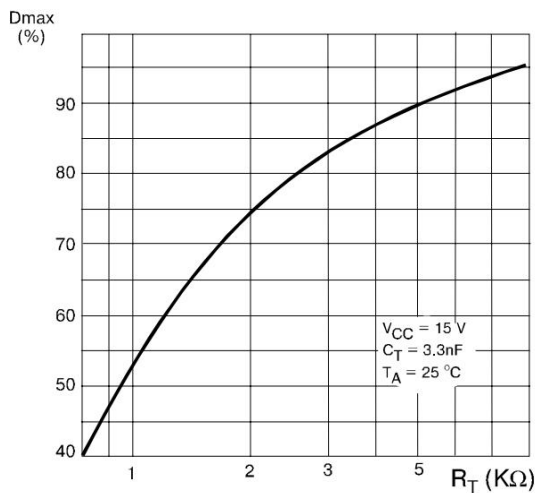


Figure 3. Maximum Output Duty Cycle vs. Timing Resistor (TL3842/43)

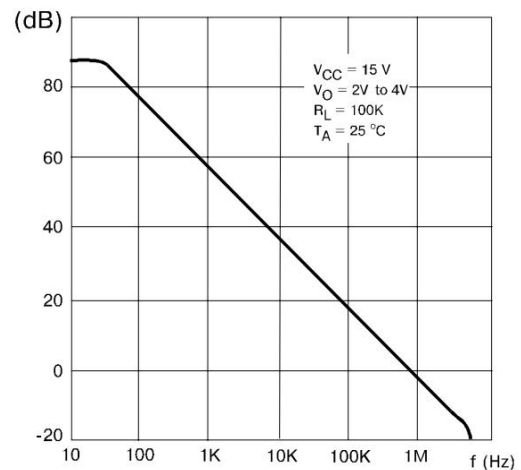


Figure 4. Error Amp Open-Loop Gain vs. Frequency

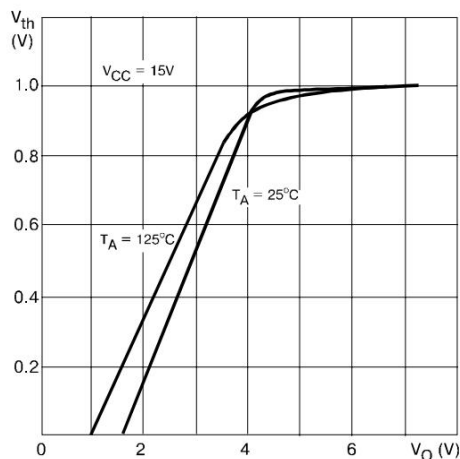


Figure 5. Current Sense Input Threshold vs. Error Amp Output Voltage

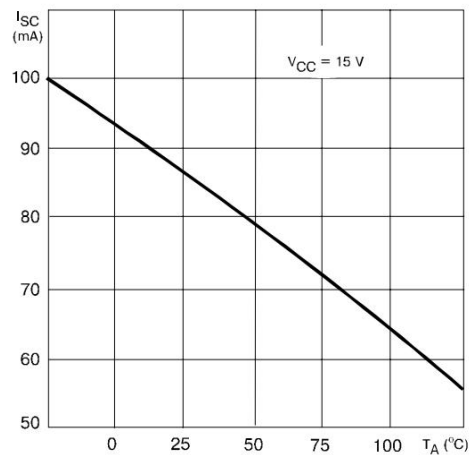


Figure 6. Reference Short Circuit Current vs. Temperature

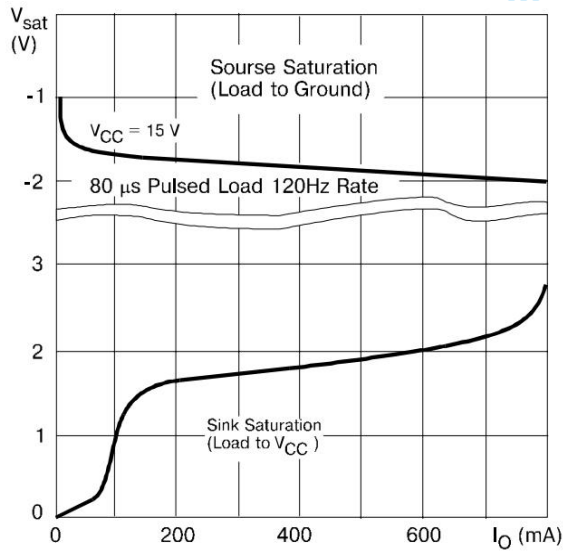


Figure 7. Output Saturation Voltage vs. Load Current
 $T_A = 25^\circ\text{C}$

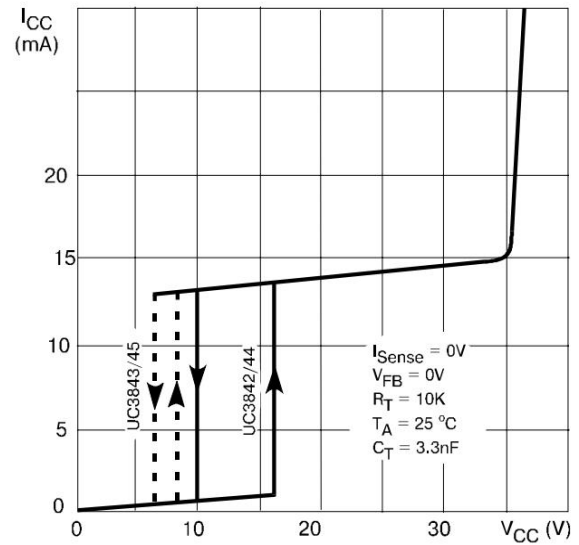


Figure 8. Supply Current vs. Supply Voltage

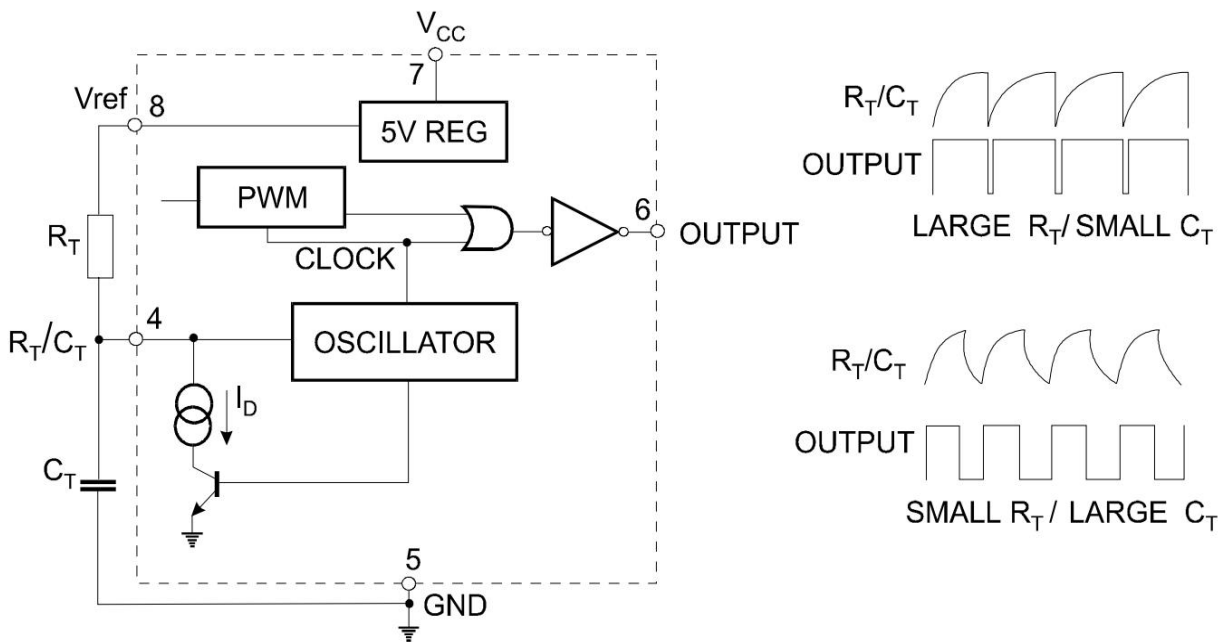


Figure 9. Oscillator and Output Waveforms

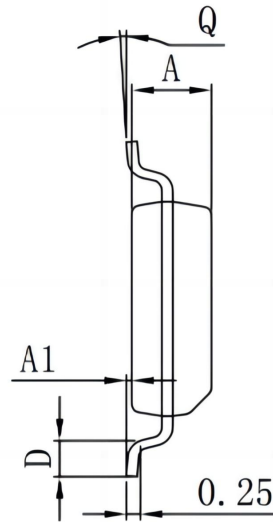
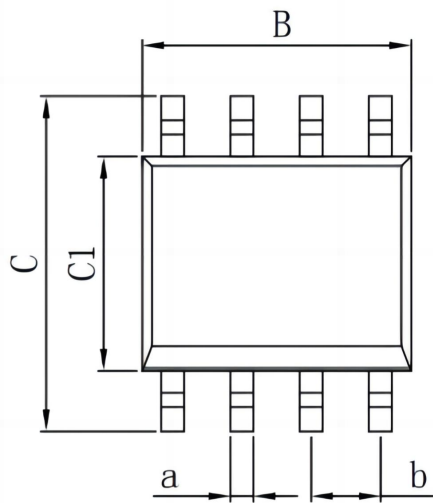
Ordering information

Order Number	Package	Package Quantity	Marking On The park
TL2842BP-TUDI	DIP8	Tube,50,A box of 2000	TL2842BP



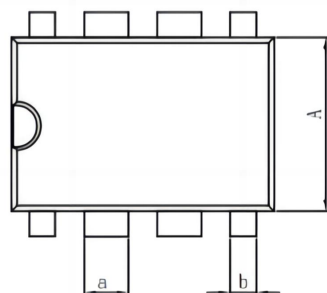
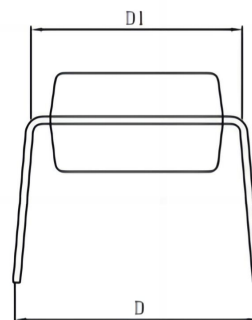
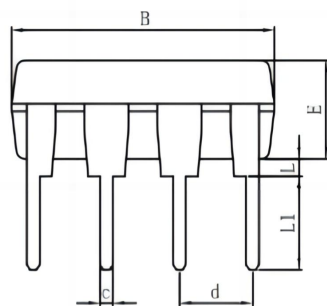
PACKAGE

SOP8



Dimensions In Millimeters					
Symbol :	Min :	Max :	Symbol :	Min :	Max :
A	1.225	1.570	D	0.400	0.950
A1	0.100	0.250	Q	0°	8°
B	4.800	5.100	a	0.420 TYP	
C	5.800	6.250	b	1.270 TYP	
C1	3.800	4.000			

DIP8



Dimensions In Millimeters					
Symbol :	Min :	Max :	Symbol :	Min :	Max :
A	6.100	6.680	L1	3.000	3.600
B	9.000	9.500	a	1.524 TYP	
D	8.400	9.000	b	0.889 TYP	
D1	7.420	7.820	c	0.457 TYP	
E	3.100	3.550	d	2.540 TYP	
L	0.500	0.700			



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