



钜地半导体  
Tudi Semiconductor

## Product Specification

CAT25M01VI-GT3-TUDI

SPI Serial EEPROM 1-Mbit(131072\*8)

网址 [www.sztdbdt.com](http://www.sztdbdt.com)

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## Features

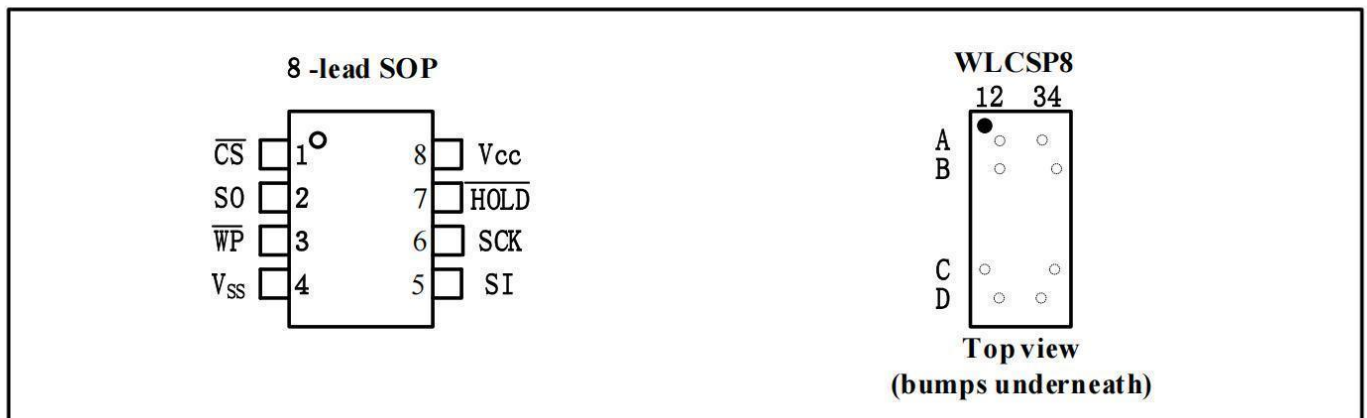
- Serial Peripheral Interface (SPI) Compatible
- Datasheet describes Mode 0 operation
- Low-voltage operation
  - $V_{CC} = 2.8V$  to  $5.5V$
- 256-byte Page Mode and Byte Write operation supported
- Block Write protection
- CAT25M01 = 5MHZ  
AT25M01 = 1MHZ/5MHZ
  - Protect  $\frac{1}{4}$ ,  $\frac{1}{2}$ , or entire array
- Write Protect ( $\overline{WP}$ ) pin and Write Disable instructions for both hardware and software data protection
- Self-timed write cycle (8ms max)
- High-reliability
  - Endurance: 1,000,000 write cycles
  - Data retention: 100 years
- Green package options (Pb/Halide-free/RoHS compliant)
- 8-lead JEDEC SOIC, 8-lead EIAJ SOIC, and 8-ball WLCSP

## Description

The AT25M01 /CAT25M01 provides 1,048,576 bits of Serial Electrically Erasable

Programmable Read-Only Memory (EEPROM) organized as 131,072 words of eight bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential.

## Pin Configuration





Additional package types that are not listed below may be available for order. Please contact Atmel for availability details.

| Atmel Ordering Code <sup>(1)</sup> | Lead Finish                        | Package    | Voltage      | Operation Range                           |
|------------------------------------|------------------------------------|------------|--------------|-------------------------------------------|
| AT25M01-SSHM-T-TUDI                | NiPdAu<br>(Lead-free/Halogen-free) | 8S1        | 2.8V to 5.5V | Industrial Temperature<br>(−10°C to 85°C) |
| CAT25M01VI-GT3-TUDI                |                                    | 8S2        |              |                                           |
| AT25M01-SHM-B-TUDI                 |                                    |            |              |                                           |
| AT25M01-SHM-T-TUDI                 |                                    |            |              |                                           |
| AT25M01-UUM-T-TUDI                 | SnAgCu<br>(Lead-free/Halogen-free) | 8U-7       |              |                                           |
| AT25M01-WWU11M-TUDI                | —                                  | Wafer Sale |              |                                           |

- Note:
- Consistent with the general semiconductor market trend, Atmel will supply devices with either gold or copper bond wires to increase manufacturing flexibility and ensure a long-term continuity of supply. There is no difference in product quality, reliability, or performance between the two variations.
  - B = Bulk delivery in tubes:
    - JEDEC SOIC = 100 units per tube
    - EIAJ SOIC = 95 units per tube
  - T = Tape and reel delivery:
    - JEDEC SOIC = 4k per reel
    - EIAJ SOIC = 2k per reel
    - WLCSP = 5k per reel
  - Contact Atmel for availability.

| Package Type |                                                                   |
|--------------|-------------------------------------------------------------------|
| <b>8S1</b>   | 8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC) |
| <b>8S2</b>   | 8-lead, 0.208" wide, Plastic Small Package Outline (EIAJ SOIC)    |
| <b>8U-7</b>  | 8-ball, Wafer Level Chip Scale Package (WLCSP)                    |

## Pin Descriptions

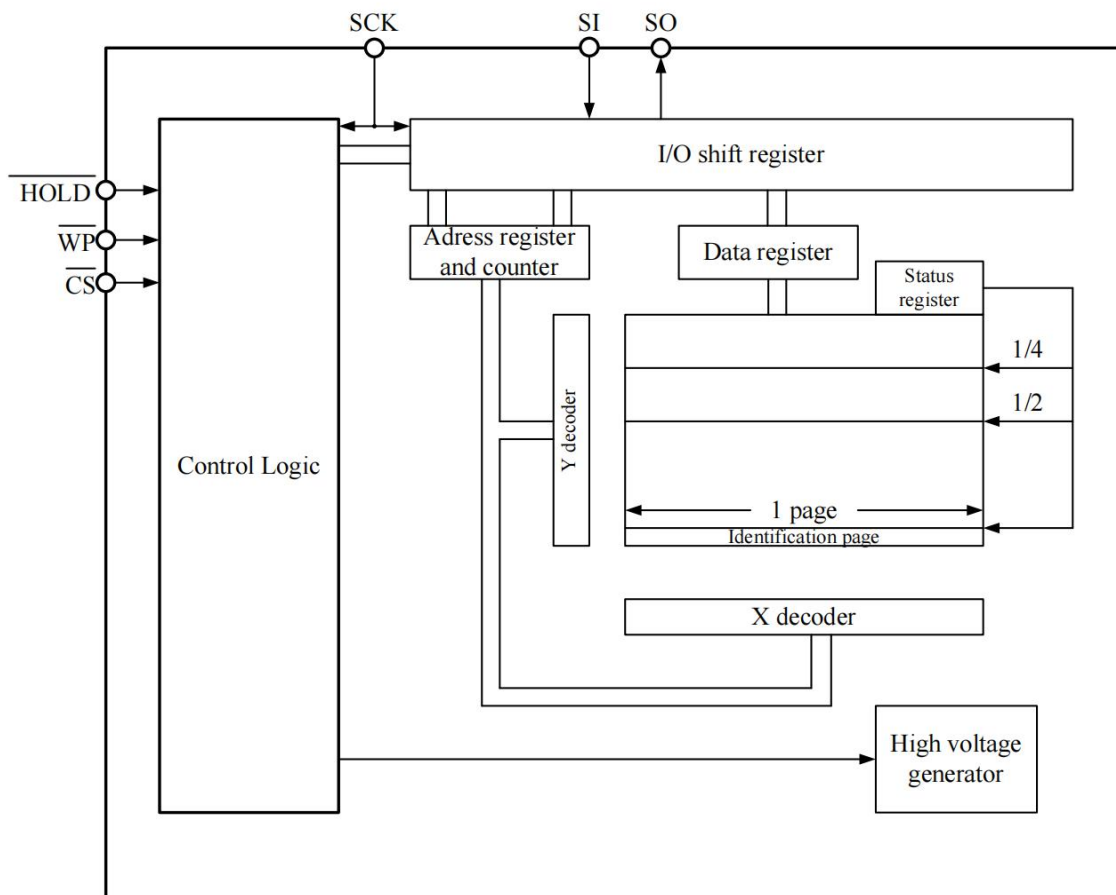
| Pin Name          | Type | Functions          |
|-------------------|------|--------------------|
| $\overline{CS}$   | I    | Chip Select        |
| SO                | O    | Serial Data Output |
| $\overline{WP}$   | I    | Write Protect      |
| $V_{SS}$          | P    | Ground             |
| $V_{CC}$          | P    | Power Supply       |
| $\overline{HOLD}$ | I    | Hold               |
| SCK               | I    | Serial Clock       |
| SI                | I    | Serial Data Input  |

Table 1

| Position | A                      | B                        | C                      | D               |
|----------|------------------------|--------------------------|------------------------|-----------------|
| 1        | -                      | -                        | SCK                    | -               |
| 2        | V <sub>CC</sub>        | $\overline{\text{HOLD}}$ | -                      | SI              |
| 3        | $\overline{\text{CS}}$ | -                        | -                      | V <sub>SS</sub> |
| 4        | -                      | SO                       | $\overline{\text{WP}}$ | -               |

Table 2

## Block Diagram







#### Serial Data Input (SI):

The SPI Serial data input (SI) is used to serially receive write instructions, addresses or data to the device on the rising edge of the Serial Clock (SCK) input pin.

Serial Data Output (SO): The SPI Serial data output (SO) is used to read data or status from the device on the falling edge of CLK.

Serial Clock (SCK): The SPI Serial Clock Input (SCK) pin provides the timing for serial input and output operations.

Chip Select ( $\overline{CS}$ ): The SPI Chip Select ( $\overline{CS}$ ) pin enables and disables device operation. When ( $\overline{CS}$ ) is high, the device is deselected and the Serial Data Output (SO) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal write cycle is in progress. When ( $\overline{CS}$ ) is brought low, the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, ( $\overline{CS}$ ) must transition from high to low before a new instruction will be accepted.

Hold ( $\overline{HOLD}$ ): The  $\overline{HOLD}$  pin allows the device to be paused while it is actively selected. When  $\overline{HOLD}$  is brought low, while  $\overline{CS}$  is low, the SO pin will be at high impedance and signals on the SI and SCK pins will be ignored (don't care). When  $\overline{HOLD}$  is brought high, device operation can resume. The  $\overline{HOLD}$  function can be useful when multiple devices are sharing the same SPI signals. The  $\overline{HOLD}$  pin is active low.

Write Protect ( $\overline{WP}$ ): The Write Protect ( $\overline{WP}$ ) pin is used in conjunction with the Status Register Write Disable (SRWD) Bit to prevent the Status Registers from being written. Write Protect ( $\overline{WP}$ ) pin and Status Register Write Disable (SRWD) Bit enable the device to be put in the Hardware Protected mode (when Status Register Write Disable (SRWD) Bit is set to 1, and Write Protect ( $\overline{WP}$ ) pin is driven low).

## Functional Description

The 25M01 device supports the Serial Peripheral Interface (SPI) bus protocol, modes (0,0) and (1,1). The device contains an 8-bit instruction register. The instruction set and associated op-codes are listed in Table 3.

Reading data stored in the 25M01 is accomplished by simply providing the READ command and an address. Writing to the 25M01, in addition to a WRITE command, address and data, also requires enabling the device for writing by first setting certain bits in a Status Register, as will be explained later.

After a high to low transition on the  $\overline{CS}$  input pin, the 25M01 will accept any one of the six instruction op-codes listed in Table 3 and will ignore all other possible 8-bit combinations. The communication protocol follows the timing from Figure 14.

The 25M01 features an additional Identification Page (256 bytes) which can be accessed for Read and Write operations when the IPL bit from the Status Register is set to "1". The user can also choose to make the Identification Page permanent write protected by setting the LIP bit from the Status Register (LIP= "1").

| Instruction | Opcode    | Operation                                       |
|-------------|-----------|-------------------------------------------------|
| WREN        | 0000 0110 | Enable Write Operations                         |
| WRDI        | 0000 0100 | Disable Write Operations                        |
| RDSR        | 0000 0101 | Read Status Register                            |
| WRSR        | 0000 0001 | Write Status Register                           |
| READ        | 0000 0011 | Read Data from Memory                           |
| WRITE       | 0000 0010 | Write Data to Memory                            |
| RDID        | 1000 0011 | Read identification page                        |
| WRID        | 1000 0010 | Write identification page                       |
| RDLS        | 1000 0011 | Reads the identification page lock status       |
| LID         | 1000 0010 | Locks the identification page in read-only mode |

Table 3



## 1. Status Register

The Status Register, as shown in Table 4, contains a number of status and control bits.

|      |   |   |   |     |     |     |       |
|------|---|---|---|-----|-----|-----|-------|
| 7    | 6 | 5 | 4 | 3   | 2   | 1   | 0     |
| SRWD | 0 | 0 | 0 | BP1 | BP0 | WEL | READY |

Table 4

**READY:** The **READY** bit indicates whether the device is busy with a write operation. This bit is automatically set to 1 during an internal write cycle, and reset to 0 when the device is ready to accept commands. For the host, this bit is read only.

**BP0, BP1:** The BP0 and BP1 (Block Protect) bits determine which blocks are currently write protected. They are set by the user with the WRSR command and are non-volatile. The user is allowed to protect a quarter, one half or the entire memory, by setting these bits according to Table 5. The protected blocks then become read-only.

| Status Register Bits |     | Array Address Protected | Protection               |
|----------------------|-----|-------------------------|--------------------------|
| BP1                  | BP0 |                         |                          |
| 0                    | 0   | None                    | No Protection            |
| 0                    | 1   | 18000h–1FFFFh           | Quarter Array Protection |
| 1                    | 0   | 10000h–1FFFFh           | Half Array Protection    |
| 1                    | 1   | 00000h–1FFFFh           | Full Array Protection    |

Table 5

**SRWD:** The SRWD (Status Register Write Disable) bit acts as an enable for the  $\overline{WP}$  pin. Hardware write protection is enabled when the  $\overline{WP}$  pin is low and the SRWD bit is 1. This condition prevents writing to the status register and to the block protected sections of memory. While hardware write protection is active, only the non-block protected memory can be written. Hardware write protection is disabled when the  $\overline{WP}$  pin is high or the SRWD bit is 0. The SRWD bit,  $\overline{WP}$  pin and WEL bit combine to either permit or inhibit Write operations, as detailed in Table 6.

| SRWD | WP   | WEL | Protected Blocks | Unprotected Blocks | Status Register |
|------|------|-----|------------------|--------------------|-----------------|
| 0    | X    | 0   | Protected        | Protected          | Protected       |
| 0    | X    | 1   | Protected        | Writable           | Writable        |
| 1    | Low  | 0   | Protected        | Protected          | Protected       |
| 1    | Low  | 1   | Protected        | Writable           | Protected       |
| X    | High | 0   | Protected        | Protected          | Protected       |
| X    | High | 1   | Protected        | Writable           | Writable        |

Table 6

## 2. Write Operations

The 25M01 device powers up into a write disable state. The device contains a Write Enable Latch (WEL) which must be set before attempting to write to the memory array or to the status register. In addition, the address of the memory location(s) to be written must be outside the protected area, as defined by BP0 and BP1 bits from the status register.

**Write Enable and Write Disable:** The internal Write Enable Latch and the corresponding Status Register WEL





bit are set by sending the WREN instruction to the 25M01. Care must be taken to take the  $\overline{CS}$  input high after the WREN instruction, as otherwise the Write Enable Latch will not be properly set. WREN timing is illustrated in Figure 2. The WREN instruction must be sent prior to any WRITE or WRSR instruction.

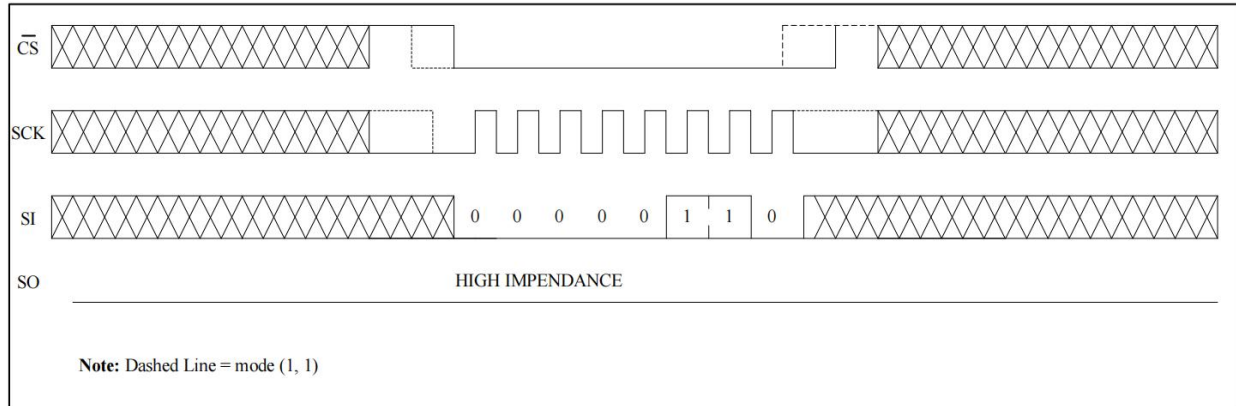


Figure 2

The internal write enable latch is reset by sending the WRDI instruction as shown in Figure 3. Disabling write operations by resetting the WEL bit, will protect the device against inadvertent writes.

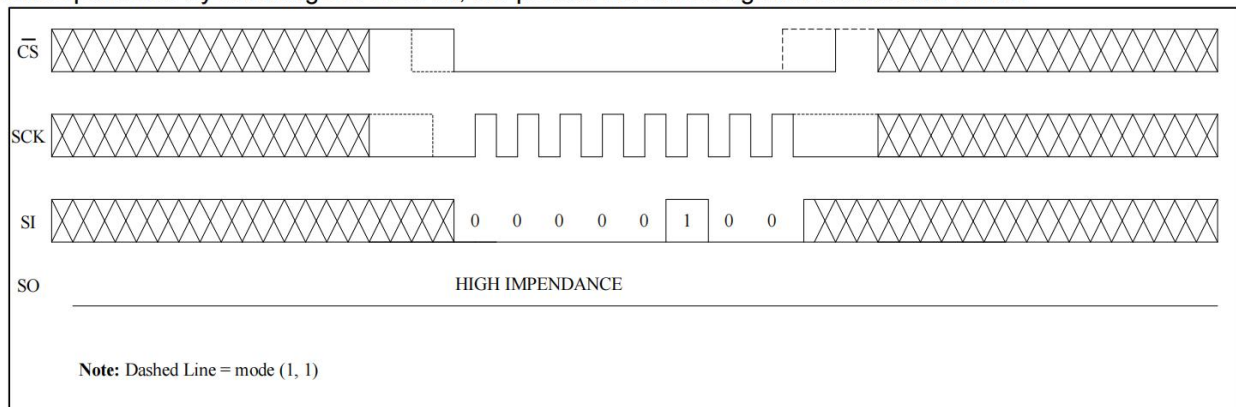


Figure 3

**Byte Write:** Once the WEL bit is set, the user may execute a write sequence, by sending a WRITE instruction, a 24-bit address and a data byte as shown in Figure 4. Only 17 significant address bits are used by the 25M01. The rest are don't care bits, as shown in Table 7. Internal programming will start after the low to high  $\overline{CS}$  transition. During an internal write cycle, all commands, except for RDSR (Read Status Register) will be ignored. The  $\overline{READY}$  bit will indicate if the internal write cycle is in progress ( $\overline{READY}$  high), or the device is ready to accept commands ( $\overline{READY}$  low).

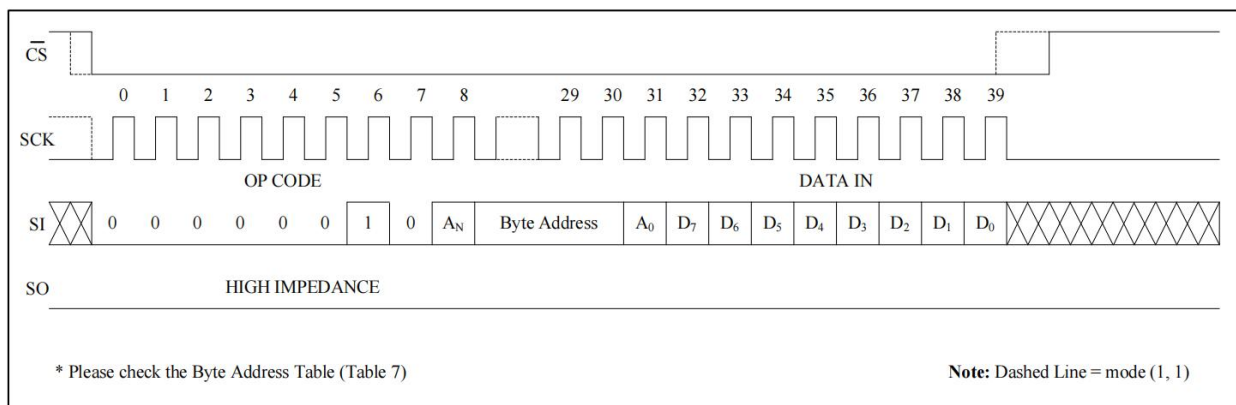


Figure 4



**Page Write:** After sending the first data byte to the 25M01, the host may continue sending data, up to a total of 256 bytes, according to timing shown in Figure 5. After each data byte, the lower order address bits are automatically incremented, while the higher order address bits (page address) remain unchanged. If during this process the end of page is exceeded, then loading will “roll over” to the first byte in the page, thus possibly overwriting previously loaded data. Following completion of the write cycle, the 25M01 is automatically returned to the write disable state.

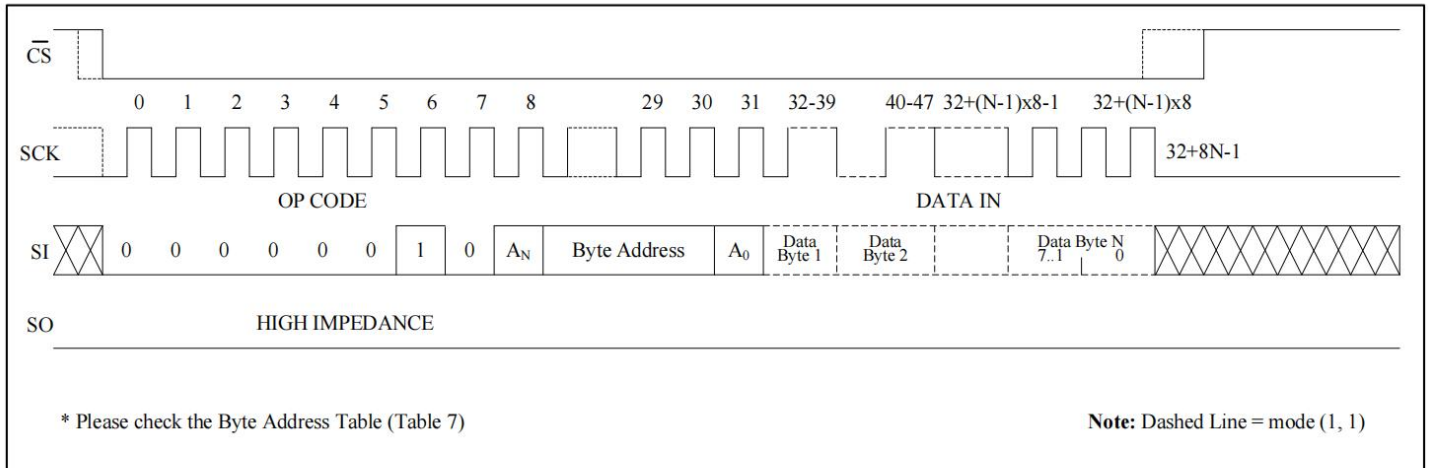


Figure 5

**Write Identification Page:** The additional 256-byte Identification Page (IP) (256 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. Writing this page is achieved with the Write Identification Page instruction, according to timing shown in Figure 6. Address bit A10 must be 0, upper address bits are Don't Care, the lower address bits [A7:A0] address bits define the byte address inside the identification page. The byte address must not exceed the 256-byte page boundary.

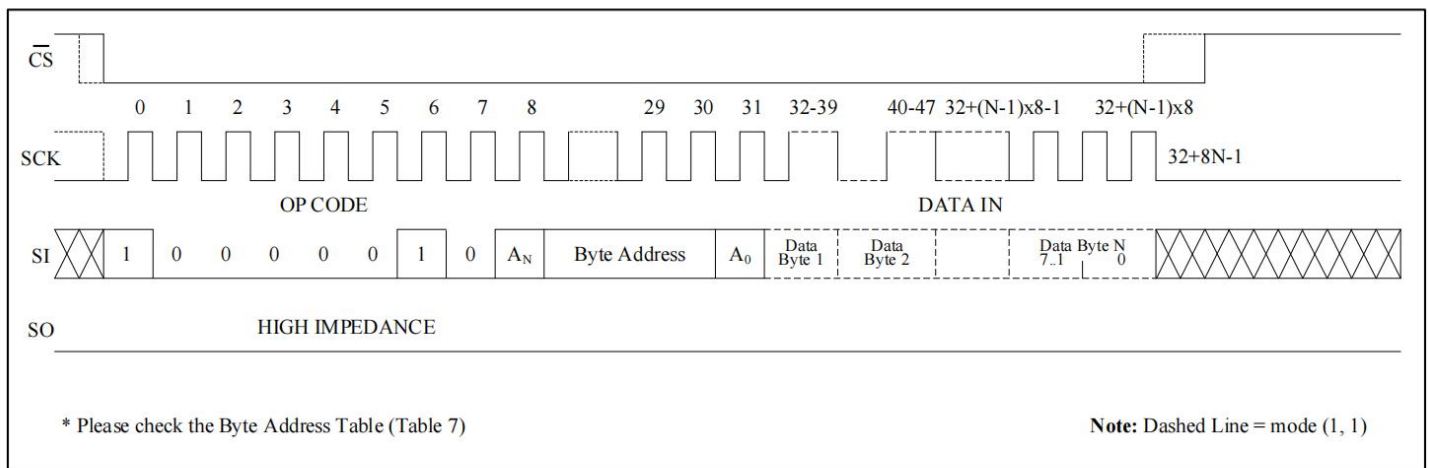


Figure 6

| Device              | Address Significant Bits | Address Don't Care Bits | # Address Clock Pulses |
|---------------------|--------------------------|-------------------------|------------------------|
| Main Memory Array   | A16 – A0                 | A23 – A17               | 24                     |
| Identification Page | A7 – A0                  | A23 – A8                | 24                     |

Table 7





**Write Status Register:** The Status Register is written by sending a WRSR instruction according to timing shown in Figure 6. Only bits 2, 3, 4, 5, 6 and 7 can be written using the WRSR command.

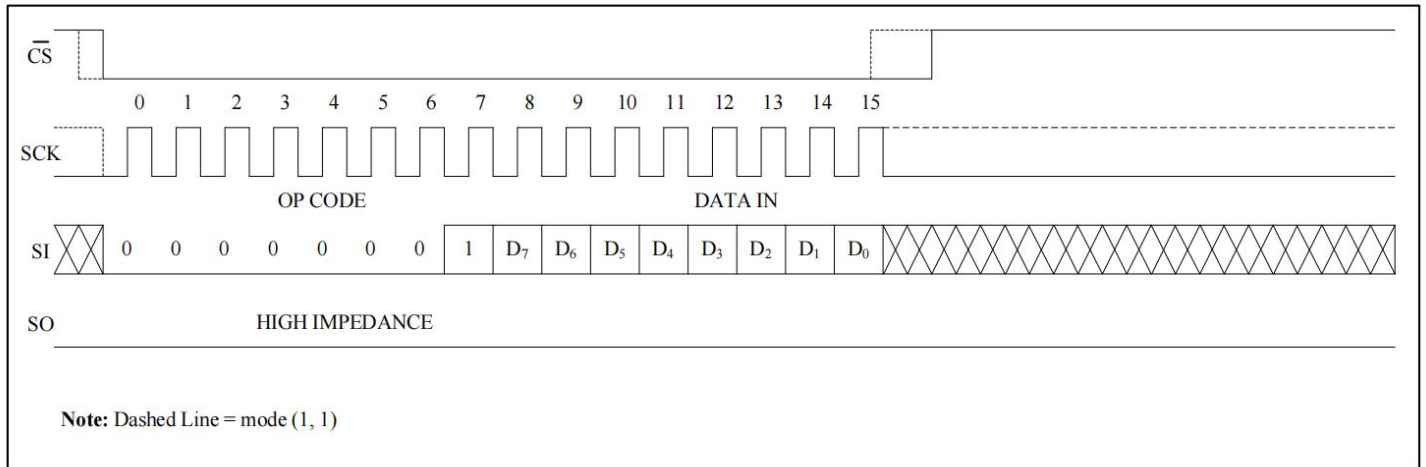


Figure 7

**Lock Identification Page:** The Lock ID instruction permanently locks the Identification Page in read-only mode. Before this instruction can be accepted, a Write Enable (WREN) instruction must have been executed. Lock Identification page is achieved with the Write Identification Page instruction, according to timing shown in Figure 8. Address bit A10 must be 1, all other address bits are Don't Care. The data bit1 must be "1", other bits don't care.

The instruction is discarded, and is not executed, under the following conditions:

- If a Write cycle is already in progress,
- If the Block Protect bits (BP1, BP0) = (1, 1),
- If a rising edge on Chip Select (CS) happens outside of a byte boundary.

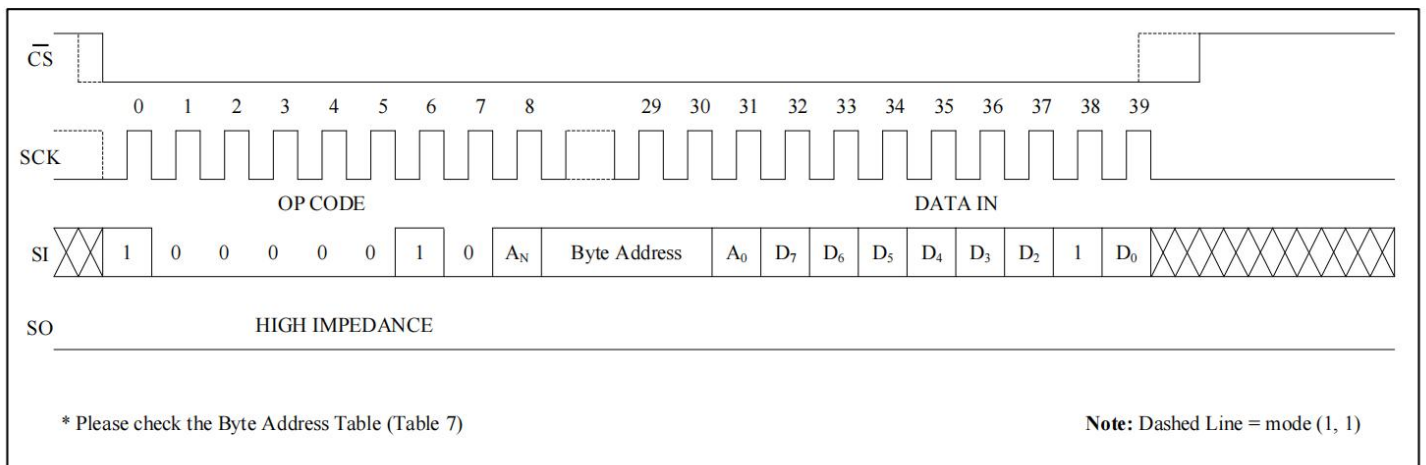


Figure 8



**Write Protection:** The Write Protect ( $\overline{WP}$ ) pin can be used to protect the Block Protect bits BP0 and BP1 against being inadvertently altered. When  $\overline{WP}$  is low and the SRWD bit is set to "1", write operations to the Status Register are inhibited.  $\overline{WP}$  going low while  $\overline{CS}$  is still low will interrupt a write to the status register. If the internal write cycle has already been initiated,  $\overline{WP}$  going low will have no effect on any write operation to the Status Register. The  $\overline{WP}$  pin function is blocked when the SRWD bit is set to "0". The  $\overline{WP}$  input timing is shown in Figure 9.

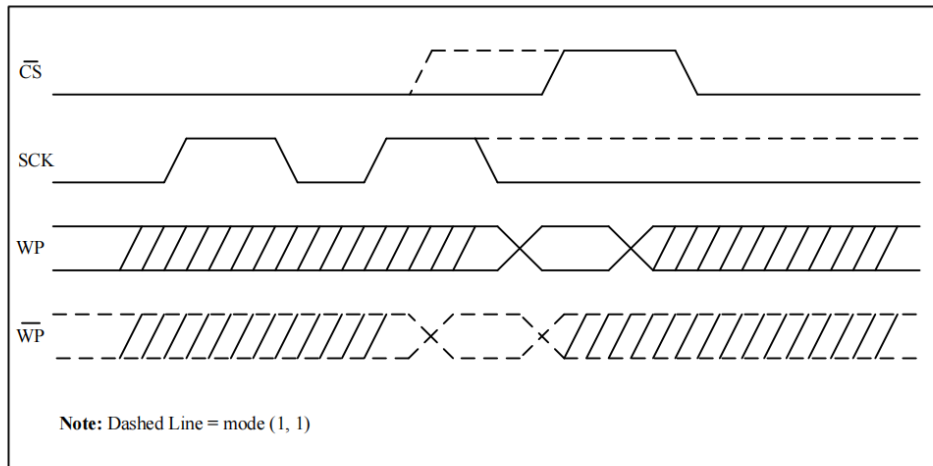


Figure 9



### 3. Read Operations

**Read from Memory Array:** To read from memory, the host sends a READ instruction followed by a 24-bit address (see Table 6 for the number of significant address bits). After receiving the last address bit, the 25M01 will respond by shifting out data on the SO pin (as shown in Figure 10). Sequentially stored data can be read out by simply continuing to run the clock. The internal address pointer is automatically incremented to the next higher address as data is shifted out. After reaching the highest memory address, the address counter “rolls over” to the lowest memory address, and the read cycle can be continued indefinitely. The read operation is terminated by taking  $\overline{CS}$  high.

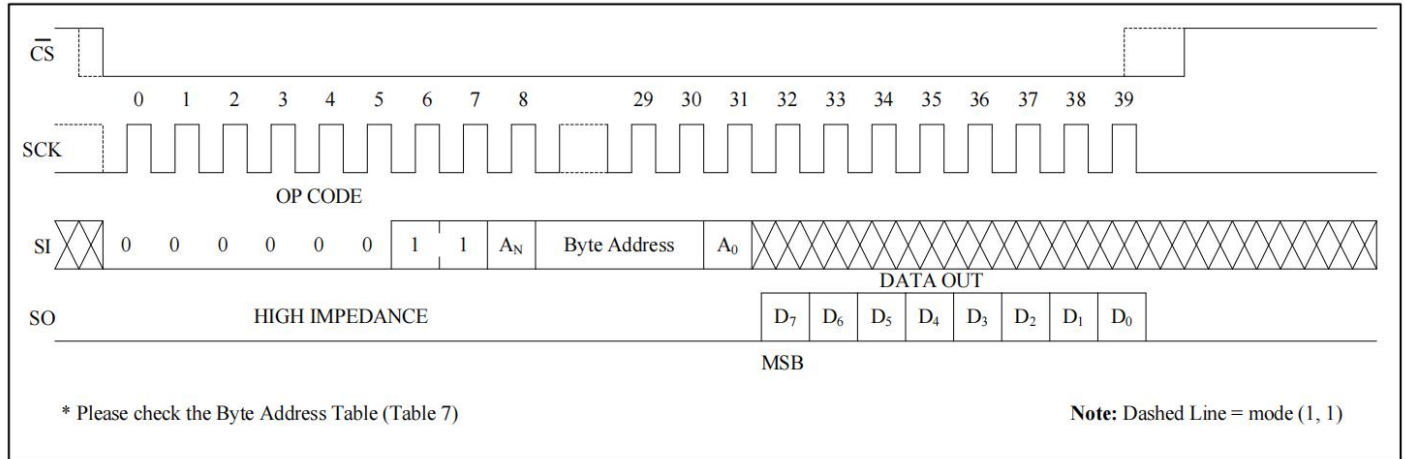


Figure 10

**Read Identification Page:** Reading the additional 256-byte Identification Page (IP) is achieved using the RDID instruction, according to timing shown in Figure 11. Address bit A10 must be 0, upper address bits are Don't Care, the lower address bits [A7:A0] address bits define the byte address inside the identification page. The byte address must not exceed the 256-byte page boundary.

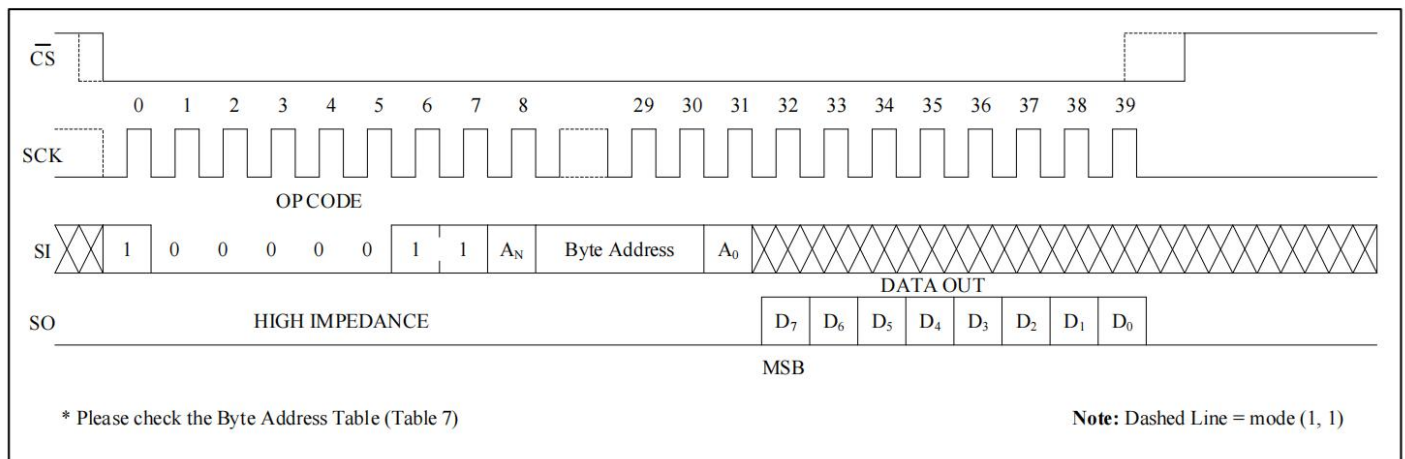


Figure 11





**Read Status Register:** To read the status register, the host simply sends a RDSR command. After receiving the last bit of the command, the 25M01 will shift out the contents of the status register on the SO pin (Figure 12). The status register may be read at any time, including during an internal write cycle.

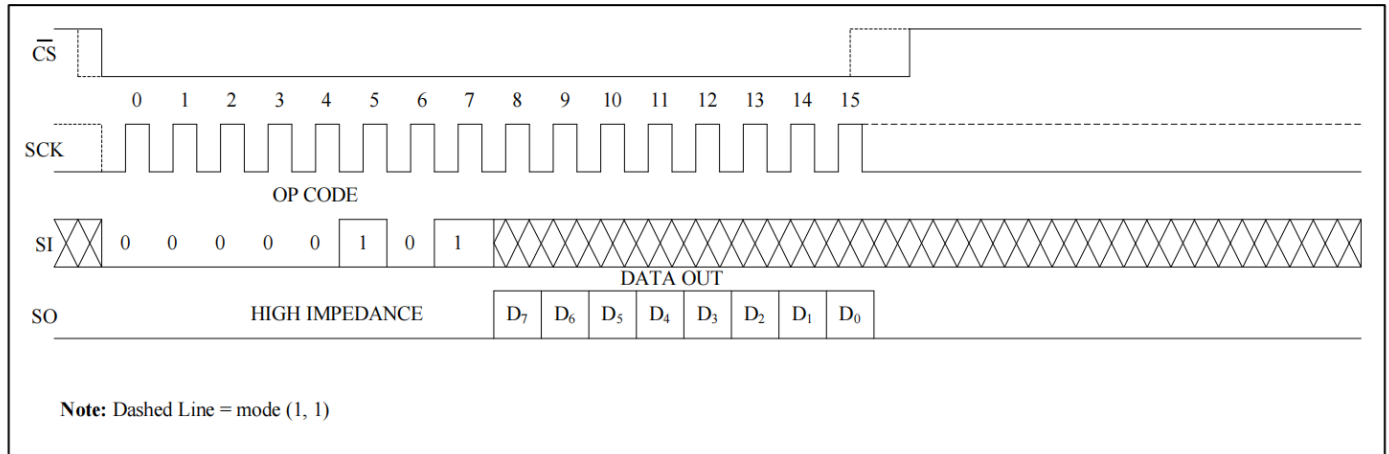


Figure 12

**Read Identification Page Lock Status:** To read Identification Page Lock status, the host simply sends a RDLS command, according to timing shown in Figure 11. The address bit A10 must be 1, all other address bits are Don't Care. The Lock bit is the bit0 of the byte read on the SO pin. It is at "1" when the lock is active and at "0" when the lock is not active. The same data byte may be read at any time, including during an internal write cycle.



#### 4. Hold Operation

The  $\overline{\text{HOLD}}$  input can be used to pause communication between host and 25M01. To pause,  $\overline{\text{HOLD}}$  must be taken low while SCK is low (Figure 13). During the hold condition the device must remain selected ( $\overline{\text{CS}}$  low). During the pause, the data output pin (SO) is tri-stated (high impedance) and SI transitions are ignored. To resume communication,  $\overline{\text{HOLD}}$  must be taken high while SCK is low.

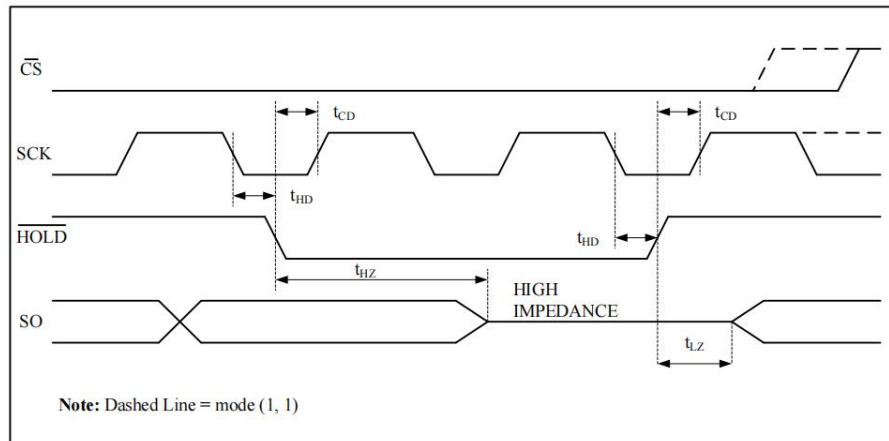


Figure 13

#### 5. Design Considerations

The 25M01 device incorporates Power-On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state. The device will power up into Standby mode after VCC exceeds the POR trigger level and will power down into Reset mode when VCC drops below the POR trigger level. This bi-directional POR behavior protects the device against 'brown-out' failure following a temporary loss of power.

The 25M01 device powers up in a write disable state and in a low power standby mode. A WREN instruction must be issued prior to any writes to the device.

After power up, the  $\overline{\text{CS}}$  pin must be brought low to enter a ready state and receive an instruction. After a successful byte/page write or status register write, the device goes into a write disable mode. The  $\overline{\text{CS}}$  input must be set high after the proper number of clock cycles to start the internal write cycle. Access to the memory array during an internal write cycle is ignored and programming is continued. Any invalid op-code will be ignored and the serial output pin (SO) will remain in the high impedance state.



## Electrical Characteristics

### Absolute Maximum Stress Ratings:

| Parameters                                         | Ratings      | Units |
|----------------------------------------------------|--------------|-------|
| Storage Temperature                                | -65 to +150  | °C    |
| Voltage on any Pin with Respect to Ground (Note 1) | -0.5 to +6.5 | V     |
| VESD (HBM)                                         | 8000         | V     |

Table 8

Comments:

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### RELIABILITY CHARACTERISTICS (Note 4):

| Symbol                        | Parameter      | Min       | Units                |
|-------------------------------|----------------|-----------|----------------------|
| N <sub>END</sub> (Notes 2, 3) | Endurance      | 1,000,000 | Program/Erase Cycles |
| TDR                           | Data Retention | 100       | Years                |

Table 9





#### D. C. OPERATING CHARACTERISTICS:

(VCC = 2.8 V to 5.5 V, unless otherwise specified)

| 25M01                        | TA = -40°C to +85°C            | VCC = +2.8V to +5.5V                                                                                         |                     |         |         |       |
|------------------------------|--------------------------------|--------------------------------------------------------------------------------------------------------------|---------------------|---------|---------|-------|
| 25M01 E1                     | TA = -40°C to +105°C           |                                                                                                              |                     |         |         |       |
| 25M01 E0                     | TA = -40°C to +125°C           |                                                                                                              |                     |         |         |       |
| Symbol                       | Parameter                      | Test Conditions                                                                                              |                     | Min     | Max     | Units |
| I <sub>CCR</sub>             | Supply Current<br>(Read Mode)  | Read, SO open                                                                                                | 2.8 V < VCC < 5.5 V | -       | 3       | mA    |
| I <sub>CCW</sub>             | Supply Current<br>(Write Mode) | Write, $\overline{CS}$ = VCC                                                                                 | 2.8 V < VCC < 5.5 V | -       | 3       | mA    |
| I <sub>SB1</sub><br>(Note 5) | Standby Current                | V <sub>IN</sub> = GND or VCC,<br>$\overline{CS}$ = VCC, $\overline{WP}$ = VCC,<br>HOLD = VCC,<br>VCC = 5.5 V |                     | -       | 5       | μA    |
| I <sub>SB2</sub><br>(Note 5) | Standby Current                | V <sub>IN</sub> = GND or VCC,<br>$\overline{CS}$ = VCC, $\overline{WP}$ = GND,<br>HOLD = GND,<br>VCC = 5.5 V |                     | -       | 5       | μA    |
| I <sub>L</sub>               | Input Leakage Current          | V <sub>IN</sub> = GND or VCC                                                                                 |                     | -       | ± 2     | μA    |
| I <sub>LO</sub>              | Output Leakage<br>Current      | $\overline{CS}$ = VCC<br>VOUT = GND or VCC                                                                   |                     | -       | ± 2     | μA    |
| V <sub>IL1</sub>             | Input Low Voltage              | VCC ≥ 2.8V                                                                                                   |                     | -0.45   | 0.3 VCC | V     |
| V <sub>IH1</sub>             | Input High Voltage             | VCC ≥ 2.8 V                                                                                                  |                     | 0.7 VCC | VCC+1   | V     |
| V <sub>OL1</sub>             | Output Low Voltage             | VCC ≥ 2.8 V, I <sub>OL</sub> = 3.0 mA                                                                        |                     | -       | 0.4     | V     |
| V <sub>OH1</sub>             | Output High Voltage            | VCC ≥ 2.8 V, I <sub>OH</sub> = -1.6 mA                                                                       |                     | 0.8 VCC | -       | V     |

Table 10



### A.C. CHARACTERISTICS:

(VCC = 2.8 V to 5.5 V, unless otherwise specified.) (Note 6)

|          |                      |                      |
|----------|----------------------|----------------------|
| 25M01    | TA = -40°C to +85°C  | VCC = +2.8V to +5.5V |
| 25M01 E1 | TA = -40°C to +105°C |                      |
| 25M01 E0 | TA = -40°C to +125°C |                      |

| Symbol                        | Parameter                   | VCC = 2.8 V – 5.5 V |     | Units |
|-------------------------------|-----------------------------|---------------------|-----|-------|
|                               |                             | Min                 | Max |       |
| f <sub>CLK</sub>              | Clock Frequency             | DC                  | 5   | MHz   |
| t <sub>SU</sub>               | Data Setup Time             | 20                  |     | ns    |
| t <sub>H</sub>                | Data Hold Time              | 20                  |     | ns    |
| t <sub>WH</sub>               | SCK High Time               | 75                  |     | ns    |
| t <sub>WL</sub>               | SCK Low Time                | 75                  |     | ns    |
| t <sub>LZ</sub>               | HOLD to Output Low Z        |                     | 50  | ns    |
| t <sub>RI</sub> (Note 7)      | Input Rise Time             |                     | 2   | μs    |
| t <sub>FI</sub> (Note 7)      | Input Fall Time             |                     | 2   | μs    |
| t <sub>HD</sub>               | HOLD Setup Time             | 0                   |     | ns    |
| t <sub>CD</sub>               | HOLD Hold Time              | 10                  |     | ns    |
| t <sub>V</sub>                | Output Valid from Clock Low |                     | 75  | ns    |
| t <sub>HO</sub>               | Output Hold Time            | 0                   |     | ns    |
| t <sub>DIS</sub>              | Output Disable Time         |                     | 50  | ns    |
| t <sub>HZ</sub>               | HOLD to Output High Z       |                     | 100 | ns    |
| t <sub>CS</sub>               | CS High Time                | 80                  |     | ns    |
| t <sub>CSS</sub>              | CS Setup Time               | 60                  |     | ns    |
| t <sub>CSH</sub>              | CS Hold Time                | 60                  |     | ns    |
| t <sub>CNS</sub>              | CS Inactive Setup Time      | 60                  |     | ns    |
| t <sub>CNH</sub>              | CS Inactive Hold Time       | 60                  |     | ns    |
| t <sub>WPS</sub>              | WP Setup Time               | 20                  |     | ns    |
| t <sub>WPH</sub>              | WP Hold Time                | 20                  |     | ns    |
| t <sub>WC</sub> (Notes 9, 10) | Write Cycle Time            |                     | 8   | ms    |

Table 11

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### POWER-UP TIMING (Notes 7, 8):

| Symbol                              | Parameter                          | Max | Units |
|-------------------------------------|------------------------------------|-----|-------|
| t <sub>PUR</sub> , t <sub>PUW</sub> | Power-up to Read / Write Operation | 0.1 | ms    |

Table 12



Note:

1. The DC input voltage on any pin should not be lower than  $-0.5\text{ V}$  or higher than  $V_{CC} + 0.5\text{ V}$ . During transitions, the voltage on any pin may undershoot to no less than  $-1.5\text{ V}$  or overshoot to no more than  $V_{CC} + 1.5\text{ V}$ , for periods of less than  $20\text{ ns}$ .
2. Page Mode,  $V_{CC} = 5\text{ V}$ ,  $25^{\circ}\text{C}$ .
3. The device uses ECC (Error Correction Code) logic with 6 ECC bits to correct one bit error in 4 data bytes. Therefore, when a single byte has to be written, 4 bytes (including the ECC bits) are re-programmed. It is recommended to write by multiple of 4 bytes located at addresses  $4N$ ,  $4(N+1)$ ,  $4(N+2)$ ,  $4(N+3)$ , in order to benefit from the maximum number of write cycles.
4. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
5. When not driven, the  $\overline{\text{WP}}$  and  $\overline{\text{HOLD}}$  inputs are pulled up to  $V_{CC}$  internally. For noisy environments, when the pin is not used, it is recommended the  $\overline{\text{WP}}$  and  $\overline{\text{HOLD}}$  input to be tied to  $V_{CC}$ , either directly or through a resistor.
6. AC Test Conditions:  
Input Pulse Voltages:  $0.3\text{ V}_{CC}$  to  $0.7\text{ V}_{CC}$   
Input rise and fall times:  $\leq 10\text{ ns}$   
Input and output reference voltages:  $0.5\text{ V}_{CC}$   
Output load: current source  $I_{OL\text{ max}}/I_{OH\text{ max}}$ ;  $C_L = 30\text{ pF}$
7. This parameter is tested initially and after a design or process change that affects the parameter.
8.  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated.
9.  $t_{WC}$  is the time from the rising edge of  $\overline{\text{CS}}$  after a valid write sequence to the end of the internal write cycle.

Bus Timing

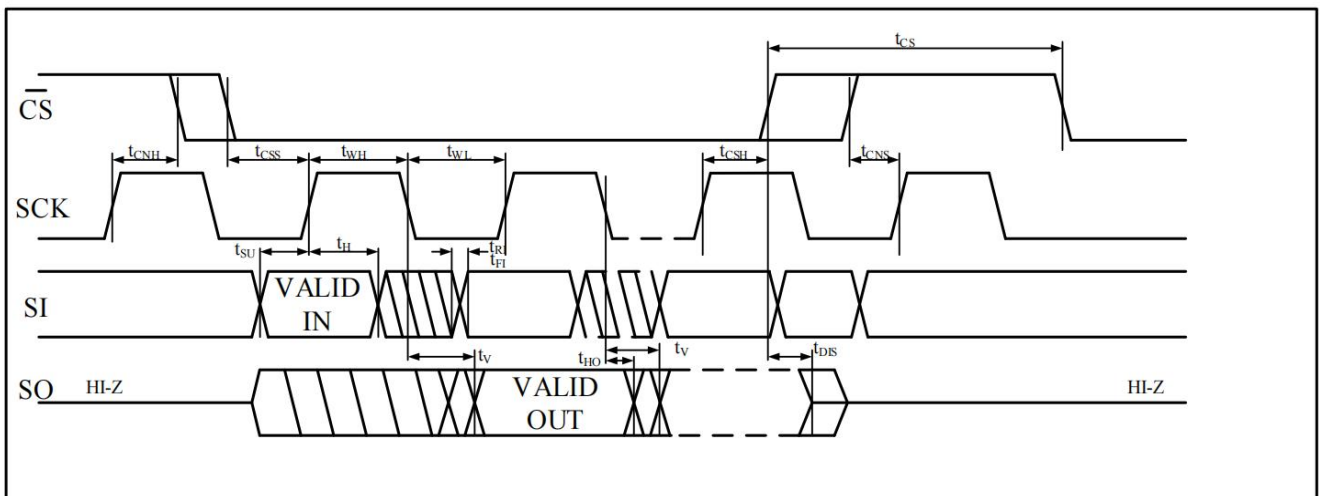


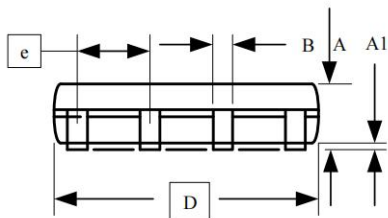
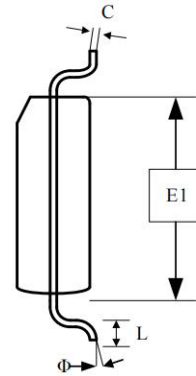
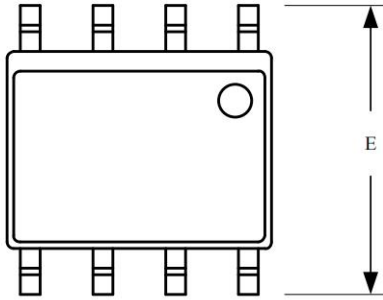
Figure 14





## Package Information

### SOP

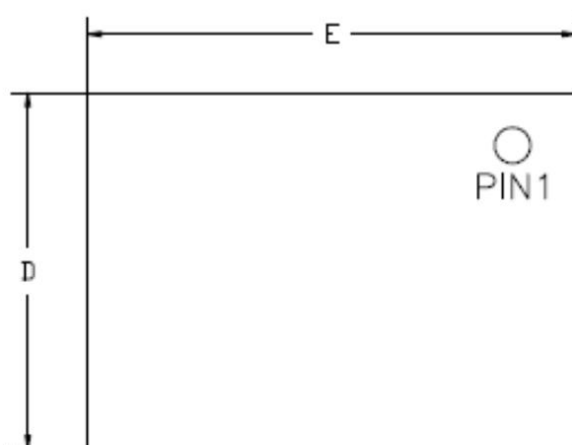


COMMON DIMENSIONS  
(Unit of Measure=mm)

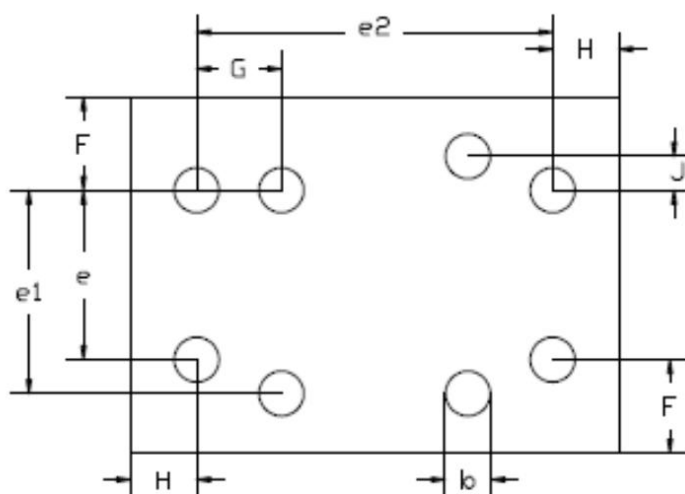
| SYMBOL | MIN     | NOM  | MAX  |
|--------|---------|------|------|
| A      | 1.35    | —    | 1.75 |
| A1     | 0.10    | —    | 0.23 |
| B      | 0.39    | —    | 0.48 |
| C      | 0.21    | —    | 0.26 |
| D      | 4.70    | 4.90 | 5.10 |
| E1     | 3.70    | 3.90 | 4.10 |
| E      | 5.80    | 6.00 | 6.20 |
| e      | 1.27BSC |      |      |
| L      | 0.50    | —    | 0.80 |
| Φ      | 0"      | —    | 8"   |



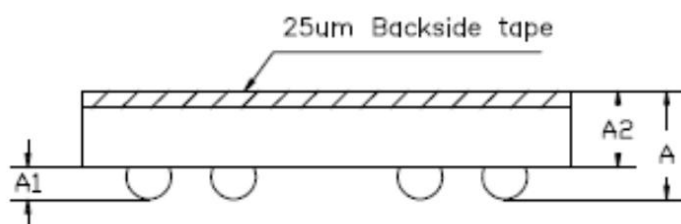
WLCSP8



TOP VIEW  
(MARK SIDE)



BOTTOM VIEW  
(BALL SIDE)



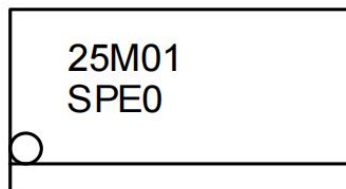
COMMON DIMENSIONS  
(UNITS OF MEASURE=MILLIMETER)

| SYMBOL | MIN       | NOM   | MAX   |
|--------|-----------|-------|-------|
| A      | 0.490     | 0.540 | 0.590 |
| A1     | 0.165     | 0.190 | 0.215 |
| A2     | 0.325     | 0.350 | 0.375 |
| D      | 2.080     | 2.100 | 2.120 |
| e1     | 1.200BSC  |       |       |
| E      | 2.860     | 2.880 | 2.900 |
| e2     | 2.100BSC  |       |       |
| b      | 0.240     | 0.270 | 0.300 |
| G      | 0.500BSC  |       |       |
| e      | 1.000BSC  |       |       |
| H      | 0.390 REF |       |       |
| F      | 0.550 REF |       |       |
| J      | 0.200 REF |       |       |



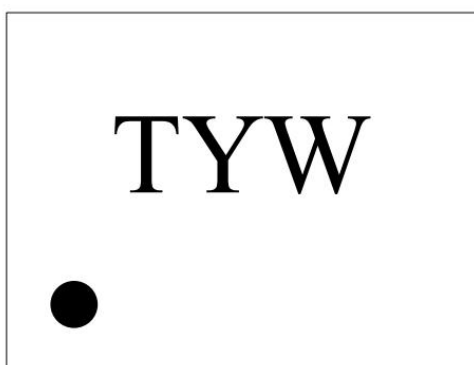
## Marking Diagram

SOP



|    |                                                                     |
|----|---------------------------------------------------------------------|
| S  | Lot ID                                                              |
| P  | P: Cu Wire Version<br>A: Au Wire Version                            |
| E0 | Blank: -40°C to +85°C<br>E1: -40°C to +105°C<br>E0: -40°C to +125°C |

WLCSP8



### PIN MARK

Y:The last digits of the year

W:week code.

|      |      |     |      |      |      |     |      |      |
|------|------|-----|------|------|------|-----|------|------|
| Y    | 1    | ... | 3    | 4    | 5    | ... | 9    | 0    |
| Year | 2021 | ... | 2023 | 2024 | 2025 | ... | 2019 | 2020 |

|      |   |     |    |    |    |     |    |    |
|------|---|-----|----|----|----|-----|----|----|
| W    | A | ... | Y  | Z  | a  | ... | y  | z  |
| Week | 1 | ... | 25 | 26 | 27 | ... | 51 | 52 |

## Ordering information

| Order Number        | Package | Package Quantity | Marking<br>On The park |
|---------------------|---------|------------------|------------------------|
| CAT25M01VI-GT3-TUDI | SOP8    | Tape,Reel,2500   | 25M01A                 |





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