MC1081S MC1081L

Ten (Four) Channel Multi-Mode Wideband Digital Capacitive Sensing Chip

1. Overview

The MC1081 series is a highly integrated, multi-channel, wide-bandwidth digital capacitance sensing chip. The chip connects directly to the measurement electrode plate and detects capacitance changes through variations in oscillation frequency. The excitation frequency is configurable within the range of 0.1 to 30 MHz. The measurement frequency output is a 16-bit digital signal, with a maximum capacitance resolution of 1 fF. The chip supports multiple operating modes, enabling measurement of single-ended capacitance, floating dual-ended capacitance, and mutual capacitance. It integrates a high-precision 16-bit digital temperature sensor for applications requiring temperature compensation or combined temperature sensing. Featuring a fully digital design, the chip configures functions and reads data via an I²C interface supporting communication rates up to 1 Mbps.

Capacitive sensing detects dielectric properties of different materials by measuring minute capacitance changes in the target substance under an applied electric field. This non-contact method offers high resolution, high speed, low power consumption, and low cost. Compared to similar domestic and international products, the MC1081 chip can simultaneously measure up to 10 single-ended capacitance channels or 5 dual-ended capacitance channels. Featuring a wide adjustable excitation frequency range and configurable amplitude, the chip offers diverse and flexible capacitance measurement modes. It operates across a broad voltage range with simple peripheral circuitry and strong adaptability. The chip is widely applicable for non-contact dielectric detection, liquid level measurement, touch control, proximity sensing, water immersion detection, dry/wet detection, moisture content analysis, and various other scenarios.

2. Features

- Supports up to 10 single-ended capacitance channels / 5 dual-ended capacitance channels
- Capacitance measurement range: 1pF to 10nF
- Measurement excitation: 100kHz to 30MHz, configurable amplitude
- Capacitance/frequency resolution: 16-bit
- Supports active shielding and adjacent mutual capacitance measurement
- Supply voltage range: 2.3V to 5.5V, with built-in LDO
- Single-channel conversion time: 0.1 ms to 23.5 ms, configurable
- Built-in 16-bit high-precision digital temperature measurement
- Typical single-channel average current: 2.5μA @ 1Hz
- Sleep current: 50nA
- Communication interface: I2C
- Operating temperature: -55°C to +125°C
- Available in QFN16/TSSOP16/DFN8 packages

3. Applications

- Liquid level measurement
- Moisture content measurement
- Water immersion sensing

- Dry/wet analysis
- Dielectric Detection
- Proximity sensing
- Button Touch
- Gesture Recognition

Product Information

Part Number	Package	Dimensions
MC1081S	QFN16	3.0*3.0*0.75mm
MC1081L	DFN8	2.0*2.0*0.55mm

Note: MC1081L is a four-channel model; other models are ten-channel.

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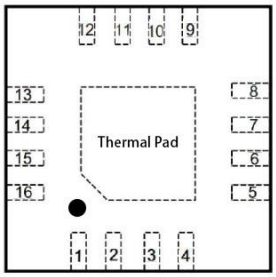
4. Package Pin Description

4.1. MC1081S Package Pinout Diagram (QFN16)



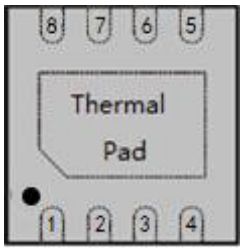
Front View

Pin Number	Pin Name	Type	Description
1	C1	A	Channel 1 Capacitive Input Terminal
2	C0	A	Channel 0 Capacitive Input Terminal
3	SHLD	O	Active Shield Output
4	SDA	I/O	I2C Data Line
5	SCL	I	I2C Clock Line
6	ADDR	I	I2C Address Line
7	VDD	P	Power Supply
8	GND	G	Ground
9	C9	A	Channel 9 Capacitive Input Terminal
10	C8	A	Channel 8 Capacitor Input Terminal
11	C7	A	Channel 7 Capacitor Input Terminal
12	C6	A	Channel 6 Capacitor Input Terminal
13	C5	A	Channel 5 Capacitor Input Terminal
14	C4	A	Channel 4 Capacitor Input Terminal
15	C3	A	Channel 3 Capacitor Input Terminal
16	C2	A	Channel 2 Capacitive Input Terminal

Note 1: I denotes input, O denotes output, P denotes power supply, G denotes ground, A denotes analog.

Note 2: Thermal Pad is left floating or grounded.

4.2. MC1081L Package Pinout Diagram (DFN8)



Front View

Pin Number	Pin Name	Type	Description
1	SDA	I/O	I2C Data Cable
2	SCL	I	I2C Clock Line
3	VDD	P	Power Supply
4	GND	G	Ground
5	C5	A	Channel 5 Capacitive Input Terminal
6	C4	A	Channel 4 Capacitor Input Terminal
7	C3	A	Channel 3 Capacitor Input Terminal
8	C2	A	Channel 2 Capacitive Input Terminal

Note 1: I denotes input, O denotes output, P denotes power supply, G denotes ground, A denotes analog signal.

Note 2: Thermal pad left floating or grounded.

5. Electrical Specifications

5.1. Absolute Maximum Ratings

		Minimum	Maximum	Unit
VDD	Supply Voltage Range	-0.3	6.0	V
Vi	Pin voltage	-0.3	VDD	V
T_J	Junction Temperature	-55	125	℃
T_{stg}	Storage Temperature	-55	125	℃

Note: The above are limit parameters. This specification does not apply to the functional operation of the device in environments exceeding these limits. Prolonged exposure to these extreme conditions may affect device reliability.

5.2. ESD Rating

		Value	Unit
V_{ESD} Electrostatic Discharge	Human-body model (HBM)	±8000	V
	Charged-Device Model (CDM)	±750	V

5.3. Electrical Characteristics

Unless otherwise specified, data in the table is measured at T=25°C and VDD=5V.

Parameters		Test Conditions	Minimum	Typical Value	Maximum	Unit
Power Consumption						
V_{DD}	Supply Voltage	T = -40°C to +125°C	2.3		5.5	V
$I_{DDCMEAS}$	Capacitance measurement current[1][5]	Single-ended mode, amplitude V_{DD} -0.8V	0.63[2]		3.35[3]	mA
		Bias mode, amplitude 2.4V	0.93[2]		2.75[3]	mA
I_{DDSLP}	Sleep Current	I2C Bus Idle		50		nA
I_{DDAVG}	Average Current	I_D =4μA, T_{CV} =1ms, 1Hz	0.63			μA
Capacitive sensing						
C_{SENSOR}	Capacitance Range		0.001		10	nF
C_{IN}	Pin Parasitic Capacitance			5		pF
Cref	Internal Reference Capacitance			20		pF
N_{BITS}	Data Bits			16		Bit
T_{CV}	Single-channel conversion time		0.1		23.5	ms
f_{SENSOR}	Oscillation frequency range		0.1		30	MHz
I_{DRIVE}	Oscillation Drive Current		0.004		2.0	mA
Temperature sensing						
T_{RANGE}	Temperature Measurement Range		-55		125	°C
T_{LSB}	Temperature Resolution			0.0038		°C
T_{ERROR}	Temperature measurement accuracy	T = -20°C to 100°C	-2		2	°C
T_{BITS}	Temperature Data Bits			16		Bit
T_{TCV}	Conversion time		1.7		4.7	ms
$I_{DDTMEAS}$	Temperature Measurement Current[4][5]			0.64		mA
System Clock						
f_{SYS}	System clock frequency	T = 25°C		19.2		MHz
TC_{SYSCLK}	System clock temperature coefficient	T = -40°C to 125°C		25	100	ppm/°C
Active Shielding						
IDDSHIELD	Active Shielding Operating Current[6]	High Drive Mode		2.45		mA
		Low Drive Mode		0.83		
fSHIELD	Signal Frequency Range	f_{SENSOR}Range for This Function	100		500	kHz
CLOAD	Load capacitance	High Drive Mode, f=500KHz			60	pF
		Low Drive Mode, f=500KHz			30	
RLOAD	Load Resistance	High drive mode,	10			kΩ

		f=500kHz				
		Low Drive Mode, f=500KHz	500			

Note 1: Capacitance measurement current represents the total current drawn by the chip during capacitance conversion. This value excludes currents for temperature measurement, active shielding, and I²C communication.

Note 2: Drive current 4μA, internal LDO configured in low-power mode.

Note 3: Drive current 2000μA, internal LDO configured in low-power mode.

Note 4: Temperature measurement current represents the total current consumed by the chip during temperature conversion. This value excludes currents for capacitance measurement, active masking, and I2C communication.

Note 5: If temperature and capacitance conversion are initiated simultaneously, the total operating current is less than the direct sum of the two values.

Note 6: When active shielding is enabled, the total operating current is the sum of the capacitance measurement current and the active shielding operating current.

5.4. I2C Interface Timing

Table 5.4 I2C Bus Timing Characteristics [1]

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Frequency	f_{SCL}	0	400	0	1000	KHz
SCL Low Level Duration	t_{LOW}	1300	—	620	—	ns
SCL High Level Duration	t_{HIGH}	600	—	220	—	ns
Duration of SCL high level after SDA is pulled low during start(restart)	$t_{HD;STA}$	400	—	260	—	ns
Time interval from SCL pull-low to SDA data change	$t_{HD;DAT}$	0	0.9	0	—	μs
Time interval from SDA data stabilization to SCL pull-high	$t_{SU;DAT}$	100	—	150	—	ns
High-level hold time of SCL before SDA is pulled low during restart	$t_{SU;STA}$	400	—	260	—	ns
Time interval from SCL pull-high to SDA pull-high during stop	$t_{SU;STO}$	400	—	260	—	ns
Interval between start and stop	t_{BUF}	1300	—	500	—	ns
SCL/SDA rising edge time	t_{RC}	20+ 0.1Cb[(2)]	1000	20+ 0.1Cb[(2)]	120	ns
SCL/SDA falling edge time required	t_{FC}	20+ 0.1Cb[(2)]	300	20+ 0.1Cb[(2)]	120	ns

Note 1: All values are referenced to VIHmin and VILmax.

Note 2: Cb = Total capacitance of the I²C bus.

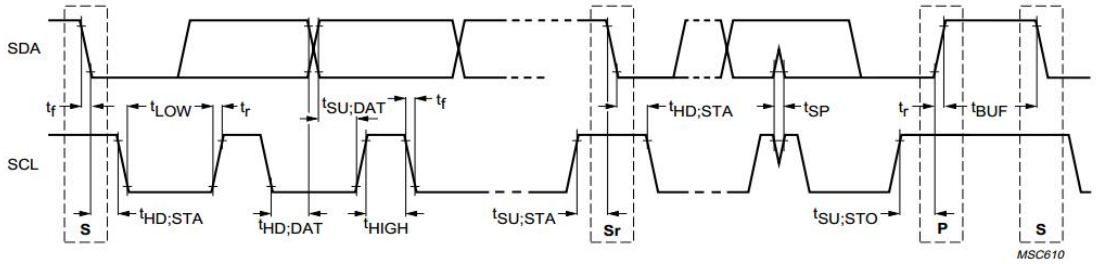


Figure 5.4 I2C Timing Parameters

6. Operating Mode Description

6.1. Working Principle

Differences in the dielectric constant characteristics of the measured substance cause variations in capacitance values. When the measured capacitance changes, the oscillation frequency of the MC1081 excitation circuit also changes accordingly. Based on this principle, the chip calculates capacitance values by measuring frequency counts, thereby obtaining physically meaningful information such as liquid level, proximity, moisture content, and touch detection.

Through different register configurations, the MC1081 chip can measure multi-channel single-ended capacitance to ground, dual-ended floating capacitance, and mutual capacitance. The chip integrates specialized capacitance measurement circuits, including a capacitance excitation circuit, frequency counting circuit, and digital signal processing, along with fully integrated designs such as LDO power management and temperature sensing circuits, eliminating the need for excessive peripheral components.

6.2. System Block Diagram

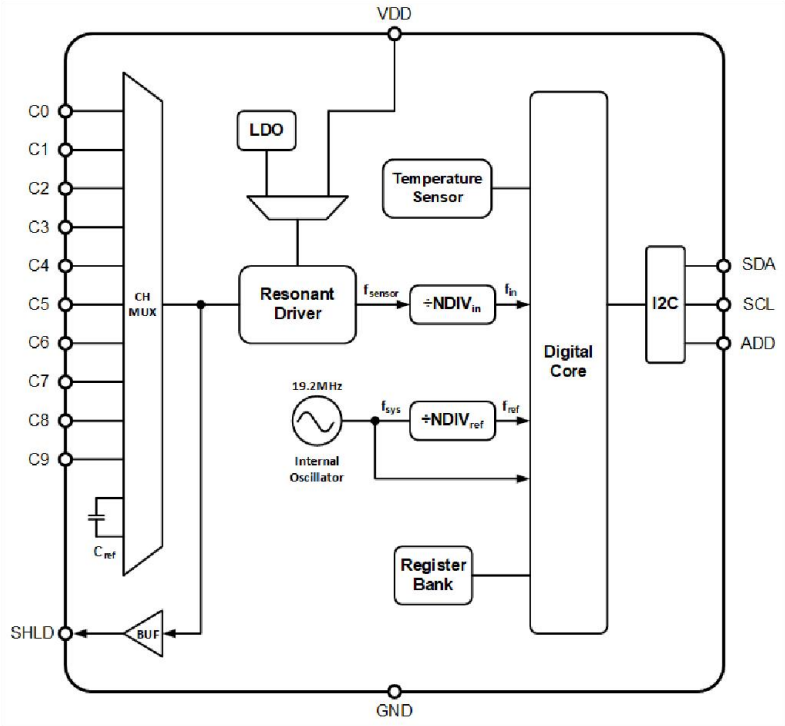


Figure 6.2 MC1081 System Block Diagram

The figure above shows the MC1081 system block diagram, including functional modules such as the resonant driver, channel multiplexer, frequency divider, internal oscillator, digital core, register bank, temperature sensor, I²C interface, LDO, and power management. The MC1081's driver circuit and external capacitor C_{sensor}form a capacitive sensor. This generates varying oscillation signals f_{sensor},which are frequency-divided and fed to the digital logic circuit to measure and digitize the input signal frequency f_{in}. The digital logic uses a reference frequency $f_{ref}$to measure the sensor signal frequency f_{in}. This reference frequency $f_{ref}$is derived from the chip's internal high-precision 19.2MHz clock through a divider. Channels $C_{0\sim9}$can connect to multiple single-point or dual-end capacitive electrodes as required by the application. Active shielding via SHLD is available when needed. The I2C interface is used for chip mode configuration and sensor data readout.

6.3. Functional Description

6.3.1. Clock System

In the MC1081 system block diagram, f_{sys}, f_{ref}, $f_{(sensor)}$,and $f_{in}$are four critical clock signals. f_{sensor}represents the oscillation frequency of the capacitance measurement circuit. After division by FIN_DIV, it yields the measured clock signal f_{in}. $f_{sys}$is the internal system clock of the chip, operating at 19.2 MHz. After being divided by FREF_DIV, it yields the reference clock f_{ref}. To ensure accurate measurement results,

$f_{ref}$and f_{in}must satisfy the following conditions:

$$f_{in} < \frac{f_{ref}}{4}$$

The following table defines the clock configuration-related registers.

Table 6.3.1 Clock Configuration Register Definitions

Clock	Register	Address	Bit	Description
f_{in}	DIV_CFG	0x1F	FINDIV[2:0]	000: Division ratio NDIVin=1 001: NDIVin division ratio = 2 010: NDIVin division ratio = 4 011: NDIVin division ratio = 8 100: NDIV$_{in}$ frequency division ratio = 16 101: NDIVin frequency division ratio = 32 110: Frequency division ratio NDIVin=64 111: Frequency division ratio NDIVin=64
f_{ref}	DIV_CFG	0x1F	FREFDIV[1:0]	00: NDIVref division ratio = 1 01: NDIVref division ratio = 2 10: NDIVref division ratio = 4 11: Division ratio NDIVref=8

The relationship between clock signals $f_{sensor}$and f_{in}, as well as $f_{sys}$and $f_{(ref),}$is expressed as follows:

$$f_{in} = \frac{f_{sensor}}{NDIV_{in}} \quad (1)$$

$$f_{ref} = \frac{f_{sys}}{NDIV_{ref}} \quad (2)$$

Note that f_{in}must be greater than 100 kHz.

6.3.2. Capacitance Measurement

The MC1081 supports multi-channel, multi-mode capacitance measurement. By configuring the C_CMD register, the capacitance measurement mode can be selected: single-ended measurement mode and dual-ended measurement mode. Single-ended measurement mode is suitable for capacitance measurement with one terminal grounded. Dual-ended measurement mode is suitable for capacitance measurement with both terminals floating.

Table 6.3.2 Single-Ended/Balanced Measurement Mode Selection

Register	Address	Bit	Description
C_CMD	0x1D	OSC_SEL	0: Single-ended measurement mode 1: Dual-ended measurement mode

6.3.3. Capacitance Measurement Mode

6.3.3.1. Single-ended to ground capacitance

Measure single-ended capacitance to ground by connecting the capacitance or electrode to any measurement channel on the chip, as shown in the figure below. Configure OSC_SEL=0 and select the measurement channel by configuring OSC1_CHS_M and OSC1_CHS_L. The capacitance values for channels 0 to 9 (10 channels total) can be measured. Refer to Section 6.3.3.5 for the pin-to-channel correspondence.

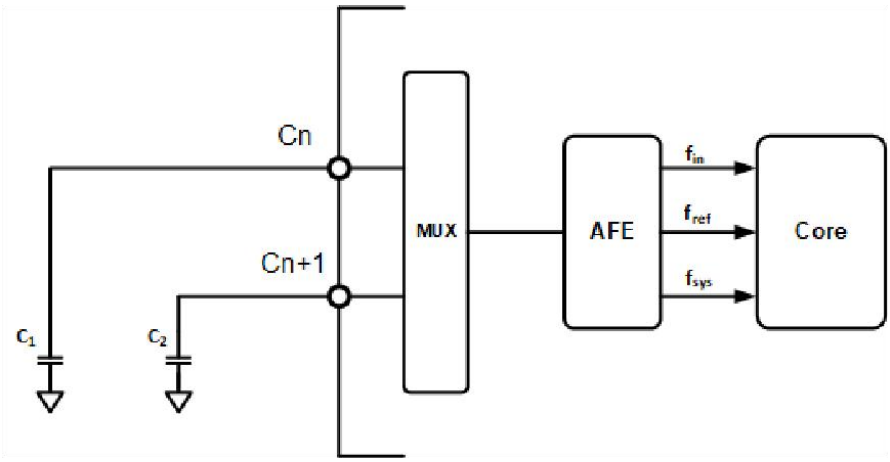


Figure 6.3.3.1 Single-Ended Capacitance Measurement

6.3.3.2. Bidirectional Floating Capacitance

To measure dual-ended floating capacitance, select the dual-ended measurement mode. This method is insensitive to ground noise and offers fast measurement speed, making it suitable for scenarios requiring rapid measurement and high ground plane interference. The connection configuration is shown below. Configure OSC_SEL=1 for measurement and select the measurement channel via OSC2_CHS. There are five measurement channels in total. Each pair of dual-ended floating capacitors occupies two single-ended channels. Refer to Section 6.3.3.7 for pin-channel correspondence.

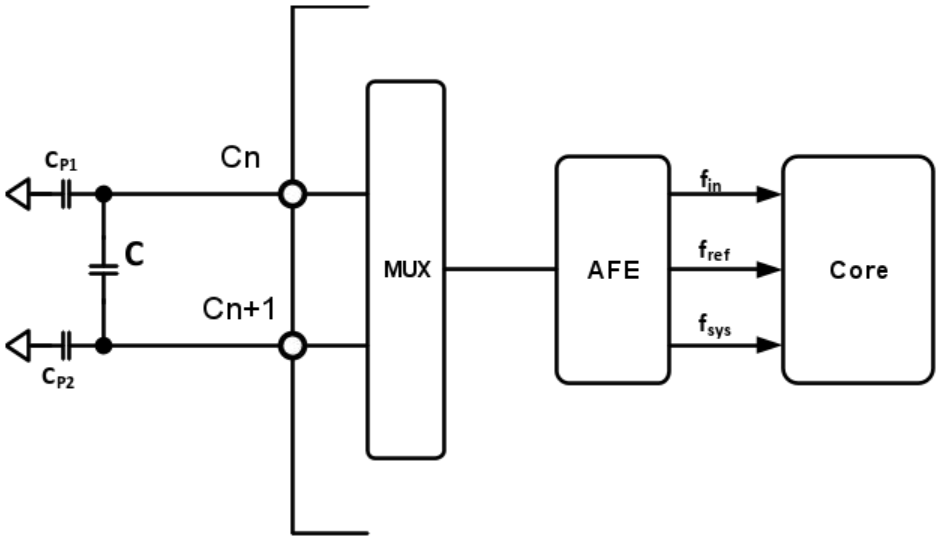


Figure 6.3.3.2 Measuring Floating Capacitance

6.3.3.3. Mutual Capacitance

Mutual capacitance eliminates channel-to-ground parasitic capacitance. Mutual capacitance measurement is performed in single-ended mode, where internal control logic and calculations yield a frequency count value reflecting mutual capacitance C_M. The mutual capacitance connection is shown below, where channel subscript n takes values 0, 2, 4, 6, and 8. In the diagram, $C_{P1}$and C(P2)$_{represent\ mutual\ capacitance,\ while\ C(P3)}$and C(P4) represent parasitic capacitance. $_{P2}$represent parasitic capacitance. Configuration OSC_SEL=0 is required for measurement, with measurement channels selected via OSC1_CHS_M, OSC1_CHS_L, and OSC1_MCHS. Five measurement channels are available, with each mutual capacitance pair occupying two single-ended channels. Refer to Section 6.3.3.5 for pin-to-channel mapping.

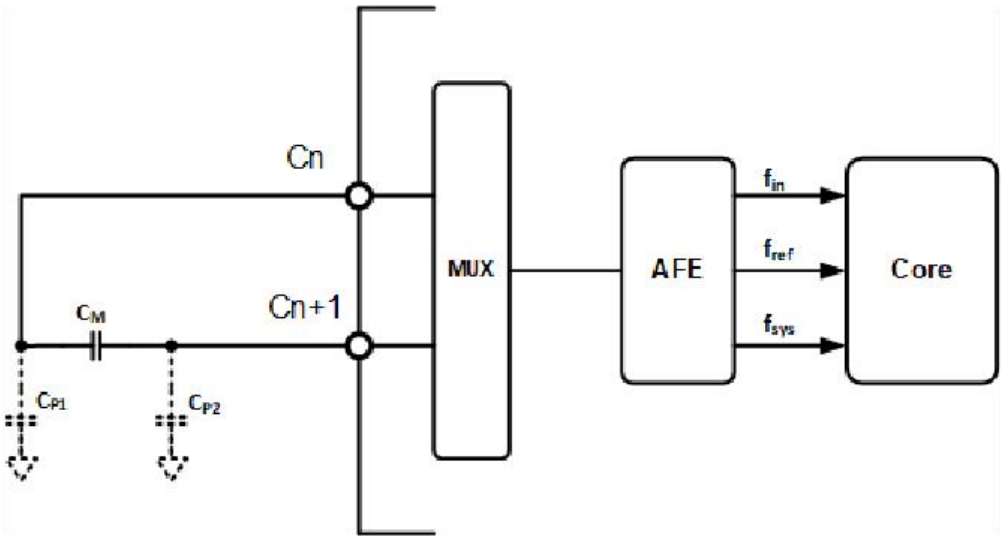


Figure 6.3.3.3-1 Measuring Mutual Capacitance

The mutual capacitance measurement process consists of three steps: Step 1: Measure capacitance value C1 Step 2: Measure capacitance value C2 Step 3: Measure capacitance value C3 The mutual capacitance $C_M = (C1+C2-C3)/2$ is then calculated. Note that this method subtracts the port parasitic capacitances $C_{(P1)}$ and C_{P2}.

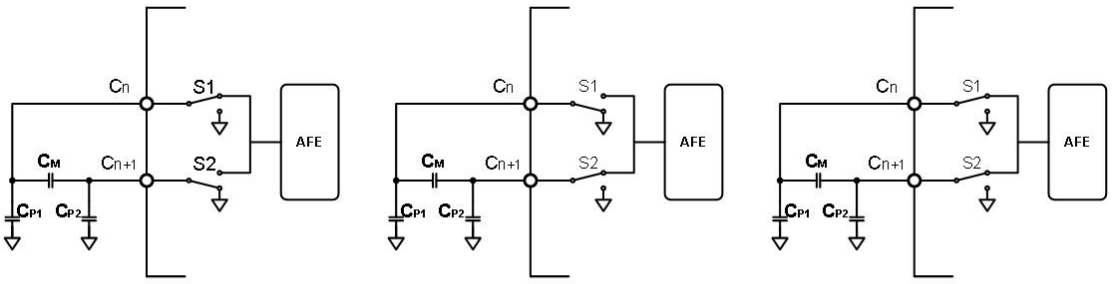


Figure 6.3.3.3-2 Steps for Mutual Capacitance Measurement

6.3.3.4. Capacitance Measurement Procedure

After determining the capacitance type under test and configuring OSC_SEL, proceed as follows. Section 6.3 provides detailed instructions.

i. Channel Selection and Pin Configuration

ii. Drive Strength and Amplitude Configuration

iii. Measurement and Configuration Conversion Duration

iv. Data Reading

v. Capacitance calculation

6.3.3.5.

In single-ended mode (OSC_SEL=0), the MC1081 provides 11 measurement channels: 10 external channels (corresponding to channels 0–9) and 1 internal reference channel (corresponding to channel 10). Table 6.3.3.5-1 details the configuration registers for single-ended mode.

Table 6.3.3.5-1 Single-Ended Mode Channel Selection Register

Channel and Corresponding Pin	Register	Address	Bit	Description
Channel 10: Internal Reference Capacitor Cref	OSC1_CHS_MSB	0x20	CH_REF	0: Indicates internal reference channel is not measured 1: Measure internal reference channel
Channel 9: C9			CH9	0: Indicates not measuring

				channel 9 1: Indicates measurement of channel 9
Channel 8: C8			CH8	0: Indicates non-measurement channel 8 1: Indicates measurement channel 8
Channel 7: C7	OSC1_CHS_LSB	0x21	CH7	0: Indicates channel 7 is not measured 1: Indicates measurement of Channel 7
Channel 6: C6			CH6	0: Indicates non-measurement channel 6 1: Indicates measurement channel 6
Channel 5: C5			CH5	0: Indicates non-measurement channel 5 1: Indicates measurement channel 5
Channel 4: C4			CH4	0: Indicates non-measurement channel 4 1: Indicates measurement channel 4
Channel 3: C3			CH3	0: Indicates non-measurement channel 3 1: Indicates measurement channel 3
Channel 2: C2			CH2	0: Indicates non-measurement of channel 2 1: Indicates measurement channel 2
Channel 1: C1			CH1	0: Indicates non-measurement of channel 1 1: Indicates measurement channel 1
Channel 0: C0			CH0	0: Indicates non-measurement channel 0 1: Indicates measurement channel 0

The MC1081 also supports mutual capacitance measurements between channels. Table 6.3.3.5-2 details the grouping and configuration register specifications for mutual capacitance measurement channels.

Table 6.3.3.5-2 Mutual Capacitance Channel Selection Register

Channel and Corresponding Pin	Register	Address	Bit	Description
Channel 4: C8 and C9	OSC1_MCHS	0x22	MCH4	0: Indicates mutual capacitance between channels 8-9 is not measured 1: Indicates mutual capacitance measurement between channels 8-9
Channel 3: C6 and C7			MCH3	0: Indicates mutual capacitance between channels 6-7 is not measured 1: Indicates mutual capacitance between measurement channels 6-7
Channel 2: C4 and C5			MCH2	0: Indicates mutual capacitance between channels 4-5 is not measured 1: Indicates measurement of mutual capacitance between channels 4-5
Channel 1: C2 and C3			MCH1	0: Indicates mutual capacitance between channels 2-3 is not measured 1: Indicates mutual capacitance between channels 2-3
Channel 0: C0 and C1			MCH0	0: Indicates mutual capacitance between channels 0-1 is not measured 1: Indicates measurement of mutual capacitance between channels 0-1

When configuring mutual capacitance channels, both the corresponding CHx bit and MCHx bit must be set to 1. For example, to select mutual capacitance channel 1 for measurement, simultaneously set CH2=1, CH3=1, and MCH1=1. The chip will automatically perform the measurement and provide the corresponding mutual capacitance $C_M$data.

In single-ended mode, when a channel is inactive, its pin connection can be configured via registers with three modes: high impedance, grounded, and active shield. Specific configurations are shown in the table below.

Table 6.3.3.5-3 Pin Configuration Register

Register	Address	Bit	Description
SHLD_CFG	0x26	CS[1:0]	00: Indicates the capacitance measurement port is in

			a high-impedance state during non-measurement periods. 01: Indicates the capacitance measurement port is grounded during non-measurement periods. 1x: Indicates the capacitance measurement port outputs an active shield signal during non-measurement periods. This is only active when OSC_SEL=0 and SHLD_EN=1.

6.3.3.6. Single-Ended Mode Drive Strength and Amplitude Configuration

In single-ended mode, the drive strength has 9 configurations. The specific configurations and corresponding drive currents are shown in the table below.

Table 6.3.3.6-1 Single-Ended Mode Drive Strength Configuration Register

Register	Address	Bit	Description
OSC1_CFG	0x23	OSC1_I[3:0]	0000: Drive current is 4uA 0001: Drive current is 8μA 0010: Drive current is 16μA 0011: Drive current is 42μA 0100: Drive current is 100 μA 0101: Drive current is 250 μA 0110: Drive current is 500 μA 0111: Drive current is 1000μA 1xxx: Drive current is 2000μA

In single-ended mode, the oscillation amplitude has 8 configurations: When higher power supply noise suppression is required, it is recommended to select the 0.2V-1.2V amplitude configuration. At this time, the drive circuit is powered by the internal LDO. When large swing excitation drive is needed, the configuration amplitude is related to the V_{DD}voltage, as shown in the last four configurations in the table below. At this time, the internal LDO is disabled, and the drive circuit is powered by VDD.

Table 6.3.3.6-5 Single-Ended Mode Oscillation Amplitude Configuration Register

Register	Address	Bit	Description
OSC1_CFG	0x23	OSC1_LDO	Internal LDO Power Mode Configuration 0: Low-power mode, suitable for fsensor < 1MHz 1: High-power mode, suitable for fsensor > 1MHz The above configuration is only valid when using the internal LDO power supply
		OSC1_V[2:0]	000: 0.2V amplitude (internal LDO power supply)

			001: 0.4V amplitude (internal LDO power supply) 010: Amplitude 0.8V (Internal LDO power supply) 011: Amplitude 1.2V (Internal LDO power supply) 100: Amplitude V_{DD}-2.2V (VDD power supply) 101: Amplitude of V_{DD}-1.6V (VDD supply) 110: Amplitude of V_{DD}-1.2V (VDD supply) 111: Amplitude of V_{DD}-0.8V (VDD supply)

6.3.3.7. Bias Mode Channel Selection and Port Configuration

In dual-ended mode (when OSC_SEL=1), adjacent capacitance measurement pins on the MC1081 form a dual-ended channel. This includes 5 external channels (corresponding to channels 0–4) and 1 internal reference channel (corresponding to channel 5). The configuration registers are shown in the table below.

Table 6.3.3.7-1 Bidirectional Mode Channel Selection Register

Channel and Corresponding Pins	Register	Address	Bit	Description
Channel 5: Internal Reference Capacitance CREF	OSC2_DCHS	0x24	DCH_REF	0: Indicates internal reference channel is not measured 1: Indicates measurement of internal reference channel
Channel 4: C8 and C9			DCH4	0: Indicates no measurement of dual-ended channel 4 1: Indicates measurement of dual-ended channel 4
Channel 3: C6 and C7			DCH3	0: Indicates no measurement for dual-ended channel 3 1: Indicates measurement of dual-ended channel 3
Channel 2: C4 and C5			DCH2	0: Indicates no measurement for dual-ended channel 2 1: Indicates measurement of dual-ended channel 2
Channel 1: C2 and C3			DCH1	0: Indicates no measurement for dual-ended channel 1 1: Indicates measurement of dual-ended channel 1

Channel 0: C0 and C1			DCH0	0: Indicates no measurement for dual-ended channel 0 1: Indicates measurement of differential channel 0

In differential mode, when a channel is inactive, its pin connection can be configured via the register with two modes: high impedance and grounded. Active shielding is not supported. Specific configurations are shown in the table below.

Table 6.3.3.7-2 Pin Configuration Register

Register	Address	Bit	Description
SHLD_CFG	0x26	CS[1:0]	00: Indicates non-measuring channel is in high-impedance state 01: Indicates non-measuring channel internally grounded 1x: Invalid (OSC_SEL=1)

6.3.3.8. Bias Strength and Amplitude Configuration for Bipolar Mode

In dual-ended mode, the drive strength has 9 configurations. The specific configurations and corresponding drive currents are shown in the table below.

Table 6.3.3.8-1 Bidirectional Mode Drive Strength Configuration Register

Register	Address	Bit	Description
OSC2_CFG	0x25	OSC2_I[3:0]	0000: Drive current is 4μA 0001: Drive current is 8μA 0010: Drive current is 16μA 0011: Drive current is 42μA 0100: Drive current is 100 μA 0101: Drive current is 250 μA 0110: Drive current is 500 μA 0111: Drive current is 1000μA 1xxx: Drive current is 2000μA

In dual-ended mode, the differential oscillation amplitude has six configurations, all of which activate the internal LDO. The specific configurations are shown in the table below.

Table 6.3.3.8-2 Dual-Mode Oscillation Amplitude Configuration Register

Register	Address	Bit	Description
OSC2_CFG	0x25	OSC2_LDO	Internal LDO Power Mode Configuration 0: Low-power mode, suitable for fsensor < 1MHz 1: High-power mode, suitable for fsensor >

			1MHz
		OSC2_V[2:0]	Dual-Ended Mode Oscillation Amplitude Configuration 000: Amplitude set to 0.4V 001: Amplitude 0.8V 010: Amplitude 1.2V 011: Amplitude is 1.6V 100: Amplitude is 2.0V 101: Amplitude of 2.4V 110: Amplitude of 2.4V 111: Amplitude of 2.4V

6.3.4. Measurement and Conversion Time

The MC1081 supports multi-channel measurement. During a single measurement session, all selected channels are measured sequentially. Measurement modes include: single measurement and cyclic measurement. The repeat interval for cyclic measurement is configurable: continuous without interval, 100ms, 1s, and 10s. In periodic measurement mode, if parameters are modified during measurement, changes will not take effect immediately. A stop measurement command must be sent first, followed by restarting the periodic measurement for the new parameters to apply.

To enhance measurement accuracy, the device supports averaging multiple measurement data sets, with selectable averaging factors of 1, 4, 8, or 32. When in sleep mode (SLEEP_EN=1), the chip enters sleep after executing each I2C command or completing a measurement to reduce power consumption. Specific configuration details are shown in the table below.

Table 6.3.4-1 Capacitance Measurement Control Register

Register	Address	Bit	Bit Definition	Description
C_CMD	0x1D	7	OSC_SEL	Oscillation Mode Selection 0: Select single-ended mode; 1: Select differential mode
		6	SLEEP_EN	Chip Sleep Mode Switch 0: Sleep mode disabled; 1: Sleep mode enabled
		5:4	CAVG[1:0]	Frequency Count Value Dx Average Count 00: 1 time 01: 4 times 10: 8 times 11: 32 times
		3:2	CR[1:0]	Cycle Conversion Interval

				Configuration 00: Measure once every 10 seconds 01: Measure once every 1 second 10: Measure every 0.1 seconds 11: Continuous uninterrupted measurement, no interval
		1:0	OS, SD	Capacitance conversion start bit 00: Periodic conversion 10: Period conversion 01: Stop conversion 11: Single conversion

The conversion duration for each channel of the MC1081 is determined by the CNT_CFG register. The value of bit FINCNT is N, indicating the total duration measured over N cycles of the f_{in}signal. To increase the total measurement duration, either increase the FINCNT value or the FINDIV division factor. Bit SETTLING indicates the channel's initial settling time, during which the signal is excluded from frequency counting. Specific configuration details are shown in the table below.

Table 6.3.4-2 Measurement Period Count and Settling Time Configuration Register

Register	Address	Bit	Bit Definition	Description
CNT_CFG	0x1E	7:0	FINCNT[7:0]	Set the number of measurement cycles N for f_{in} 0x00: Measure the duration of 1 fin cycle 0x01~0xFF: Measure the duration of N fin cycles, N=1~255
DIV_CFG	0x1F	7	SETTLING	Set the number of f_{in}cycles for settling 0: Represents the settling time of 1 f_{in}cycle 1: Represents the settling time over 4 f_{in}cycles

The following diagram illustrates the workflow for a single measurement, using Channel 0, Channel 1, and Channel 4 in single-ended mode as an example.

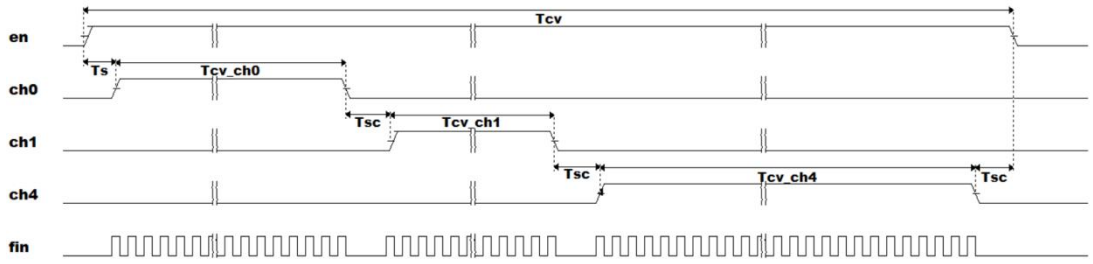


Figure 6.3.4-1 Measurement Workflow for

In the figure above, the en signal enables the capacitive sensor. When measurement begins, the en signal is pulled high; when measurement completes, the en signal is pulled low, with a total conversion time of T_{cv}. After en is pulled high, the oscillation circuit stabilizes, taking a time of T_s(=50us). Subsequently, channel 0 is selected, with a conversion time of T_{cv_ch0}. After Channel 0 completes, the system switches to Channel 1. The channel switching time is T_{sc}(=5μs). After Channel 1 is selected, its conversion time is T_{cv_ch1}. Following Channel 1's completion, the system switches to Channel 4, with switching time $T_{sc}$and conversion time T_{cv_ch4}. After Channel 4 completes, another T_{sc}elapses to finish the entire measurement process. Adding one channel x increases the total conversion time by (T_{cv_chx}+ T_{sc}). The expression for the total conversion time $T_{cv}$is:

$$T_{cv} = T_s + \left(T_{cv\_ch1} + T_{sc}\right) + \left(T_{cv\_ch2} + T_{sc}\right) + \left(T_{cv\_ch4} + T_{sc}\right) \quad (3)$$

$$T_{cv\_chx} = \frac{FIN\_CNT * C\_AVG * N_s}{f_{inx}} = \frac{(FREF\_DIV * D_x) * \left(C\_AVG + \frac{N_s}{FIN\_CNT}\right)}{f_{xin}} \quad (4)$$

In Equation (4):

- FIN_CNT represents the number of measurement cycles for f_{in}, as detailed in Table 6.3.4-2 Measurement Cycle Count and Settling Time Configuration Register;
- C_AVG is the number of internal sampling averages, as detailed in Table 6.3.4-1 Capacitance Measurement Control Register;
- $N_{(s)}$ isthe number of settling cycles for f_{in}, which can be set to 1 or 4 based on the SETTLING configuration;
- FREF_DIV is the system clock division factor. Refer to Table 6.3.1 Clock Configuration Register for details;
- Dx is the frequency count value read from the data register for each channel (x denotes the selected channel). Refer to Table 6.3.7 Data Register for details;
- $f_{inx}$is the oscillation frequency of channel x after division by FIN_DIN;

- $f_{sys}$is the internal system clock frequency of the chip, set at 19.2 MHz.

The mutual capacitance measurement timing for the MC1081 is divided into three steps. Taking the mutual capacitance between channels 2 and 3 as an example, the process is illustrated in the figure below:

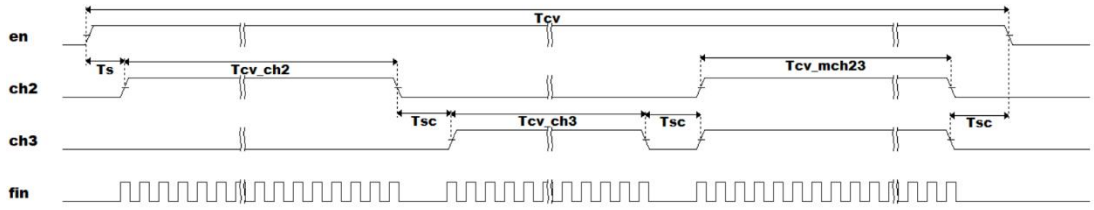


Figure 6.3.4-2 Mutual Capacitance Measurement Workflow

Step 1: Measure channel 2 with conversion time T_{cv_ch2} ; Step 2: Measure channel 3 with conversion time T_{cv_ch3} ; Step 3: Simultaneously measure channels 2 and 3 with conversion time T_{cv_mch23}. T_s represents the oscillation circuit settling time, and T_{sc} represents the channel switching time. The expression for total conversion time T_{cv} is:

$$T_{cv} = T_s + (T_{cv\_ch2} + T_{sc}) + (T_{cv\_ch3} + T_{sc}) + (T_{cv\_mch23} + T_{sc}) \qquad (5)$$

In equation (5):

The calculation of $T_{cv_chx}$is detailed in formula (4).

6.3.5. Status and Overflow

The status register is used to query the chip's current operating state. When in capacitance conversion or temperature conversion mode, the corresponding flag bit is set to 1. The chip also features data overflow protection. Since the DATA register's upper limit is 65535, overflow may occur when f_{in}frequency is low and FINCNT count is large. Data overflow can be detected by checking the overflow flag register. Writing a 1 to the OF_CLEAR bit in the status register clears the data overflow flag. Relevant registers are shown in the table below.

Table 6.3.5 Overflow Flag Register

Register	Address	Bit	Description
OSC1_OF_MSB	0x18	MOF[4:0] OFREF OF[9:8]	MOFx: 1 indicates mutual capacitance channel x count overflow, where x ranges from 0 to 4 OFREF: 1 indicates count overflow in single-ended reference channel OFx: 1 indicates count overflow for single-ended channel x, where x ranges from 0 to 9
OSC1_OF_LSB	0x19	OF[7:0]	OFx: 1 indicates single-ended channel x count overflow, where x ranges from 0 to 7

OSC2_OF	0x1A	DOFREF DOF[4:0]	DOFREF: 1 indicates a two-ended reference channel count overflow DOFx: 1 indicates overflow in dual-ended channel x, where x ranges from 0 to 4

Table 6.3.5 Status Registers

Register	Address	Bit	Description
STATUS	0x1B	OF_CLEAR	Writing a 1 to this bit clears all overflow flags. The read value is 0.
		FLAG_TCVT	1 indicates a temperature conversion is in progress. 0 indicates temperature conversion has stopped.
		FLAG_CCVT	1 indicates capacitance conversion is in progress. In cyclic mode, this flag remains high until a stop command is issued. 0 indicates capacitance conversion is stopped.

6.3.6. Clock Configuration

Registers related to the MC1081 clock configuration include CNT_CFG and DIV_CFG. The configuration process is as follows:

i. Determine the conversion time $_{T(CV)}$based on application requirements. Generally, longer conversion times yield higher measurement accuracy. Alternatively, increasing the number of averages can reduce noise levels and improve effective resolution.

ii. Estimate the oscillation frequency $_{f(sensor)}$based on the maximum capacitance value of the $_{sensor}$, circuit connection method, oscillation mode, drive strength, and oscillation amplitude (note that estimated values may differ from actual measured frequencies due to non-ideal factors). The estimation formula for $f_{sensor}$is as follows:

$$T_{half} = K_r \cdot (C + C_p) \cdot ln\left(\frac{v_{drv}+v_{amp}}{v_{drv}-v_{amp}}\right) + 8 \times 10^{-9} \quad (6)$$

$$f_{sensor} = 1/2T_{half} \quad (7)$$

In Equations (6) and (7):

- T_{half}represents the half-oscillation period;
- C is the estimated capacitance value of the device under test;
- $C_p$is the equivalent parasitic capacitance of the chip I/O, typically estimated at 6 pF;

- The values of drive voltage amplitudes v_{drv} ,振荡幅度v_{amp} , and 电流系数K_r depend on the configuration.

Details are shown in the table below, where OSC1_VTH[2:0] and OSC2_VTH[2:0] denote the amplitude configuration of the oscillation register.

Single-ended mode: OSC_SEL=0			Balanced Mode: OSC_SEL=1		
OSC1_VTH[2:0]	V_{amp}	V_{drv}	OSC2_VTH[2:0]	V_{amp}	V_{drv}
000	0.2	2	000	0.2	2
001	0.4	2	001	0.4	2
010	0.8	2	010	0.6	2
2011	1.2	2	011	0.8	2
100	VDD-2.2	VDD	100	1.0	2
101	VDD-1.6	VDD	101	1.2	2
110	VDD-1.2	VDD	110	1.2	2
111	VDD-0.8	VDD	111	1.2	2

Note: VDD is the chip's supply voltage.

I[3:0]	K_r	Drive Current
0000	2.56e5	4μA
0001	1.28e5	8μA
0010	6.4e4	16μA
0011	2.4×10^4	42μA
0100	1e4	100μA
0101	4e3	250μA
0110	2e3	500μA
0111	1e3	1000μA
1xxx	5e2	2000μA

iii. Since the upper limit of DATA's count value is 65535, $FINCN_{T(MAX)}$can be estimated using the following formula after determining NDIVin, NDIVref, and f_{sensor}. Typically, FINCNT=0.5 $FINCNT_{MAX}$. The factor of 0.5 is applied to account for design margin against non-ideal factors such as parasitic effects and temperature drift. For higher precision, the data averaging count C_AVG can be set to 32.

$$FINCNT_{MAX} = (FREF\_DIV \cdot Dx \cdot f_{sensorx}) / (FIN\_DIV \cdot f_{sys}) \quad (8)$$

In equation (8):

$FINCNT_{MAX}$represents the maximum number of measurement cycles for f_{in};

FREF_DIV is the system clock division ratio, as detailed in Table 6.3.1 Clock

Configuration Register;

FIN_DIV is the signal-under-test (SUT) division ratio.

iv. If conversion time is constrained, typically set NDIVref = 1, CAG = 1, and configure the measured signal settling as SETTLING = 0. $FINCNT_{MAX}$can be estimated using the following formula. Generally, take FINCNT = 0.5 $FINCNT_{MAX}$. Note that T_{cv_chx}in the formula represents the conversion time for a single channel, not the total duration T_{cv}. The calculation of $T_{cv_chx}$is detailed in Formula (4).

$$FINCNT_{MAX} = \left(T_{cv_{chx}} \cdot f_{sensorx}\right) \Big/ NDIV_{in} - N_s, \ N_s = 1 \quad (9)$$

In equation (9),

Ns represents the number of signal settling cycles. Refer to Table 6.3.4-2 for measurement cycle count and settling time configuration registers.

v. Combine the results from iii and iv to select the smallest value for FINCNT. Simultaneously determine parameters such as FIN_DIV, FREF_DIV, SETTLING, and C_AVG.

vi. When measuring mutual capacitance, three measurements are required. When setting FINCNT, select the smallest value. The measurement duration for one mutual capacitance channel is the sum of the three measurements.

6.3.7. Data Acquisition and Capacitance Calculation

Data for each channel is shown in the table below.

Table 6.3.7 Data Registers

Register	Address	Bit	Description		
			Single-ended (OSC_SEL=0)	Mutual Capacitance (OSC_SEL=0)	Dual-Ended (OSC_SEL=1)
D0_MSB D0_LSB	0x02 0x03	DATA[15:8] DATA[7:0]	Channel CH0 Data		Channel DCH0 Data
D1_MSB D1_LSB	0x04 0x05	DATA[15:8] DATA[7:0]	Channel CH1 Data	Channel MCH0 Data	Channel DCH1 Data
D2_MSB D2_LSB	0x06 0x07	DATA[15:8] DATA[7:0]	Channel CH2 Data		Channel DCH2 Data
D3_MSB D3_LSB	0x08 0x09	DATA[15:8] DATA[7:0]	Channel CH3 Data	Channel MCH1 Data	Channel DCH3 Data
D4_MSB D4_LSB	0x0A 0x0B	DATA[15:8] DATA[7:0]	Channel CH4 Data		Channel DCH4 Data
D5_MSB D5_LSB	0x0C 0x0D	DATA[15:8] DATA[7:0]	Channel CH5 Data	Channel MCH2 Data	Invalid

D6_MSB D6_LSB	0x0E 0x0F	DATA[15:8] DATA[7:0]	Channel CH6 Data		Invalid
D7_MSB D7_LSB	0x10 0x11	DATA[15:8] DATA[7:0]	Channel CH7 Data	Channel MCH3 Data	Invalid
D8_MSB D8_LSB	0x12 0x13	DATA[15:8] DATA[7:0]	Channel CH8 Data		Invalid
D9_MSB D9_LSB	0x14 0x15	DATA[15:8] DATA[7:0]	Channel CH9 Data	Channel MCH4 Data	Invalid
DREF_MSB DREF_LSB	0x16 0x17	DATA[15:8] DATA[7:0]	Channel CHREF Data		Channel CHREF Data

Note that in single-ended mode, when mutual capacitance measurement is enabled, the valid data for MCHx is located in registers D1, D3, D5, D7, and D9. In differential mode, the valid data for DCHx is located in registers D0, D1, D2, D3, D4, and DREF.

The data read from the above table represents the channel's count value, with the corresponding frequency conversion formula as follows.

$$f_{sensorx} = \left(FIN\_DIV \cdot f_{sys} \cdot FIN\_CNT\right) / \left(FREF\_DIV \cdot Dx\right) \qquad (10)$$

In Equation (10):

- FIN_DIV is the internal frequency division factor for measuring the channel oscillation frequency; refer to Table 6.3.1 Clock Configuration Register for details;
- $f_{sys}$is the internal system clock frequency of the chip, which is 19.2 MHz;
- FIN_CNT is the number of measurement cycles for f_{in}, as detailed in Table 6.3.4-2 Measurement Cycle Count and Settling Time Configuration Register;
- FREF_DIV is the system clock division factor; refer to Table 6.3.1 Clock Configuration Register for details;
- Dx is the frequency count value read from the data register for each channel (x denotes the selected channel, applicable to single-ended capacitance, mutual capacitance, and differential capacitance). Refer to Table 6.3.7 Data Registers for details.

To ensure correct data acquisition in a single measurement, data must be read after conversion completes. For single measurements, the FLAG_CCVT bit in the status register indicates whether the current measurement is complete. For cyclic and continuous measurements, the chip automatically measures at fixed intervals; users need only read data at an appropriate time.

In practical applications, the reference measurement method is employed to eliminate the effects of non-ideal factors such as drift. This method requires all measurement channels and the reference channel to be configured identically. For reference channel selection, refer to Section 6.3.8.

The specific measurement calculation methods are as follows:

Method 1: Using the internal reference capacitance channel (applicable to single-ended capacitance, mutual capacitance, and differential capacitance)

i. Measure and read *the* frequency count *value Dx* for *channel x*

ii. Under identical configurations, measure and read the frequency count *value DREF* of the internal reference channel.

iii. Calculate the capacitance value $_{C(x)\ using}$ the following formula.$_{Note}$that *the* internal *reference capacitance* $C_{ref}$is 20 pF.

$$C_x = \left(C_{ref} \cdot Dx\right) / DREF$$

Method 2: Using an external reference capacitor (applicable to single-ended capacitance and mutual capacitance)

i. Select one channel (e.g., single-ended channel CH7, corresponding to pin C7), connect *the external* reference *capacitor* C_{ref}, and connect other channels to the electrodes or the capacitance under test. The size of the external reference capacitor should be as close as possible to the capacitance under test.

ii. Measure and read the frequency count value Dx for channel x.

iii. Measure and read the frequency count value D7 for channel CH7.

iv. Calculate the capacitance value using the following formula

$$C_x = \left(C_{ref} \cdot Dx\right) / D7$$

Method 3: Using a Single External Reference Capacitor (Applicable to Balanced Capacitors)

i. Select one channel (e.g., differential channel DCH3, corresponding to pins C6 and C7), connect *an external* reference *capacitor* C_{ref}, and connect the other channels to electrodes or the capacitance under test. The value of the external reference capacitor should be as close as possible to that of the capacitance under test.

ii. Measure and read *the* frequency count *value Dx* for *channel x*

iii. Measure and read the frequency count *value D3* for channel DCH3

iv. Calculate the capacitance value using the following formula

$$C_x = \left(C_{ref} \cdot Dx\right) / D3$$

Method 4: Using two external reference capacitors (suitable for single-ended capacitance and mutual capacitance)

i. Select one channel (e.g., single-ended channel CH6, corresponding to pin C6) and connect *an* external *reference capacitor* C_{ref1}. Select a second channel (e.g., single-ended channel CH7, corresponding to pin C7) *and* connect *an external reference capacitor* C_{ref2}. Connect other channels to the electrode or the capacitance under test. *Require* C_{ref1}*= 2**C_{ref2}. The size*of the* external *reference capacitor* C_{ref1}should be as close as possible to the capacitance being measured.

ii. Measure and calculate the period of channel x. $T_{sensorx} = 1/f_{sensorx}$

iii. Measure and calculate the period of reference channel 6. $T_{cref1} = 1/f_{sensor6}$

iv. Measure and calculate the period of reference channel 7. $T_{cref2} = 1/f_{sensor7}$

v. Calculate the time correction parameter,$T_{fix} = 2T_{cref2} - T_{cref1}$

vi. correct the period of reference channel 6,$T_{cref1\_fix} = T_{cref1} - T_{fix}$

vii. Correct the period of the measurement channel $T_{sensorx\_fix} = T_{sensorx} - T_{fix}$

viii. Calculate the capacitance value according to the following formula

$$C_x = \left(C_{ref1} \cdot T_{sensorx\_fix}\right) / T_{cref1\_fix}$$

Method 5: Use two external reference capacitors (suitable for differential capacitance)

i. Select one channel (e.g., dual-ended channel DCH3, corresponding to pins C6 and C7) and connect external *reference capacitor* C_{ref1}; select a second channel (e.g., dual-ended channel DCH4, corresponding to pins C8 and C9) and connect *external reference capacitor* C_{ref2}. Connect other channels to electrodes or the capacitance under test. *Require* C_{ref1}*= 2**C_{ref2}. The value*of the* external *reference capacitor* C_{ref1}should be as close as possible to the capacitance being measured.

ii. Measure and calculate the period of channel x $T_{sensorx} = 1/f_{sensorx}$

iii. Measure and calculate the period of reference channel DCH3. $T_{cref1} = 1/f_{sensor3}$

iv. Measure and calculate the period of reference channel DCH4. $T_{cref2} = 1/f_{sensor4}$

v. Calculate the time correction parameter: `$T_{fix} = 2T_{cref2} - T_{cref1}$ `

vi. Correct the period of reference channel DCH3: $T_{cref1\_fix} = T_{cref1} - T_{fix}$

vii. Correct the period of the measurement channel $T_{sensorx\_fix} = T_{sensorx} - T_{fix}$

viii. Calculate the capacitance value using the following formula

$$C_x = \left(C_{ref1} \cdot T_{sensorx\_fix}\right) / T_{cref1\_fix}$$

Among the five methods above, Methods 1, 2, and 4 are applicable to single-ended capacitance and mutual capacitance; Methods 1, 3, and 5 are applicable to differential capacitance. Methods 1, 2, and 3 are susceptible to parasitic capacitance. Methods 4 and 5 offer the highest measurement accuracy.

6.3.8. Reference Capacitor Selection

The MC1081's reference capacitance can be selected from the built-in capacitor, an external capacitor, or an electrode structure.

For general applications, the internal 20 pF capacitor Cref can be used as the reference capacitor. In this case, all 10 single-ended or 5 differential channels can be utilized for measurement.

For applications requiring temperature drift compensation, an external capacitor or electrode structure can be selected as the reference. For single-ended measurements, channel CH7 is recommended as the reference channel. For differential measurements, channel DCH3 is recommended as the reference channel.

For applications requiring high-precision measurement, two external capacitors can be selected as the reference. For single-ended measurements, it is recommended to use channels CH6 and CH7 as reference channels. For differential measurements, it is recommended to use channels DCH3 and DCH4 as reference channels.

6.3.9. Active Shielding

The MC1081 provides an Active Shielding function to eliminate the effects of surrounding parasitic capacitance. When the measured electrode is at the same potential as the surrounding shielding layer, no charge transfer occurs between them, and the parasitic capacitance has no effect on the measured electrode. As shown in Figure 6.3.3-1, cap1 represents the electrode under test. cap0, cap2, and the metal layer (shield) form the active shielding layer. The shield drive circuit (BUF) is implemented using the internal unity-gain op-amp within the chip. The SHLD, $C_{(n)}$,and $C_{(n+2)}$pins output identical waveforms, i.e., Vcap1 = Vshield = Vcap0 = Vcap2. This configuration effectively counters interference on the electrode surface without compromising sensitivity.

Configure the SHLD_CFG register bits CS[1:0]=1X and set SHLD_EN=1 to enable active shielding. If the capacitive load of the shielded electrode is relatively large, configure SHLD_HP=1 to activate high-power drive mode.

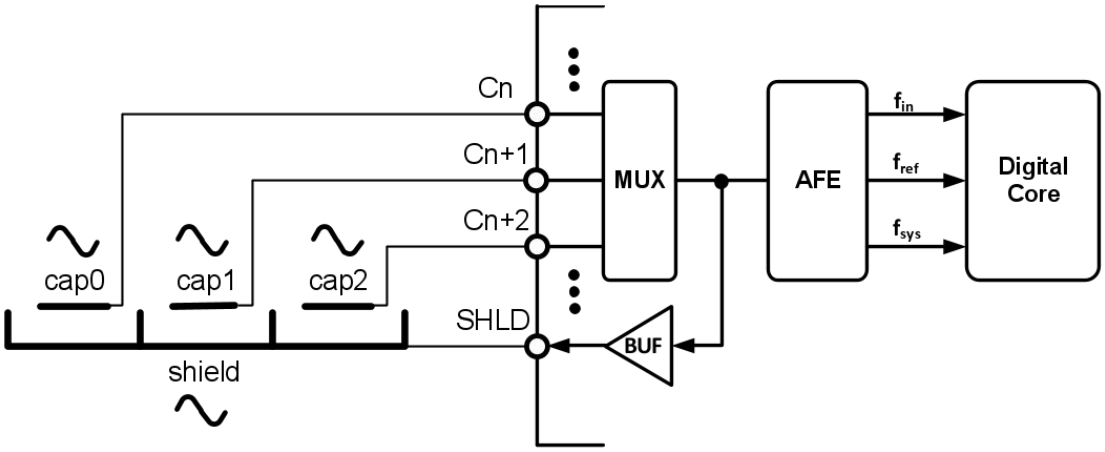


Figure 6.3.9 Active Shielding Function ( )

When using the active shielding function, note the following:

i. Active shielding can only be enabled in single-ended capacitive mode. Mutual capacitance and differential capacitance modes do not support active shielding.

ii. The maximum signal frequency supported by active shielding is f_{sensor}= 500 kHz.

iii. Active shielding drives operate in either high-power mode or low-power mode, with differences in the maximum capacitive and minimum resistive loads they can drive.

The register for configuring active shielding is SHLD_CFG. Specific register descriptions are shown in the table below.

Table 6.3.9 Active Shielding Configuration Register

Register	Address	Bit	Description
SHLD_CFG	0x26	CS[1:0]	Capacitance measurement port status bit during non-measurement periods 00: Indicates the capacitance measurement port is in a high-impedance state during non-measurement periods 01: Indicates the capacitance measurement port is grounded during non-measurement periods 1x: Indicates the capacitance measurement port outputs an active shield signal during non-measurement periods
		SHLD_HP	0: Indicates low-power mode, driving a maximum load of 30pF 1: Indicates high-power mode, driving a maximum load

			of 60pF
		SHLD_EN	0: Disables active shielding 1: Enable active shielding

6.3.10. Temperature Measurement

The MC1081 incorporates a high-precision temperature sensing function with a measurement range of -55°C to +125°C. Temperature measurement accuracy across the full range is ±2°C. The temperature value can be used for temperature drift compensation in capacitive sensing channels.

6.3.10.1. Temperature Measurement Parameter Configuration

The chip generates a voltage signal proportional to temperature internally. This signal is converted by a 16-bit ADC and output to the temperature data register. Setting bit STC in the temperature measurement configuration register initiates a single temperature conversion cycle. Configuring the TCVT bit allows setting the duration of a single conversion cycle; longer conversion times yield higher effective resolution. The temperature conversion process and capacitance conversion process operate independently and do not interfere with each other. The temperature measurement configuration register is described as follows:

Table 6.3.10-1 Temperature Measurement Configuration Register

Register	Address	Bit	Description
T_CMD	0x1C	TCVT[1:0]	Temperature Conversion Time Configuration Bit 00: 1.7ms, corresponding to 13-bit effective resolution 01: 2.1ms, corresponding to 14-bit effective resolution 10: 3.0ms, corresponding to 15-bit effective resolution 11: 4.7ms, corresponding to 16-bit effective resolution
		STC	Temperature Conversion Start Bit 0: Stop conversion 1: Initiate single conversion, read value is 0

6.3.10.2. Temperature Data Format and Calculation Formula

Temperature data format is 16-bit signed number, T_{LSB}= 0.0038 °C. Register description follows:

Table 6.3.10-2 Temperature Data Register

Register	Address	Bit	Description
T_MSB T_LSB	0x0 0x1	TDATA[15:8] TDATA[7:0]	Temperature data, 16-bit signed number

The temperature value calculation formula is:

$$Temperature = \frac{TDATA[15:0]}{255} + 28.7\,℃$$

6.3.11. Power Consumption Modes

The MC1081 has three power consumption states: Standby Mode, Active Mode, and Sleep Mode.

Upon power-up, the MC1081 automatically configures registers to default values and enters Standby Mode. During this state, internal power supplies and the system clock remain active, awaiting user-initiated parameter configuration and measurement conversion commands via I2C.

After each I²C read/write operation, the MC1081 automatically enters Sleep Mode. During this state, internal power supplies and the system clock are disabled, representing the lowest power consumption mode.

Upon receiving a valid I2C command from the host, the chip automatically wakes up, executes the corresponding operation, and enters the operational mode. Note that in periodic measurement mode, the MC1081 enters standby mode after each conversion completes, not sleep mode.

6.3.12. Software Reset

The MC1081 provides a software reset (Soft-Reset) function. Writing 0x7A to the reset register activates the software reset, restoring the sensor to its initial state upon power-up and resetting all registers to their default values.

Table 6.3.12 Reset Register

Register	and Address	Bit	Description
RESET	0x69	RESET[7:0]	b01111010: Initiates software reset, restoring the sensor to its initial state upon power-up and resetting all registers to default values. Other values: Invalid. Read value is 0x00.

7. I2C Interface

The MCU accesses the MC1081's control and data registers via the I2C interface. The SDA and SCL pins incorporate spike suppression circuits to reduce the impact of bus noise. The MC1081 supports an I2C communication rate of 400KHz. The I2C interface's data line (SDA) and clock line (SCL) are connected to the corresponding ports of the host processor. Each line is connected to VDD via a pull-up resistor R_P, enabling read/write control of each node chip through host software. The address of the slave device can be set via the ADDR pin value according to the specific application.

7.1. I2C Address Selection

The MC1081S achieve different I2C addresses through varying configurations of the ADDR pin. The specific correspondence is detailed in the table below.

Table 7.1 I2C Address Truth Table

ADDR Connection Configuration	I2C Address
Connected to GND	0x70
Connected to VDD	0x71
Connect to SDA	0x72
Connect to SCL	0x73

The I2C address of the MC1081L is 0x71.

7.2. I2C Interface Data Format

Typical I2C bus operation is defined as follows:

Bus idle: Both SDA and SCL remain high.

Start Data Transmission: When SCL is high, a change in SDA state (from high to low) indicates a start condition. Each data transmission begins with a start condition.

End of Data Transfer: When SCL is high, a change in the state of SDA (from low to high) indicates the stop condition. Each data transfer ends with a repeated start or stop condition.

Data Transfer: The number of data bytes transferred between start and stop conditions is unrestricted and determined by the master device. The receiver acknowledges the data transfer.

Acknowledgment: Each receiving slave device must generate an acknowledgment

signal when addressed. The slave acknowledgment must stabilize SDA at a low level during the rising edge of the acknowledgment clock pulse. On the master side, data transmission termination is achieved by the master not acknowledging the last byte transmitted by the slave.

For I2C bus communication, the host first transmits the slave address and write flag (Slave Address + W), followed immediately by the register logical address (Register Address). For read operations, the master subsequently transmits the slave address and read flag (Slave Address + R). The slave then sends data from the register to the master. Upon receiving an ACK from the master, the slave may proceed to send the next byte of data. If the master responds with a NACK, the slave must cease sending data. For write operations, the master directly transmits data to the slave (Data to Register). Note that the slave address width is 7 bits, with the write flag W=0 and the read flag R=1. The specific read/write timing diagrams are as follows:

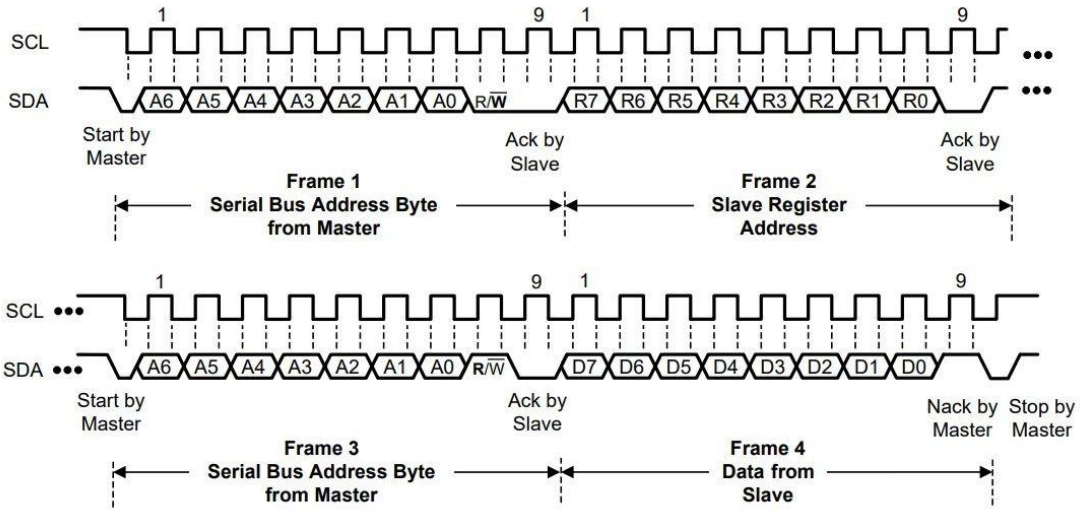
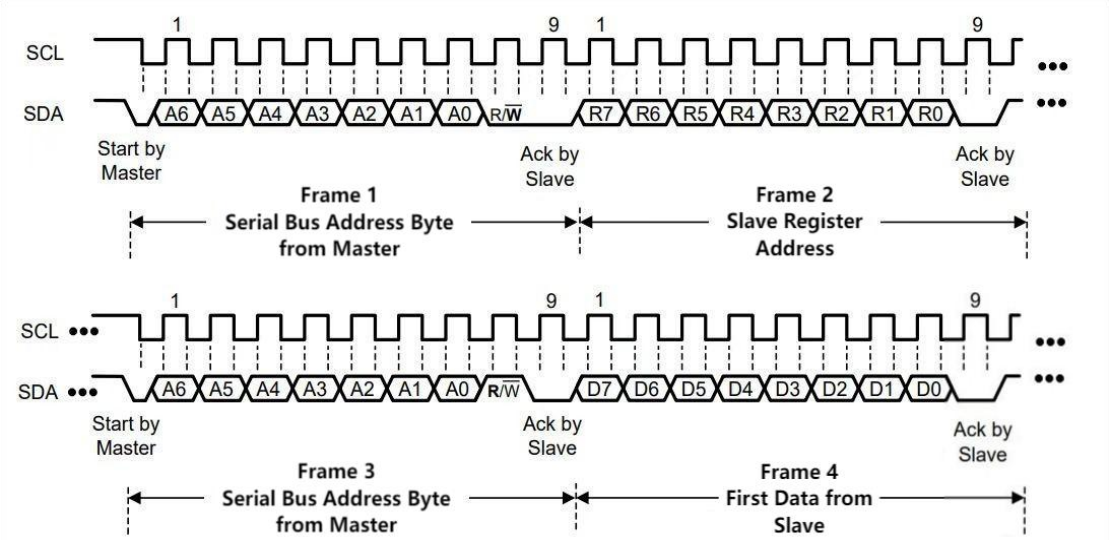


Figure 7.2-1 I2C Read Timing



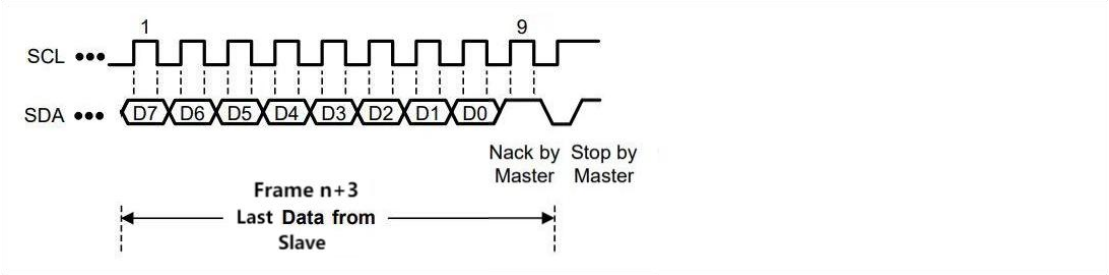


Figure 7.2-2 I2C Continuous Read Timing

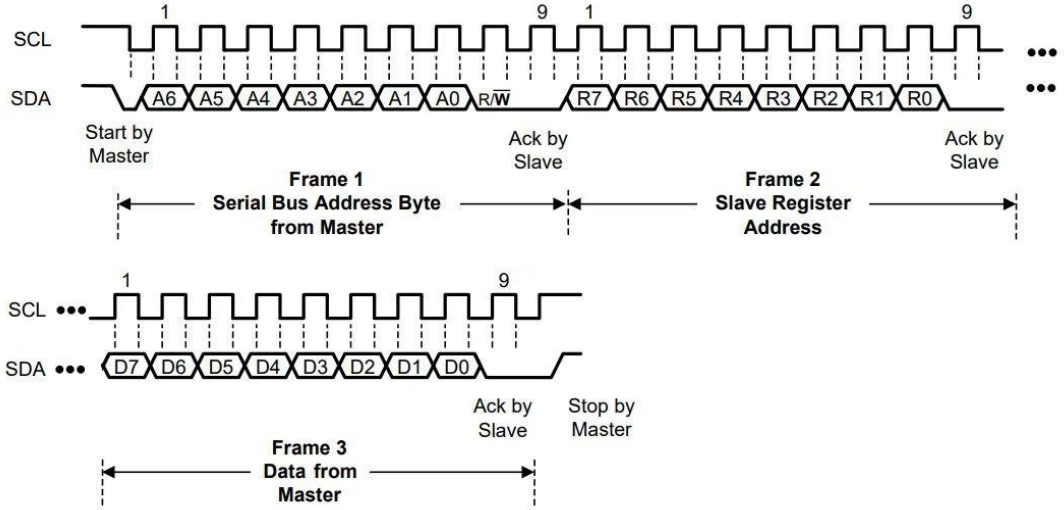


Figure 7.2-3 I2C Write Timing

8. Register Description

8.1. Register List

The MC1081 registers are categorized into three types: read/write, read-only, and write-only. Default values represent the initial state upon sensor power-up. The following is the complete register list.

Table 8.1 Register List

Address	Name	Default Value	Description		
0x00	T_MSB	0x00	Temperature data, read-only		
0x01	T_LSB	0x00			
			OSC_SEL=0		OSC_SEL=1
			MCHx=0	MCHx=1	
0x02	D0_MSB	0x00	Single-ended channel 0 frequency		Dual-ended channel 0 frequency
0x03	D0_LSB	0x00			

			count value, read-only		count value, read-only
0x04	D1_MSB	0x00	Single-ended Channel 1 Frequency Count Value, Read Only	Mutual Capacitance Channel 0 Frequency Count Value, Read-Only	Dual-ended Channel 1 Frequency Count Value, Read-only
0x05	D1_LSB	0x00			
0x06	D2_MSB	0x00	Single-ended Channel 2 Frequency Count Value, Read-only		Dual-ended Channel 2 Frequency Count Value, Read-only
0x07	D2_LSB	0x00			
0x08	D3_MSB	0x00	Single-ended Channel 3 Frequency Count Value, Read-only	Mutual Capacitance Channel 1 Frequency Count Value, Read-Only	Dual-ended Channel 3 Frequency Count Value, Read-only
0x09	D3_LSB	0x00			
0x0A	D4_MSB	0x00	Single-ended Channel 4 Frequency Count Value, Read-only		Dual-ended Channel 4 Frequency Count Value, Read-only
0x0B	D4_LSB	0x00			
0x0C	D5_MSB	0x00	Single-ended Channel 5 Frequency Count Value, Read-only	Mutual capacitance channel 2 frequency count value, read-only	Invalid
0x0D	D5_LSB	0x00			
0x0E	D6_MSB	0x00	Single-ended Channel 6 Frequency Count Value, Read Only		Invalid
0x0F	D6_LSB	0x00			
0x10	D7_MSB	0x00	Single-ended Channel 7 Frequency Count Value, Read-only	Mutual capacitance channel 3 frequency count value, read-only	Invalid
0x11	D7_LSB	0x00			
0x12	D8_MSB	0x00	Single-ended channel 8 frequency count value, read-only		Invalid
0x13	D8_LSB	0x00			

0x14	D9_MSB	0x00	Single-ended Channel 9 Frequency Count Value, Read-only	Mutual capacitance channel 4 frequency count value, read-only	Invalid
0x15	D9_LSB	0x00			
0x16	DREF_MSB	0x00	Internal Reference Channel Frequency Count Value, Read-Only	Internal reference channel frequency count value, read-only	Internal reference channel frequency count value, read-only
0x17	DREF_LSB	0x00			
0x18	OSC1_OF_MSB	0x00	Single-ended mode channel data overflow flag, read-only		
0x19	OSC1_OF_LSB	0x00			
0x1A	OSC2_OF	0x00	Dual-ended mode channel data overflow flag, read-only		
0x1B	STATUS	0x00	Data conversion flag and overflow flag cleared, read/write		
0x1C	T_CMD	0x80	Temperature measurement control, read/write		
0x1D	C_CMD	0x55	Capacitance measurement control, read/write		
0x1E	CNT_CFG	0x3F	fin Count cycle setting, range 0~255, read/write		
0x1F	DIV_CFG	0x00	Clock signal division configuration, read/write		
0x20	OSC1_CHS_MSB	0x04	Single-ended mode channel selection, read/write		
0x21	OSC1_CHS_LSB	0x01			
0x22	OSC1_MCHS	0x00	Single-ended mode mutual capacitance channel selection, read/write		
0x23	OSC1_CFG	0x42	Single-ended mode parameter configuration, read/write		
0x24	OSC2_DCHS	0x21	Dual-ended mode channel selection, read/write		
0x25	OSC2_CFG	0x21	Dual-ended mode parameter configuration, read/write		
0x26	SHLD_CFG	0x40	Active masking configuration, read/write		
0x69	RESET	0x00	Software reset, write-only		
0x7E	CHIP_ID_MSB	0x10	Chip ID, read-only		
0x7F	CHIP_ID_LSB	0x81			

8.2. T_MSB, T_LSB

T_MSB (0x00) & T_LSB (0x01) Description

Bit	Bit Definition	Operation	Default Value	Description
15:8	TDATA[15:8]	Read-only	0000 0000	16-bit temperature data, signed number
7:0	TDATA[7:0]	Read-	0000	

		only	0000	

8.3. D0_MSB, D0_LSB

D0_MSB (0x02) & D0_LSB (0x03) Description

Bit	Bit Definition	Operation	Default Value	Description
15:8	D0[15:8]	Read-only	0000 0000	16-bit Data OSC_SEL=0 indicates the frequency count value for single-ended channel 0. OSC_SEL=1 indicates the frequency count value for differential channel 0.
7:0	D0[7:0]	Read-only	0000 0000	

8.4. D1_MSB, D1_LSB

D1_MSB (0x04) & D1_LSB (0x05) Description

Bit	Bit Definition	Operation	Default Value	Description
15:8	D1[15:8]	Read-only	0000 0000	16-bit Data OSC_SEL=0 indicates the frequency count value for single-ended channel 1. When MCH0=1, indicates the frequency count value for mutual capacitance channel 0. OSC_SEL=1 indicates the frequency count value for differential channel 1.
7:0	D1[7:0]	Read-only	0000 0000	

8.5. D2_MSB, D2_LSB

D2_MSB (0x06) & D2_LSB (0x07) Description

Bit	Bit Definition	Operation	Default Value	Description
15:8	D2[15:8]	Read-only	0000 0000	16-bit Data OSC_SEL=0 indicates the frequency count value for single-ended channel 2. OSC_SEL=1 indicates the frequency count value for differential channel 2.
7:0	D2[7:0]	Read-only	0000 0000	

8.6. D3_MSB, D3_LSB

D3_MSB (0x08) & D3_LSB (0x09) Description

Bit	Bit Definition	Operation	Default Value	Description

15:8	D3[15:8]	Read-only	0000 0000	16-bit Data OSC_SEL=0 indicates the frequency count value for single-ended channel 3. When MCH1=1, indicates the frequency count value for mutual capacitance channel 1. OSC_SEL=1 indicates the frequency count value for differential channel 3.
7:0	D3[7:0]	Read-only	0000 0000	

8.7. D4_MSB, D4_LSB

D4_MSB (0x0A) & D4_LSB (0x0B) Description

Bit	Bit Definition	Operation	Default Value	Description
15:8	D4[15:8]	Read-only	0000 0000	16-bit Data OSC_SEL=0 indicates the frequency count value for single-ended channel 4. OSC_SEL=1 indicates the frequency count value for differential channel 4.
7:0	D4[7:0]	Read-only	0000 0000	

8.8. D5_MSB, D5_LSB

D5_MSB (0x0C) & D5_LSB (0x0D) Description

Bit	Bit Definition	Operation	Default Value	Description
15:8	D5[15:8]	Read-only	0000 0000	16-bit Data OSC_SEL=0 indicates the frequency count value for single-ended channel 5. When MCH2=1, indicates the frequency count value for mutual capacitance channel 2.
7:0	D5[7:0]	Read-only	0000 0000	

8.9. D6_MSB, D6_LSB

D6_MSB (0x0E) & D6_LSB (0x0F) Description

Bit	Bit Definition	Operation	Default Value	Description
15:8	D6[15:8]	Read-only	0000 0000	16-bit Data OSC_SEL=0 indicates the frequency count value for single-ended channel 6.
7:0	D6[7:0]	Read-only	0000 0000	

8.10. D7_MSB, D7_LSB

D7_MSB (0x10) & D7_LSB (0x11) Description

Bit	Bit Definition	Operation	Default Value	Description
15:8	D7[15:8]	Read-only	0000 0000	16-bit Data OSC_SEL=0 indicates the frequency count value for single-ended channel 7. When MCH3=1, indicates the frequency count value for mutual capacitance channel 3.
7:0	D7[7:0]	Read-only	0000 0000	

8.11. D8_MSB, D8_LSB

D8_MSB (0x12) & D8_LSB (0x13) Description

Bit	Bit Definition	Operation	Default Value	Description
15:8	D8[15:8]	Read-only	0000 0000	16-bit Data OSC_SEL=0 indicates the frequency count value for single-ended channel 8.
7:0	D8[7:0]	Read-only	0000 0000	

8.12. D9_MSB, D9_LSB

D9_MSB (0x14) & D9_LSB (0x15) Description

Bit	Bit Definition	Operation	Default Value	Description
15:8	D9[15:8]	Read-only	0000 0000	16-bit Data OSC_SEL=0 indicates the frequency count value for single-ended channel 9. When MCH4=1, indicates the frequency count value for mutual capacitance channel 4.
7:0	D9[7:0]	Read-only	0000 0000	

8.13. DREF_MSB, DREF_LSB

DREF_MSB (0x16) & DREF_LSB (0x17) Description

Bit	Bit Definition	Operation	Default Value	Description
15:8	DREF[15:8]	Read-only	0000 0000	16-bit Data Represents the frequency count value of the reference channel.
7:0	DREF[7:0]	Read-only	0000 0000	

8.14. OSC1_OF_MSB, OSC1_OF_LSB

OSC1_OF_MSB (0x18) & OSC1_OF_LSB (0x19) Description

Bit	Bit Definition	Operation	Default	Description
15:11	MOF[4:0]	Read-only	0000 0000	MOFx: 1 indicates a count value overflow for mutual capacitance channel x.
10	OFREF			1 indicates overflow in the count value of the single-ended reference channel.
9:8	OF[9:8]			OFx: 1 indicates count overflow for single-ended capacitance channel x.
7:0	OF[7:0]	Read-only	0000 0000	

8.15. OSC2_OF

OSC2_OF (0x1A) Description

Bit	Bit Definition	Operation	Default Value	Description
7:6	RSV	Read-only	0000 0000	Reserved
5	DOFREF			1 indicates overflow in the count value of the dual-ended reference channel.
4:0	DOF[4:0]			DOFx: 1 indicates overflow in the count value of dual-ended capacitance channel x.

8.16. STATUS

STATUS (0x1B) Description

Bit	Bit Definition	Operation	Default Value	Description
7:5	RSV	Read-only	0000 0000	Reserved
4	OF_CLEAR	Read/Write		Write 1 to clear all overflow flags; read value is 0.
3:2	RSV	Read Only		Reserved bit
1	FLAG_TCVT			1 indicates ongoing temperature conversion. 0 indicates stopped temperature conversion.
0	FLAG_CCVT			1 indicates capacitance conversion is in progress. In cyclic mode, this flag remains high until a stop command is issued. 0 indicates capacitance conversion is stopped.

8.17. T_CMD

T_CMD (0x1C) Description

Bit	Bit Definition	Operation	Default Value	Description
7:6	RSV	Read/Write	1000 0000	Reserved bit, writeable only 10
5:4	TCVT[1:0]			Temperature measurement conversion time configuration 00: 1.7ms 01: 2.1ms 10: 3.0ms 11: 4.7ms
3:1	RSV			Reserved bit, can only be written as 000
0	STC			Temperature conversion start bit 0: Stop conversion; 1: Start single conversion Read value is 0

8.18. C_CMD

C_CMD (0x1D) Description

Bit	Bit Definition	Operation	Default Value	Description
7	OSC_SEL	Read/Write	0101 0101	Oscillation Mode Selection 0: Select single-ended mode; 1: Select differential mode
6	SLEEP_EN			Chip Sleep Mode Switch 0: Sleep mode disabled; 1: Sleep mode enabled
5:4	CAVG[1:0]			Frequency Count Value Dx Average Count 00: 1 time 01: 4 times 10: 8 times 11: 32 times
3:2	CR[1:0]			Cycle Conversion Interval Configuration 00: Measure once every 10 seconds 01: Measure once per second 10: Measure every 0.1 seconds 11: Continuous uninterrupted measurement, no interval

1:0	OS, SD			Capacitance conversion start bit 00: Periodic conversion 10: Periodic conversion 01: Stop Conversion 11: Single conversion

8.19. CNT_CFG

CNT_CFG (0x1E) Description

Bit	Bit Definition	Operation	Default Value	Description
7:0	FINCNT[7:0]	Read/Write	0011 1111	Set the number of measurement cycles N for fin 0x00: Measure the duration of 1 fin cycle 0x01~0xFF: Measure the duration of N fin cycles, N=1~255

8.20. DIV_CFG

DIV_CFG (0x1F) Description

Bit	Bit Definition	Operation	Default Value	Description
7	SETTLING	Read/Write	0000 0000	Set the number of fin establishment cycles 0: Indicates the setup time for one fin cycle 1: Represents the setup time for 4 fin cycles
6:4	FINDIV[2:0]			Channel signal division ratio NDIVin 000: No frequency division 001: 2x division 010: 4-way division 011: 8-way division 100: 16-way division 101: 32-way crossover 110: 64-way crossover 111: 64-way crossover
3:2	RSV			Reserved bit, can only be written as 00
1:0	FREFDIV[1:0]			Reference clock division ratio NDIVref 00: No division 01: Divide by 2 10: Divide by 4 11: Divide by 8

8.21. OSC1_CHS_MSB & OSC1_CHS_LSB

OSC1_CHS_MSB (0x20) & OSC1_CHS_LSB (0x21) Description

Bit	Range	Operation	Default	Description
15:11	RSV	Read/Write	0000 0100	Reserved bit, can only be written as 00000
10	CH_REF			1 indicates measurement of single-ended reference channel, 0 indicates no measurement of single-ended reference channel
9:8	CH[9:8]		0000 0001	CHx: 1 indicates measurement of single-ended channel x, 0 indicates no measurement of single-ended channel x
7:0	CH[7:0]			

8.22. OSC1_MCHS

OSC1_MCHS (0x22) Description

Bit	Range	Operation	Default	Description
7:5	RSV	Read/Write	0000 0000	Reserved bit, can only be written as 000
4:0	MCH[4:0]			Mutual Capacitance Measurement Start Configuration 0 indicates mutual capacitance measurement is disabled for the corresponding channel. When CH0 and CH1 are set to 1, MCH0=1 indicates mutual capacitance measurement is initiated for the C0-C1 channel. Measurement data is written to the D1 data register. When CH2 and CH3 are set to 1, MCH1=1 indicates mutual capacitance measurement is initiated for the C2-C3 channel. Measurement data is written to the D3 data register. When CH4 and CH5 are set to 1, MCH2=1 indicates mutual capacitance measurement is initiated for the C4-C5 channel. Measurement data is written to the D5 data register. When CH6 and CH7 are set to 1, MCH3=1 indicates initiation of mutual capacitance measurement for the C6-C7 channel. Measurement data is written to the D7 data register. When CH8 and CH9 are set to 1, MCH4=1 indicates initiation of mutual capacitance

				measurement for the C8-C9 channel. Measurement data is written to the D9 data register.

8.23. OSC1_CFG

OSC1_CFG (0x23) Description

Bit	Range	Operation	Default	Description
7	OSC1_LDO	Read/Write	0100 0010	Internal LDO Power Mode Selection for Single-Ended Mode 0: Low-power mode, suitable for f_{sensor} < 1MHz 1: High-power mode, suitable for fsensor > 1MHz
6:4	OSC1_V[2:0]			Single-Ended Mode Oscillation Amplitude Configuration 000: Amplitude 0.2V (Internal LDO Power Supply) 001: Amplitude 0.4V (Internal LDO power supply) 010: Amplitude 0.8V (Internal LDO power supply) 011: Amplitude 1.2V (Internal LDO power supply) 100: Amplitude is VDD-2.2V (VDD power supply) 101: Amplitude of VDD-1.6V (VDD supply) 110: Amplitude of VDD-1.2V (VDD supply) 111: Amplitude of VDD-0.8V (VDD supply)
3:0	OSC1_I[3:0]			Single-ended mode drive current configuration

				0000: Drive current is 4uA 0001: Drive current is 8μA 0010: Drive current is 16μA 0011: Drive current is 42μA 0100: Drive current is 100μA 0101: Drive current is 250 μA 0110: Drive current is 500μA 0111: Drive current is 1000μA 1xxx: Drive current is 2000μA

8.24. OSC2_DCHS

OSC2_DCHS (0x24) Description

Bit	Range	Operation	Default Value	Description
7:6	RSV	Read/Write	0010 0001	Reserved bit, can only be written as 00
5	DCH_REF			1 indicates measurement of dual-ended reference channel, 0 indicates no measurement of dual-ended reference channel
4:0	DCH[4:0]			DCHx: 1 indicates measurement of differential channel x, 0 indicates no measurement of differential channel x

8.25. OSC2_CFG

OSC2_CFG (0x25) Description

Bit	Range	Operation	Default	Description
7	OSC2_LDO	Read/Write	0010 0001	Dual-Mode Internal LDO Power Mode Selection 0: Low-power mode, suitable for f_{sensor} < 1MHz 1: High-power mode, suitable for fsensor > 1MHz
6:4	OSC2_V[2:0]			Dual-End Mode Oscillation Amplitude Configuration 000: Amplitude 0.4V 001: Amplitude 0.8V 010: Amplitude 1.2V 011: Amplitude is 1.6V 100: Amplitude is 2.0V 101: Amplitude of 2.4V 110: Amplitude of 2.4V

				111: Amplitude of 2.4V All options utilize internal LDO power supply
3:0	OSC2_I[3:0]			Dual-Ended Mode Oscillation Drive Current Configuration 0000: Drive current is 4uA 0001: Drive current is 8μA 0010: Drive current is 16μA 0011: Drive current is 42μA 0100: Drive current is 100μA 0101: Drive current is 250 μA 0110: Drive current is 500 μA 0111: Drive current is 1000μA 1xxx: Drive current is 2000μA

8.26. SHLD_CFG

SHLD_CFG (0x26) Description

Bit	Range	Operation	Default	Description
7:6	CS[1:0]	Read/Write	0100 0000	Capacitance Measurement Port State Selection During Non-Measurement Period 00: Indicates the capacitance measurement port is in a high-impedance state during non-measurement periods. 01: Indicates the capacitance measurement port is grounded during non-measurement periods. 1x: Indicates the capacitance measurement port outputs an active shield signal during non-measurement periods (enhanced active shielding function). This is only active when OSC_SEL=0 and SHLD_EN=1; otherwise, the measurement port automatically enters high-impedance state during non-measurement periods.
5:2	RSV			Reserved bit, can only be written as 0000
1	SHLD_HP			Active Shielding Mode Selection 0 indicates low-power mode, 1 indicates

				high-power mode
0	SHLD_EN			Active Shielding Function Enable Bit 0 Disables active shielding, 1 Enables active shielding

8.27. RESET

RESET (0x69) Description

Bit	Range	Operation	Default	Description
7:0	RESET[7:0]	Read/Write	0000 0000	01111010: Initiate software reset. The sensor returns to its initial state upon power-up, and all registers revert to default values. Other values: Invalid This byte reads as 0x00

8.28. CHIPID_MSB, CHIPID_LSB

CHIPID_MSB (0x7E) & CHIPID_LSB (0x7F) Description

Bit	Range	Operation	Default	Description
15:8	CHIPID[15:8]	Read-only	0001 0000	Chip ID: 0x10, 0x81
7:0	CHIPID [7:0]	Read-only	1000 0001	

9. Typical Application Circuit Diagram

The typical application circuit for the MC1081 in single-ended mode is shown in Figure 9-1.

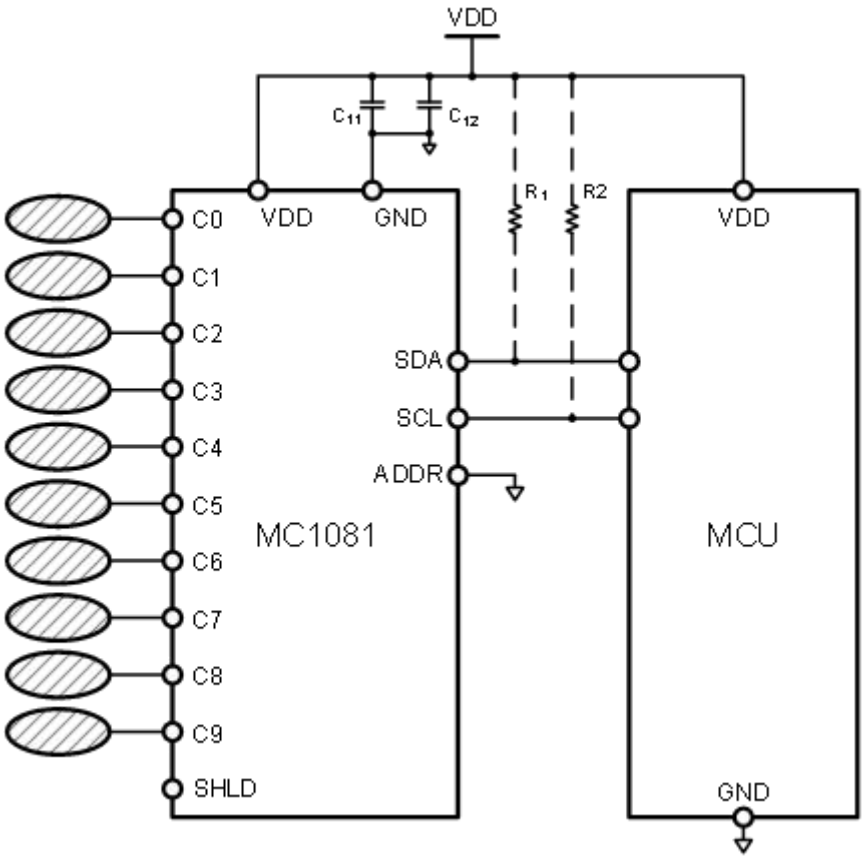


Figure 9-1 MC1081 Single-Ended Mode Typical Application Circuit Diagram

Pins C0 to C9 are connected to the single-ended electrodes, with the internal 20pF capacitor selected as the reference capacitor. The pin assignments shown are merely one example. In actual applications, pins can be assigned as needed to connect single-ended electrodes, mutual capacitance electrodes, or external capacitors. For detailed specifications, refer to Section 6.3.2. The recommended value for capacitor C11 is 100nF, and for capacitor C12 is 10uF. R1 and R2 are I2C pull-up resistors. The MC1081's SDA and SCL pins incorporate internal 10K pull-up resistors, making R1 and R2 optional. The address select pin ADDR supports four connection methods; the diagram above shows it grounded. For detailed specifications, refer to Section 6.4.1.

Refer to Figure 9-1 for instructions on chip configuration, measurement, and data reading:

1) Configure the CNT_CFG register. The default value is 0x3F, indicating a count of 63 cycles.
2) Configure the DIV_CFG register. The default value is 0x00, indicating no clock division.
3) Configure the OSC1_CFG register. The default value is 0x42, indicating an oscillation amplitude of 2.8V and a drive current of 16uA when powered by 5V.
4) Configure the channel selection register. Set OSC1_CHS_MSB=0x07 and OSC1_CHS_LSB=0xFF to select all channels.

5) Configure the C_CMD register to initiate capacitance measurement. Write 0x53 to perform a single-shot measurement of single-ended capacitance with 4-averaging.
6) Configure the T_CMD register to initiate temperature measurement. Write 0x01 to perform a single-shot temperature measurement.
7) Read the STATUS register to determine if conversion is complete. FLAG_CCVT being 1 indicates capacitance conversion is in progress. FLAG_TCVT being 1 indicates temperature conversion is in progress.
8) After conversion completes, read the temperature data and frequency count data. The specific registers are T, D0 to D9, and DREF.

A typical application circuit for the MC1081 dual-ended mode is shown in Figure 9-2.

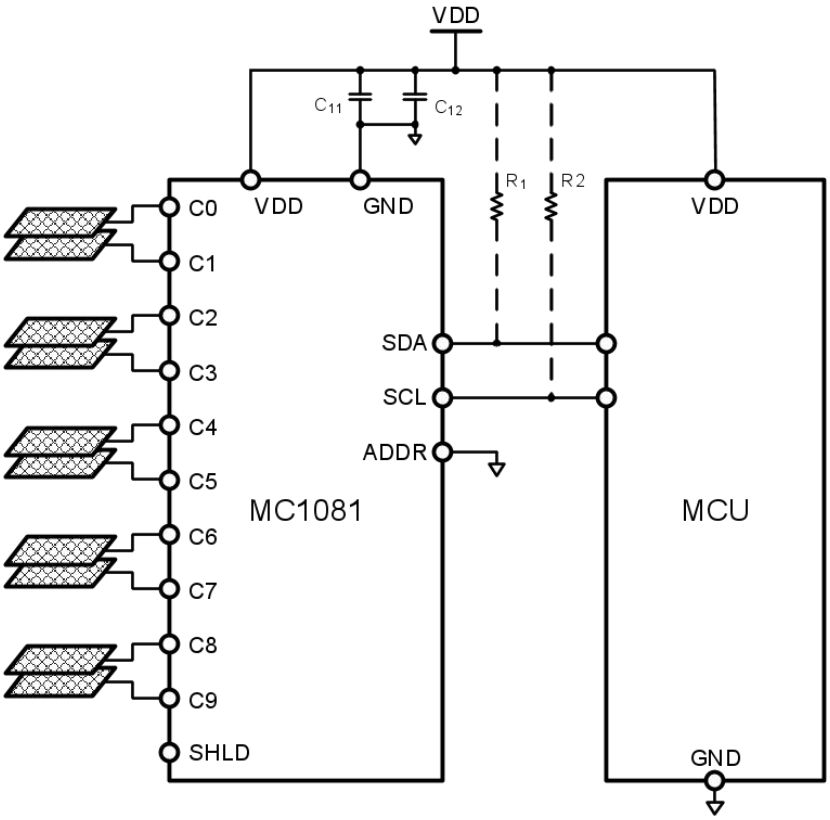


Figure 9-2 Typical Application Circuit Diagram for MC1081 Dual-Ended Mode

Here, C0 and C1, C2 and C3, C4 and C5, C6 and C7, C8 and C9 are connected to the dual-ended electrodes, with the internal 20pF capacitor selected as the reference capacitor. In practical applications, dual-ended electrodes or external capacitors can be connected as needed. Refer to Section 6.3.2 for detailed specifications. The recommended value for capacitor C11 is 100nF, and for capacitor C12 is 10uF. R1 and R2 serve as I2C pull-up resistors. The MC1081's SDA

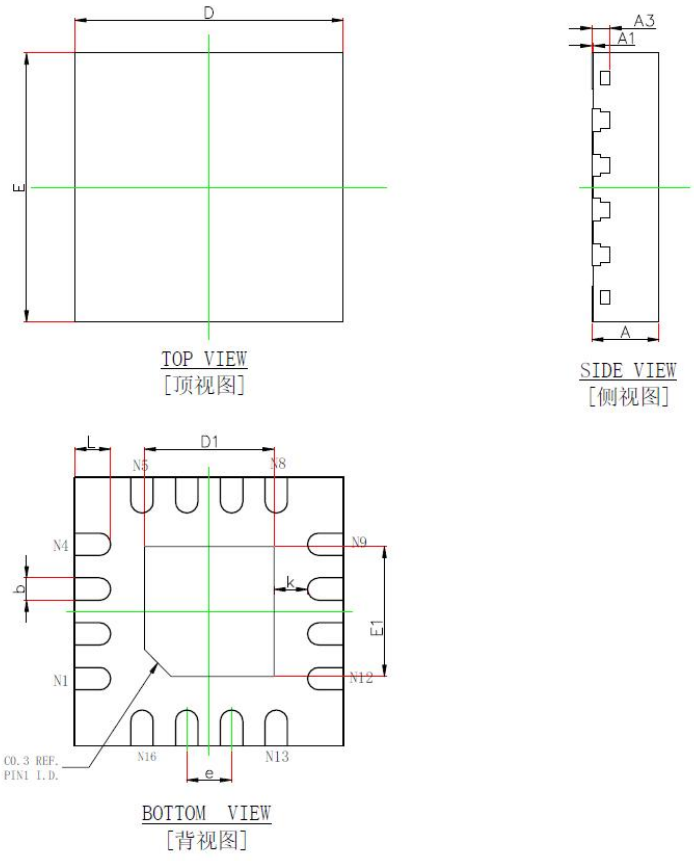
and SCL pins incorporate internal 10kΩ pull-up resistors, making R1 and R2 optional. The address select pin ADDR has four connection methods; the diagram above shows it grounded. For detailed specifications, refer to Section 6.4.1.

Refer to Figure 9-2 for instructions on chip configuration, measurement, and data reading:

1) Configure the CNT_CFG register. The default value is 0x3F, indicating a count of 63 cycles.
2) Configure the DIV_CFG register. The default value is 0x00, indicating no clock division.
3) Configure the OSC2_CFG register. The default value is 0x21, indicating an amplitude of 1.2V and a drive current of 8uA.
4) Configure the channel selection register. Set OSC2_DCHS = 0xD3F to select all channels.
5) Configure the C_CMD register to initiate capacitance measurement. Write 0xD3 to perform a single measurement of a dual-ended capacitance with 4-averaging.
6) Write 0x01 to the T_CMD register to perform a single temperature measurement.
7) Read the STATUS register to determine if conversion is complete. FLAG_CCVT being 1 indicates capacitance conversion is in progress. FLAG_TCVT being 1 indicates temperature conversion is in progress.
8) After conversion completes, read the temperature data and frequency count data. The specific registers are T, D0 to D4, and DREF.

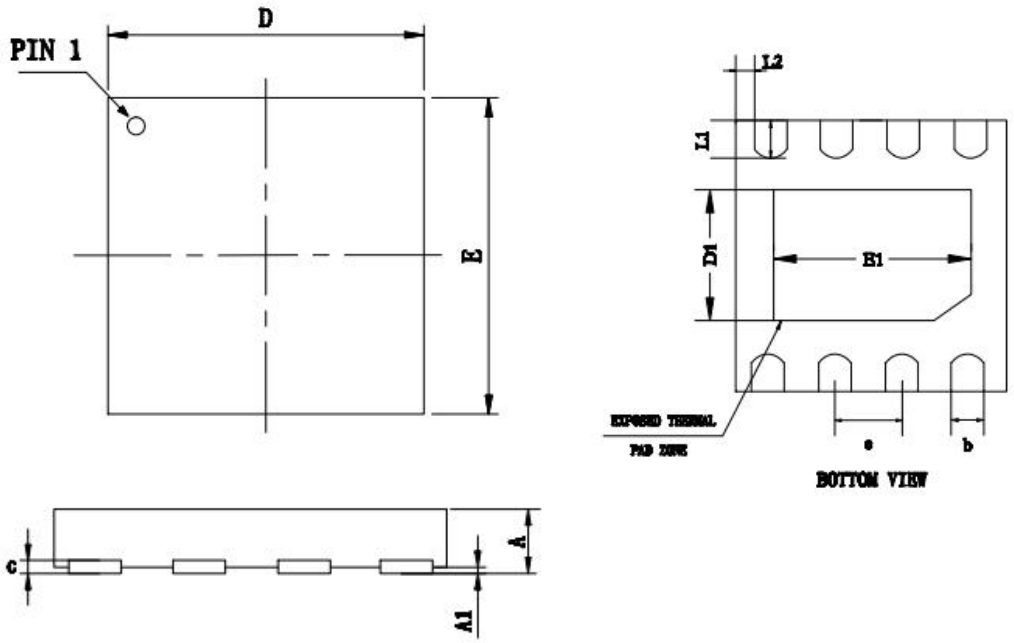
10. Package

10.1. MC1081S QFN16 3.0*3.0*0.75mm Product Dimension Specification Diagram



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.350	1.550	0.053	0.061
E1	1.350	1.550	0.053	0.061
k	0.375REF.		0.015REF.	
b	0.200	0.300	0.008	0.012
e	0.500BSC.		0.020BSC.	
L	0.300	0.500	0.012	0.020

10.2. MC1081L DFN8 2.0*2.0*0.55mm Product Dimension Drawing



SYMBOL	MIN	NOM	MAX
A	0.5	0.55	0.6
A1	-	0.02	0.05
b	0.23	0.25	0.27
c	0.13	0.15	0.2
D	1.9	2.0	2.1
D1	0.87	0.89	0.91
e	0.5BSC		
E	1.9	2.0	2.1
E1	1.48	1.5	1.52
L1	0.2	0.3	0.4
L2	0.105	0.125	0.145

11. Ordering Information

Part Number	Package Type	Package Qty
MC1081S	QFN16	5000
MC1081L	DFN8	3000