

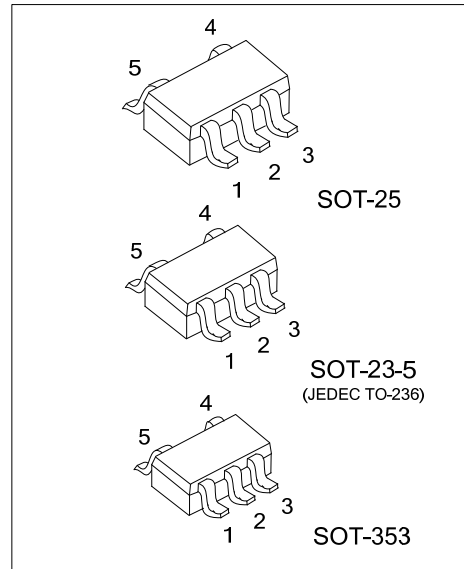
**U74LVC1G126****CMOS IC****BUS BUFFER/LINE DRIVER;
3-STATE****DESCRIPTION**

The **U74LVC1G126** is single bus buffer/line driver with 3-state output. The output is disabled When the output enable (OE) is low. When OE is high, true data is will pass A input to the Y output.

This device has power-down protective circuit preventing device from destruction when it is powered down.

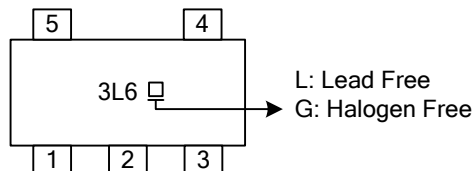
FEATURES

- * Operate From 1.65V to 5.5V
- * Inputs Accept Voltages to 5.5V
- * High Noise Immunity
- * Low Power Dissipation
- * Direct Interface With TTL level

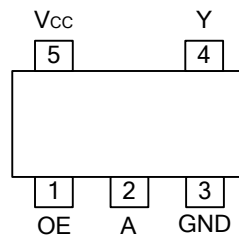
**ORDERING INFORMATION**

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC1G126L-AE5-R	U74LVC1G126G-AE5-R	SOT-23-5	Tape Reel
U74LVC1G126L-AF5-R	U74LVC1G126G-AF5-R	SOT-25	Tape Reel
U74LVC1G126L-AL5-R	U74LVC1G126G-AL5-R	SOT-353	Tape Reel

U74LVC1G126G-AE5-R	(1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) AE5: SOT-23-5, AF5: SOT-25, AL5: SOT-353 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING

■ PIN CONFIGURATION

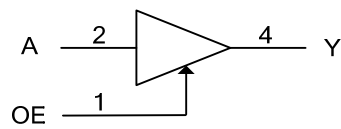


■ FUNCTION TABLE

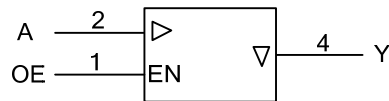
INPUT(OE)	INPUT(A)	OUTPUT(Y)
H	L	L
H	H	H
L	X	Z

Note: H: HIGH voltage level; L: LOW voltage level; X=don't care; Z=high-impedance OFF-state.

■ LOGIC DIAGRAM (Positive Logic)



Logic Symbol



IEC Logic Symbol

■ ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{CC}	-0.5 ~ +6.5	V
Input Voltage		V_{IN}	-0.5 ~ +6.5	V
Output Voltage	Enable mode	V_{OUT}	-0.5 ~ $V_{CC} + 0.5$	V
	Disable mode		-0.5 ~ +6.5	V
	Power-down mode		-0.5 ~ +6.5	V
V_{CC} or GND Current		I_{CC}	±100	mA
Continuous Output Current ($V_{OUT}=0$ to V_{CC})		I_{OUT}	±50	mA
Input Clamp Current ($V_{IN}<0$)		I_{IK}	-50	mA
Output Clamp Current ($V_{OUT}>V_{CC}$ or $V_{OUT}<0$)		I_{OK}	±50	mA
Power Dissipation ($T_A=-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$)	SOT-23-5	P_D	300	mW
	SOT-25		360	
	SOT-353		250	
Operating Temperature		T_{OPR}	-40 ~ +125	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-65 ~ +150	$^{\circ}\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		5.5	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}	$V_{CC}=1.65\text{V} \sim 5.5\text{V}$; Enable mode	0		V_{CC}	V
		$V_{CC}=1.65\text{V} \sim 5.5\text{V}$; Disable mode	0		5.5	V
		$V_{CC}=0\text{V}$; Power-Down Mode	0		5.5	V
Input Transition Rise or Fall Rate	t_R / t_F	$V_{CC}=1.65\text{V} \sim 2.7\text{V}$			20	ns/V
		$V_{CC}=2.7\text{V} \sim 5.5\text{V}$			10	ns/V

■ ELECTRICAL CHARACTERISTICS ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	$V_{CC}=1.65\text{V} \sim 1.95\text{V}$	$0.65 \times V_{CC}$			V
		$V_{CC}=2.3\text{V} \sim 2.7\text{V}$	1.7			V
		$V_{CC}=2.7\text{V} \sim 3.6\text{V}$	2			V
		$V_{CC}=4.5\text{V} \sim 5.5\text{V}$	$0.7 \times V_{CC}$			V
Low-Level Input Voltage	V_{IL}	$V_{CC}=1.65\text{V} \sim 1.95\text{V}$			$0.35 \times V_{CC}$	V
		$V_{CC}=2.3\text{V} \sim 2.7\text{V}$			0.7	V
		$V_{CC}=2.7\text{V} \sim 3.6\text{V}$			0.8	V
		$V_{CC}=4.5\text{V} \sim 5.5\text{V}$			$0.3 \times V_{CC}$	V
High-Level Output Voltage	V_{OH}	$V_{CC}=1.65 \sim 5.5\text{V}$, $I_{OH}=-100\mu\text{A}$	$V_{CC}-0.1$			V
		$V_{CC}=1.65\text{V}$, $I_{OH}=-4\text{mA}$	1.2			V
		$V_{CC}=2.3\text{V}$, $I_{OH}=-8\text{mA}$	1.9			V
		$V_{CC}=2.7\text{V}$, $I_{OH}=-12\text{mA}$	2.2			V
		$V_{CC}=3.0\text{V}$, $I_{OH}=-24\text{mA}$	2.3			V
		$V_{CC}=4.5\text{V}$, $I_{OH}=-32\text{mA}$	3.8			V
Low-Level Output Voltage	V_{OL}	$V_{CC}=1.65 \sim 5.5\text{V}$, $I_{OL}=100\mu\text{A}$			0.1	V
		$V_{CC}=1.65\text{V}$, $I_{OL}=4\text{mA}$			0.45	V
		$V_{CC}=2.3\text{V}$, $I_{OL}=8\text{mA}$			0.3	V
		$V_{CC}=2.7\text{V}$, $I_{OL}=12\text{mA}$			0.4	V
		$V_{CC}=3.0\text{V}$, $I_{OL}=24\text{mA}$			0.55	V
		$V_{CC}=4.5\text{V}$, $I_{OL}=32\text{mA}$			0.55	V

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=5.5V$, $V_{IN}=5.5V$ or GND		± 0.1	± 5	μA
Power OFF Leakage Current	I_{OFF}	$V_{CC}=0V$, V_{IN} or $V_{OUT}=5.5V$		± 0.1	± 10	μA
3-State Output OFF-State Current	I_{OZ}	$V_{CC}=5.5V$, $V_{IN}=V_{IH}$ or V_{IL} , $V_{OUT}=V_{CC}$ or GND		± 0.1	± 10	μA
Quiescent Supply Current	I_{CC}	$V_{CC}=5.5V$, $V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$		0.1	10	μA
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	$V_{CC}=2.3 \sim 5.5V$, $V_{IN}=V_{CC}-0.6V$, $I_{OUT}=0$		5	500	μA

■ SWITCHING CHARACTERISTICS ($T_A=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay From Input A to Output Y	t_{PLH} / t_{PHL}	$C_L=30pF$, $V_{CC}=1.8\pm 0.15V$, $R_L=1K\Omega$	1.0	3.0	8.0	ns
		$V_{CC}=2.5\pm 0.2V$, $R_L=500\Omega$	0.5	2.1	5.5	ns
		$C_L=50pF$, $R_L=500\Omega$, $V_{CC}=2.7V$	0.5	2.3	5.5	ns
		$V_{CC}=3.3\pm 0.3V$	0.5	2.0	4.5	ns
		$V_{CC}=5\pm 0.5V$	0.5	1.7	4.0	ns
3-State Output Enable Time From Input OE to Output Y	t_{PZH} / t_{PZL}	$C_L=30pF$, $V_{CC}=1.8\pm 0.15V$, $R_L=1K\Omega$	1.0	3.2	9.4	ns
		$V_{CC}=2.5\pm 0.2V$, $R_L=500\Omega$	0.5	2.2	6.6	ns
		$C_L=50pF$, $R_L=500\Omega$, $V_{CC}=2.7V$	0.5	2.4	6.6	ns
		$V_{CC}=3.3\pm 0.3V$	0.5	2.1	5.3	ns
		$V_{CC}=5\pm 0.5V$	0.5	1.6	5.0	ns
3-State Output Disable Time From Input OE to Output Y	t_{PLZ} / t_{PLH}	$C_L=30pF$, $V_{CC}=1.8\pm 0.15V$, $R_L=1K\Omega$	1.0	4.3	9.2	ns
		$V_{CC}=2.5\pm 0.2V$, $R_L=500\Omega$	0.5	2.7	5.5	ns
		$C_L=50pF$, $R_L=500\Omega$, $V_{CC}=2.7V$	0.5	3.4	5.5	ns
		$V_{CC}=3.3\pm 0.3V$	0.5	3.0	5.5	ns
		$V_{CC}=5\pm 0.5V$	0.5	2.2	4.2	ns

From Output

C_L

R_L

R_L

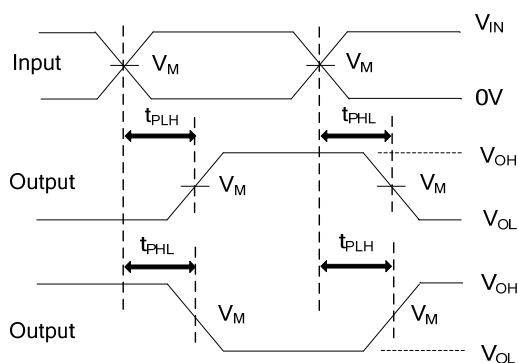
S

V_{LOAD}

- Open
- GND

TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	V_{LOAD}

V _{CC}	INPUTS		V _M	V _{LOAD}	V _Δ	C _L	R _L
	V _{IN}	t _R , t _F					
1.8V±0.15V	V _{CC}	≤2ns	V _{CC} /2	2×V _{CC}	0.15V	30pF	1KΩ
2.5V±0.2V	V _{CC}	≤2ns	V _{CC} /2	2×V _{CC}	0.15V	30pF	500Ω
2.7V	2.7V	≤2.5ns	1.5V	6V	0.3V	50pF	500Ω
3.3V±0.3V	2.7V	≤2.5ns	1.5V	6V	0.3V	50pF	500Ω
5V±0.5V	V _{CC}	≤2.5ns	V _{CC} /2	2×V _{CC}	0.3V	50pF	500Ω



Timing diagram for a 1T1C SRAM cell. The diagram shows the input signal V_{IN} and the output signal $V_{LOAD/2}$ over time. The input signal transitions between V_M and $0V$. The output signal transitions between V_{OL} and V_{OH} . The diagram illustrates the propagation delay t_{PZL} and t_{PLZ} for the low-to-high transition, and t_{PZH} and t_{PHZ} for the high-to-low transition. The output signal is shown with a delay t_{PZL} and t_{PLZ} relative to the input signal.

ENABLE AND DISABLE TIMES

2. All input pulses are supplied by generators having the following characteristics: $P_{RR} \leq 10\text{MHz}$, $Z_0 = 50\Omega$.

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