XPA5108D3R

Dual Adjustable Voltage Monitor with Reset and Gate Driver Outputs

Description

The XPA5108D3R is a dual-voltage monitor and sequencer that is ideal for use in a wide variety of multi-voltage application. The device has a fixed-sense threshold voltage and two adjustable sense input that can be configured by two external resistors. Sequence timing is also programmable by external capacitor. A charge-pump circuit is also implemented for external N-MOSFET load switch gate control. The gate control sequence timing is also programmable by external capacitor as well.

As the voltage at each monitored input exceeds its respective threshold, the output goes high after a propagation delay or a capacitor-set time delay. When a voltage falls below its threshold, the output goes low after a propagation delay.

The XPA5108 is available in a small package, WDFN-10L 3x3.

Applications

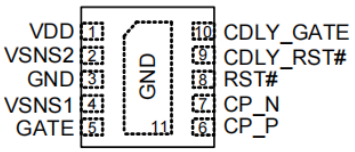
- Multi-Voltage Systems
- DC-DC Supplies
- Servers/Workstations
- Storage Systems
- Networking/Telecommunication Equipment

Features

- Operates from VDD= 3V to 16V
- Dual Adjustable Threshold Down to 0.6V
- ±1.5% VSNS High-Accuracy Threshold Voltage
- Push-Pull Reset Output with Capacitor-Adjustable Delay Time
- Gate Driver Output with Capacitor-Adjustable Delay Time
- Temperature Range: −40°C to 125°C
- Small Package: WDFN-10L 3x3

Pin Configuration

(TOP VIEW)



WDFN-10L 3x3

Typical Application Circuit

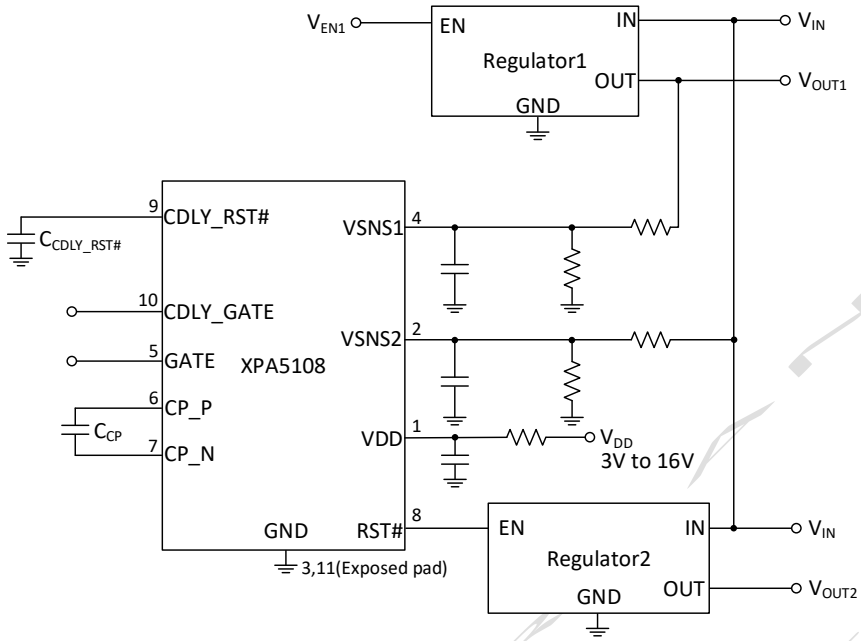


Figure 1. General Application (Sequential control between 2 regulators)

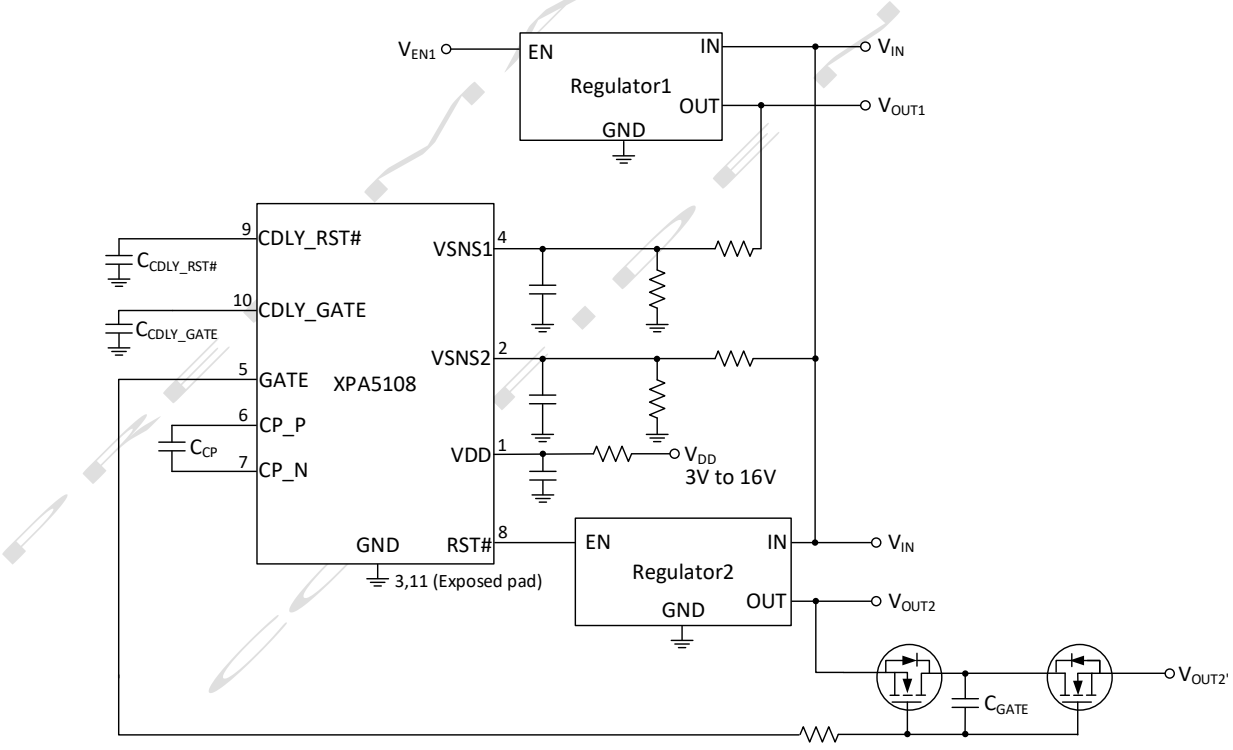
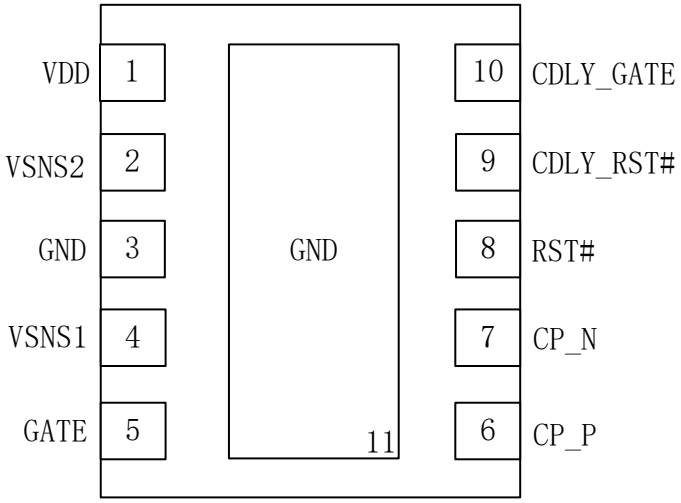


Figure 2. Application with External Switches to Control Regulator's Output Connection

PIN Configuration and Description



Top View

Pin	Name	Description
1	VDD	Power input, in the range of 3V to 16V.
2	VSNS2	Voltage sense input 2.
3,11 (Exposed pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
4	VSNS1	Voltage sense input 1.
5	GATE	Gate driver output from charge pump circuitry. VGATE = 2 x VCC
6	CP_P	Charge pump capacitor positive node.
7	CP_N	Charge pump capacitor negative node.
8	RST#	Push-pull reset output. RST# is normally low, and assets HIGH when both VSNS1 and VSNS2 rise above threshold voltage.
9	CDLY_RST#	Capacitor-adjustable delay input for RST# pin. Connect an external capacitor from CDLY_RST# to GND to set the RST# pin delay period. Leave CDLY_RST# open for internal propagation delay.
10	CDLY_GATE	Capacitor-adjustable delay input for GATE pin. Connect an external capacitor from CDLY_GATE to GND to set the GATE pin delay period. Leave CDLY_GATE open for internal propagation delay.

Operation

The XPA5108 is designed to provide supervisory and sequencing functions for multi-voltage systems. Once the VDD voltage is higher than the POR threshold, the XPA5108 starts monitoring VSNS1 and VSNS2. When both VSNS1 and VSNS2 are higher than V_{TH_VSNS} , an internal current source of 1uA will be activated and sourcing out to charge an external capacitor at CDLY_RST# pin. The push-pull RST# asserts HIGH when the voltage CDLY_RST# pin is higher than VTH_RST# (1.234V typ.). Once RST# is deasserted, another 1uA current source will be activated to charge an external capacitor at CDLY_GATE. Once the CDLY_GATE pin voltage rises above VTH_GATE (1.234V typ.), a voltage level of 2xVCC is output at the GATE pin for driving an external N-MOSFET load switch. Designer can program the delay timing of RST# & GATE by choosing the capacitors of CDLY_RST# and CDLY_GATE.

Comparators

Comparators are used to compare V_{VSNS1} and V_{VSNS2} with a VSNS1/VSNS2 threshold voltage V_{TH_VSNS} (typ. 0.6V).

Power-On Reset (POR)

Power-On Reset (POR) occurs when V_{VDD} rises above 2.5V, the XPA5108 resets fault latch and gets ready for operation.

Oscillator

A built-in oscillator generates a clock signal for an internal charge pump.

Charge Pump

A charge pump is integrated to provide gate drive control for turning on external N-type MOSFET load switch. The gate voltage is 2xVDD. Consideration should be taken to ensure VGATE is sufficiently high to turn on the external MOSFET regarding the application. The recommended C_{CP} capacitor value is ranging from 1nF to 1uF.

Regulators

The XPA5108 works over a wide V_{DD} ranging from 3V to 16V. An internal regulator is designed to regulate the internal V_{CC} at 5V. The regulator tracks V_{DD} and operates in low dropout mode if V_{DD} is lower than 5V.

Push-Pull Reset Output

RST# is normally low, and asserts HIGH after a capacitor-adjustable delay time when both of the monitored voltage VSNS1 and VSNS2 rise above the threshold voltage.

GATE Output

Capacitor-Adjustable Delay Input for GATE pin. Connect an external capacitor from CDLY_GATE to GND to set the GATE pin delay period. Leave CDLY_GATE open for internal propagation delay.

Over-Temperature Protection

The XPA5108 includes an Over-Temperature Protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down timer and charge pump function when junction temperature exceeds a thermal shutdown threshold TSD. Once the junction temperature cools down by a thermal shutdown hysteresis (ΔT_{SD}), the IC will resume normal operation.

Absolute Maximum Ratings

Parameter	Min	Max	Units
VDD	-0.3	29	V
VSNSx	-0.3	3.5	V
CP_P,GATE	-0.3	12.6	V
ALL Other Pins	-0.3	6	V
Power Dissipation, P_D@T_A=25°C			
WDFN-10L 3x3	-	3.27	W
Lead Temperature (Soldering, 10 sec.)	-	260	°C
Junction Temperature	-	150	°C
Storage Temperature Range	-65	150	°C
ESD Susceptibility HBM (Human Body Model) CDM (Charged Device Model)	 - -	 2 1	 kV kV

Note: (1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note: (2) Devices are ESD sensitive. Handling precaution is recommended.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
VSNS1,VSNS2	-	0		3	V
Supply Input Voltage	V_{DD}	3		16	V
Junction Temperature	T_J	-40		+125	°C

Note: (3) The device is not guaranteed to function outside its operating conditions.

Thermal Information

Parameter	Symbol	Typ	Units
Junction-to-Ambient Thermal Resistance	θ_{JA}	30.5	°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	7.5	°C/W

Note: (4) θ_{JA} is measured under natural convection (still air) at TA = 25°C with the component mounted on a high effective thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

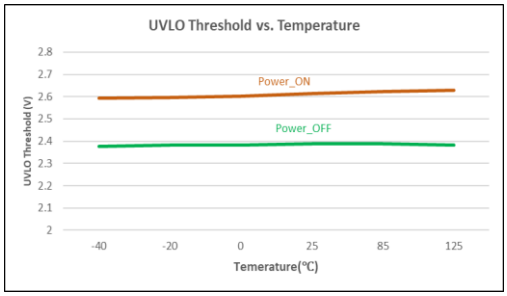
Electrical Characteristics

(V_{VDD} = 16V, T_A = −40°C to 125°C, unless otherwise specified)

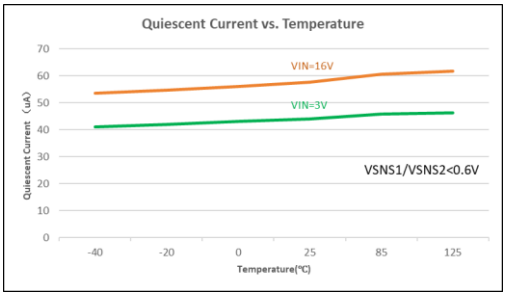
Parameter		Symbol	Test Condition	Min	Typ	Max	Units
VDD Range		V_{VDD}		3	--	16	V
VDD Supply Current			Charge-pump off	--	50	100	uA
VDD POR Threshold		V_{TH_VDD}		2.3	2.5	2.7	V
VDD POR Hysteresis		ΔV_{TH_VDD}		--	300	--	mV
VSNS1/VSNS2 Rising Threshold		V_{RTH_VSNS}		0.591	0.6	0.609	V
VSNS1/VSNS2 Falling Threshold		V_{FTH_VSNS}		0.539	0.55	0.561	V
VSNS1/VSNS2 Hysteresis		ΔV_{TH_VSNS}		--	60	--	mV
VSNS1/VSNS2 Input Current		I_{VSNS}		-100	--	100	nA
RST# Output Voltage	Logic-High	$V_{OH\_RST\#}$	V_{VDD} = 3V, $I_{RST\#}$ = -2mA	2.6	2.85	3	V
			V_{VDD} = 4V, $I_{RST\#}$ = -2mA	3.6	3.85	4	
			V_{VDD} = 5V, $I_{RST\#}$ = -2mA	3.9	4.57	5	
			V_{VDD} > 5.5V, $I_{RST\#}$ = -2mA	3.9	4.6	5.5	
	Logic-Low	$V_{OL\_RST\#}$	$I_{RST\#}$ = 2mA	0	--	0.4	
CDLY_RST# Source Current		$I_{CDLY\_RST\#}$	VSNS1 > 0.6V, VSNS2 > 0.6V	0.9	1	1.1	uA
CDLY_GATE Source Current		I_{CDLY_GATE}	VSNS1 > 0.6V, VSNS2 > 0.6V	0.9	1	1.1	uA
GATE Output Voltage		V_{GATE}	VDD ≤ 5V	-15%	2 x VDD	15%	V
			VDD > 5V	8.5	--	11.5	
CDLY_RST# Trip Rising Threshold		$V_{RTH\_RST\#}$		1.172	1.234	1.296	V
CDLY_RST# Hysteresis				--	50	--	mV
CDLY_GATE Trip Rising Threshold		V_{RTH_GATE}		1.172	1.234	1.296	V
CDLY_GATE Hysteresis				--	50	--	mV
CDLY _RST# Discharging Resistor			$I_{CDLY\_RST\#}$ = 10mA	--	7	12	Ω
CDLY _GATE Discharging Resistor			I_{CDLY_GATE} = 10mA	--	7	12	Ω
Over-Temperature Protection							
Thermal Shutdown		T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	30	--	

Typical Operating Characteristics

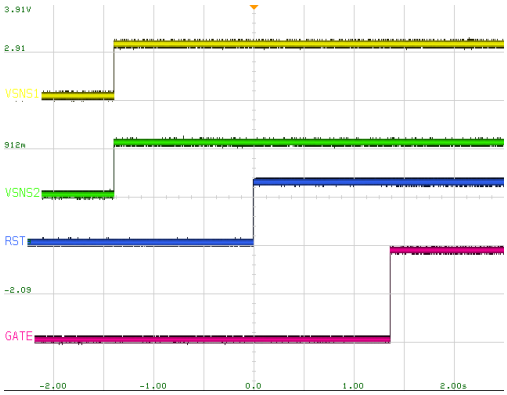
UVLO Threshold vs. Temperature



Quiescent Current vs. Temperature

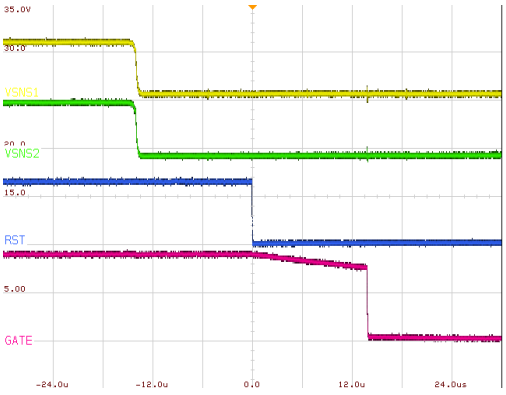


VSNS1 and VSNS2 Power on



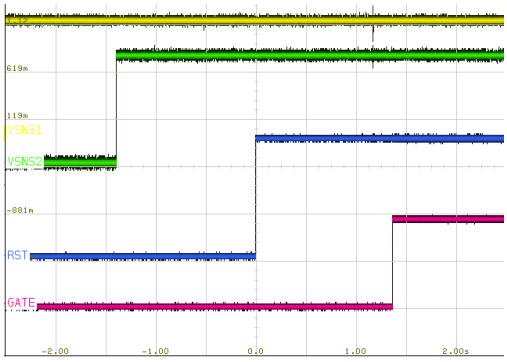
VIN=16V, VSNS1=VSNS2=1.2V, $C_{CDLY\_RST\#}$=1uF, $C_{CDLY\_GATE\#}$=1uF

VSNS1 and VSNS2 Power off



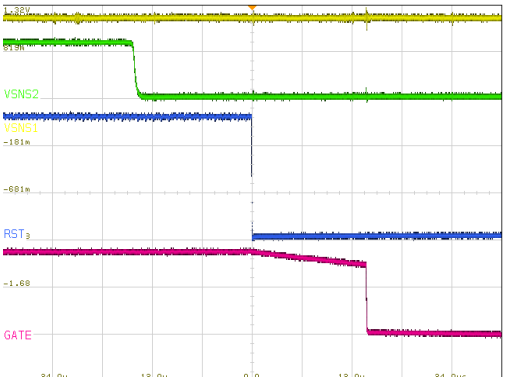
VIN=16V, VSNS1=VSNS2=1.2V, $C_{CDLY\_RST\#}$=1uF, $C_{CDLY\_GATE\#}$=1uF

VSNS2 Power on



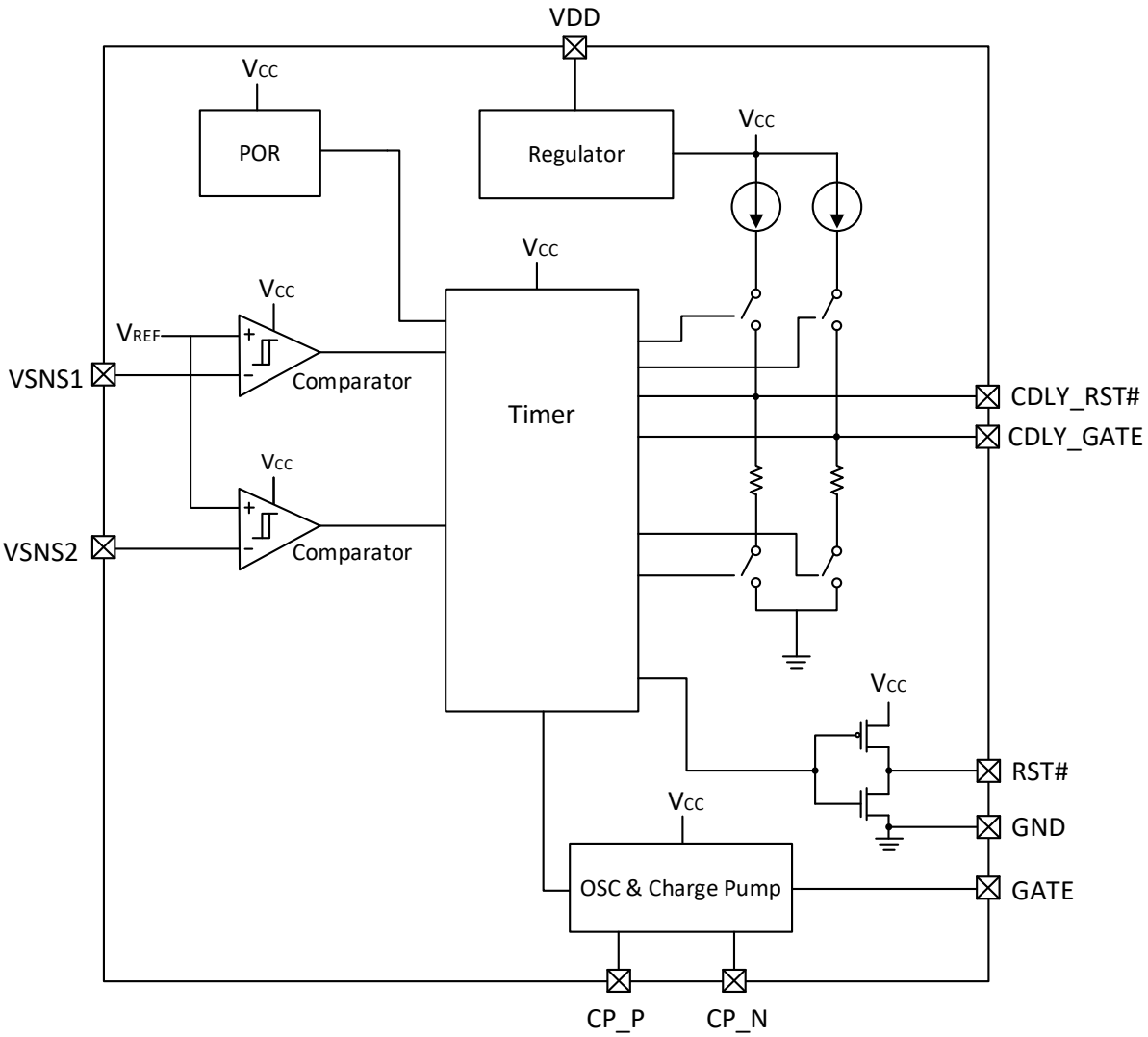
VIN=16V, VSNS1=VSNS2=1.2V, $C_{CDLY\_RST\#}$=1uF, $C_{CDLY\_GATE\#}$=1uF

VSNS2 Power off



VIN=16V, VSNS1=VSNS2=1.2V, $C_{CDLY\_RST\#}$=1uF, $C_{CDLY\_GATE\#}$=1uF

Functional Block Diagram



Block Diagram

Application Information

VSNS Transient Immunity

The XPA5108 IC is immune to short negative transients on the VSNS1 and VSNS2 pins.

Those pins sensitivity is shown in Figure 3. The T-V graphs indicate the relation between the transient and voltage below V_{RTH_VSNS}. Any combination of transient duration and overdrive voltage which reposes above the curves will bring about RST# being asserted low. That is to say, any glitch which lies below the curves will be ignored by the IC.

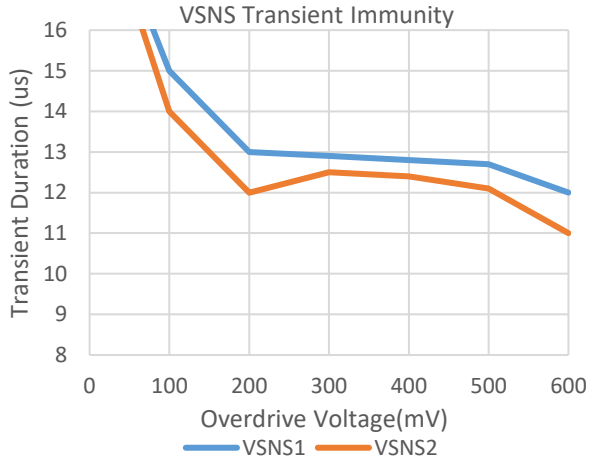


Figure 3. VSNS Transient Immunity

Adjustable Input Sensing Threshold

The XPA5108 offers two monitoring input, VSNS1 and VSNS2, with fixed reset threshold voltage V_{TH} which is 0.6V. To monitor a voltage V_S, connect a resistive divider network to the circuit as shown in Figure 4 and use the following equation to calculate the threshold voltage :

$$V_{S\_TH} = V_{TH} \times \left(1 + \frac{R1}{R2}\right)$$

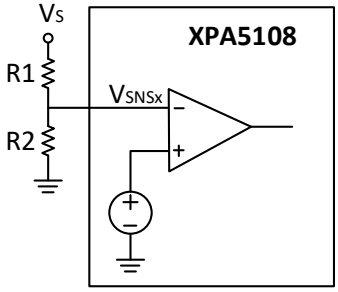


Figure 4. Setting the Adjustable Sense Input

Design engineer should check the VSNSx voltage "NOT" over 3V regarding to the highest V_S. Besides, the resistor selection is a tradeoff between accuracy and power use. The VSNSx is a high-impedance input with a small 100nA leakage current. This leakage current influences the overall error of the threshold voltage where the output is asserted. This error will reduce with lower value resistors, however, the amount of power consumed in the resistors will increase.

The following equation is provided to help estimate the value of the resistors based on the amount of acceptable error :

$$R1 = \frac{V_{S\_TH \times \varepsilon}}{I_{LEAK}}$$

V_{S_TH} is the voltage at which the output should assert, and e is the fraction of the maximum acceptable absolute resistive divider error attributable to the input leakage current (use 0.01 for ±1%), I_{LEAK} is the worst-case VSNS leakage current (see the Electrical Characteristics). Calculate R2 as follows :

$$R2 = \frac{V_{TH} \times R1}{V_{S\_TH} - V_{TH}}$$

Adjustable Delay (CDLY_RST#, CDLY_GATE)

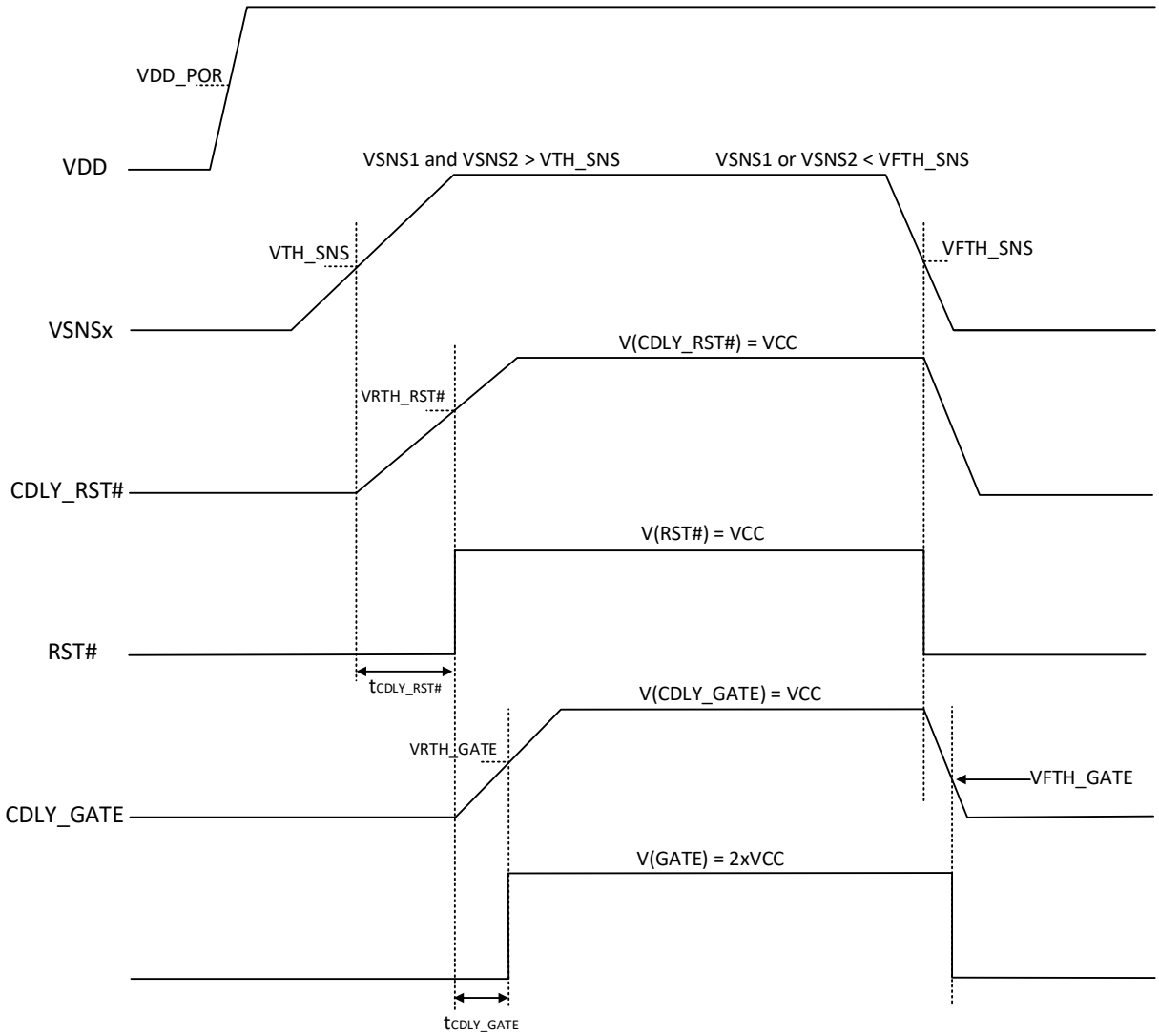
Both RST# and GATE pins output delay time can be programmed by adding external capacitors on CDLY_RST# and CDLY_GATE pins respectively. When the VSNS1/VSNS2 input sense voltage level both above the 0.6V threshold, an internal current source 1uA starts charge the external capacitor $C_{CDLY\_RST\#}$ on CDLY_RST# pin. While the capacitor voltage level is charged above the threshold 1.234V, the RST# signal level goes high then the internal current 1uA starts charge the other external C_{CDLY_GATE}. After the voltage level on C_{CDLY_GATE} above the threshold 1.234V, the GATE signal level goes high to turn on the external switch component. The delay time period can be calculated as follows :

$$t_{CDLY\_RST\#} = \frac{1.234V \times C_{CDLY\_RST\#}}{1uA}$$

$$t_{CDLY\_GATE} = \frac{1.234V \times C_{CDLY\_GATE}}{1uA}$$

Where $t_{CDLY\_RST\#}$ and t_{CDLY_GATE} are in seconds, $C_{CDLY\_RST\#}$ and C_{CDLY_GATE} are in Farads. For each VSNS1/VSNS2 input sense voltage level is lower than the 0.55V, both CDLY_RST# and CDLY_GATE pins start discharging the current from connected capacitors, after the voltage level on CDLY_RST# and CDLY_GATE lower than the threshold 1.184V (Rising threshold − Hysteresis = 1.184V), the RST# and GATE goes low to deassert the operation of connected regulators. The specific operating time sequence as shown in Figure 5 the delay time also can refer the table 1 for different capacitors setting :

$t_{CDLY\_RST\#\_Falling} = t_{CDLY\_GATE\_Falling} = 4.6 \times R \times C$ Where R is the discharge resistor and C represent $C_{CDLY\_RST\#}$ or C_{CDLY_GATE}.



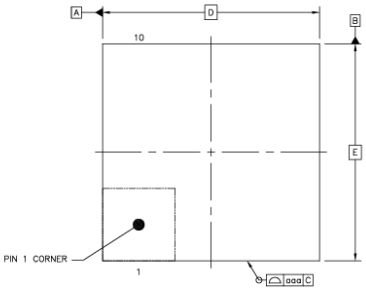
Note : VCC is internally used only. VCC tracks VDD if VDD is lower than 5V. VCC is near 5V if VDD is higher than 5V.

Figure 5. Timing Sequence Diagram

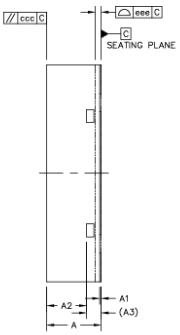
Table 1. Different Capacitors Setting

Capacitor	Rising Time (0-1.234V)	Falling Time (99%)
Open (~50pF)	60.5us	1.24ns
1nF	1.21ms	24.8ns
10nF	12.10ms	248ns
22nF	26.62ms	546ns
47nF	56.87ms	1170ns
100nF	121.00ms	2480ns
1uF	1210.00ms	24.8us

Physical Dimensions

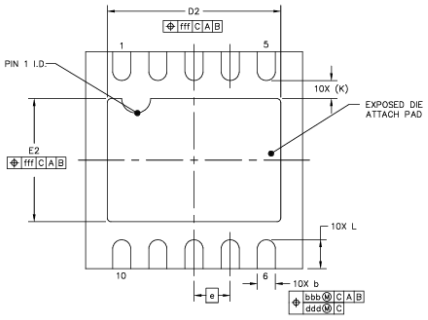


TOP VIEW



SIDE VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	2.3	2.4	2.5
	Y	E2	1.6	1.7	1.8
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.25 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	



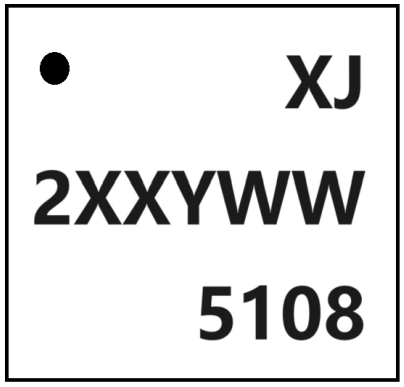
BOTTOM VIEW

Marking and Reel Information

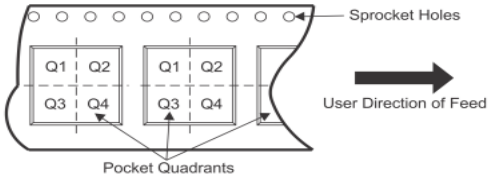
Package Marking & PQ information

XPA5108D3R Marking

Format:



Pin 1 located in Q2 direction in T&R



Remark:

Font: Arial

Logo of XINJI should be required and placed on assigned Logo position as upside illustration.

Trace-ability Code:

1. Manufacturing Location Code + Assembly lot#+Year Code+WK codeLine 1

a) 1st digit: Assembly location code: 2

b) 2nd & 3rd digit: Assembly lot number

XX means serial number for traceability, either of the 2 characters can be replaced by "0-9, A-Z, a-z"

c) 4th digit: Year code:

Year Code 2020-2051

Year	Code
2020	0
2021	1
2022	2
2023	3
2024	4
2025	5
2026	7
2027	C

Year	Code
2028	D
2029	E
2030	F
2031	H
2032	I
2033	J
2034	K
2035	L

Year	Code
2036	N
2037	P
2038	R
2039	S
2040	T
2041	U
2042	V
2043	X

Year	Code
2044	Y
2045	Z
2046	b
2047	c
2048	d
2049	h
2050	i
2051	j

d)5th & 6th digit: Week code, 01 means the 1st Work Week base on XinJi's calendar.

2. Line2: Product Name Code:

Product Name	P/N Code	Remark
XPA5108D3R	5108	

3. Packing: 3K/reel