6A Dual-Channel Ultra-Low On-Resistance Load Switch with Slew Rate Control

Features

- Integrated dual-channel NMOS load switch
- Input voltage: V_{IN}=0.6V to V_{BIAS}
- V_{BIAS} voltage: V_{BIAS}=2.5V to 5.5V
- On-resistance
  - R_{on}=18mΩ (Typical) at V_{BIAS}=5V and V_{IN}=0.6V to 5V
  - R_{on}=19mΩ (Typical) at V_{BIAS}=2.5V and V_{IN}=0.6V to 2.5V
- 6A continuous switch current
- Quiescent Current
  - 47μA (typical, both channels) at V_{BIAS}=5V and V_{IN}=5V
  - 23μA (typical, single channel) at V_{BIAS}=5V and V_{IN}=5V
- Controlled slew rate to limit inrush currents
- Over-Temperature Protection(OTP)
- Quick Output Discharge (QOD)
- DFN 3mmX2mmX0.75mm-14L Package with Thermal Pad

General Description

The AW35142A is a dual-channel NMOS load switch with slew rate control. The device integrated a typical R_{on} of 18mΩ and has 6A maximum continuous switch current. Each channel has independent enable control pin ON1/ON2 which is suitable for interfacing directly with low voltage I/O ports.

The AW35142A features over temperature protection. The device shuts down when the junction temperature exceeds 160℃and return on when the temperature drops 30℃. The AW35142A also has QOD function which can prevent the output from floating when the switch is disabled.

Applications

Notebook

Tablet PCs

Consumer Electronics

Typical Application Circuit

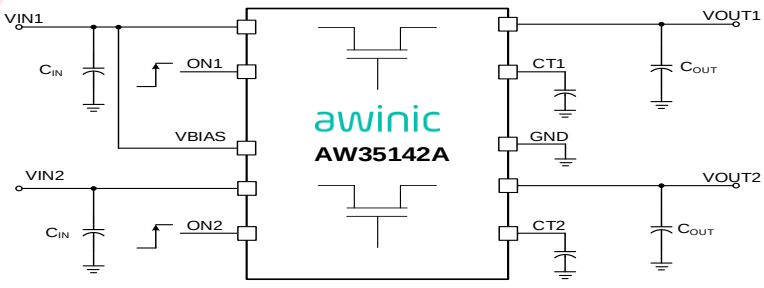


Figure 1. Typical Application Circuit of AW35142ADNR

Pin Configuration And Top Mark

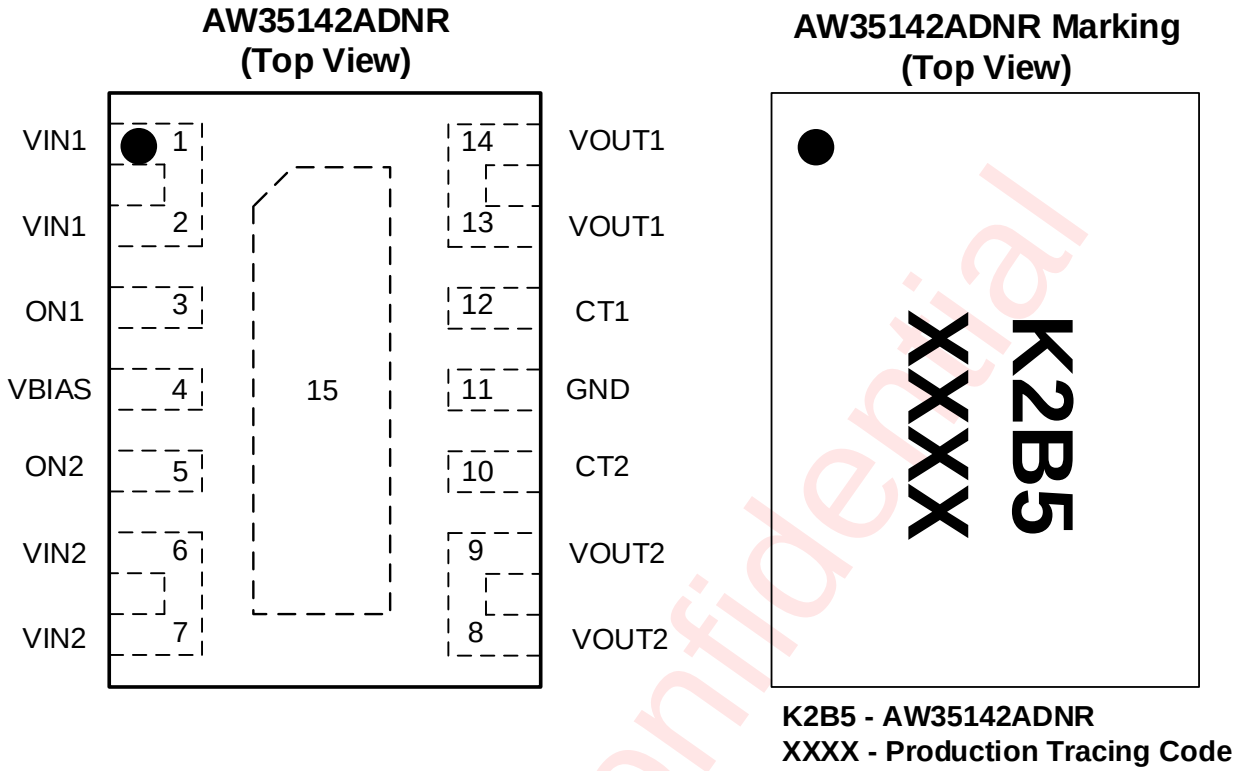


Figure 2. Pin Configuration and Top Mark

Pin Definition

Pin	Name	Description
1	VIN1	Channel 1 input
2		
3	ON1	Channel 1 enable (active high)
4	VBIAS	Power supply
5	ON2	Channel 2 enable (active high)
6	VIN2	Channel 2 input
7		
8	VOUT2	Channel 2 output
9		
10	CT2	Channel 2 slew rate control
11	GND	Ground
12	CT1	Channel 1 slew rate control
13	VOUT1	Channel 1 output
14		
15	Thermal pad	Expose pad can be tied to ground plane for better power dissipation

Functional Block Diagram

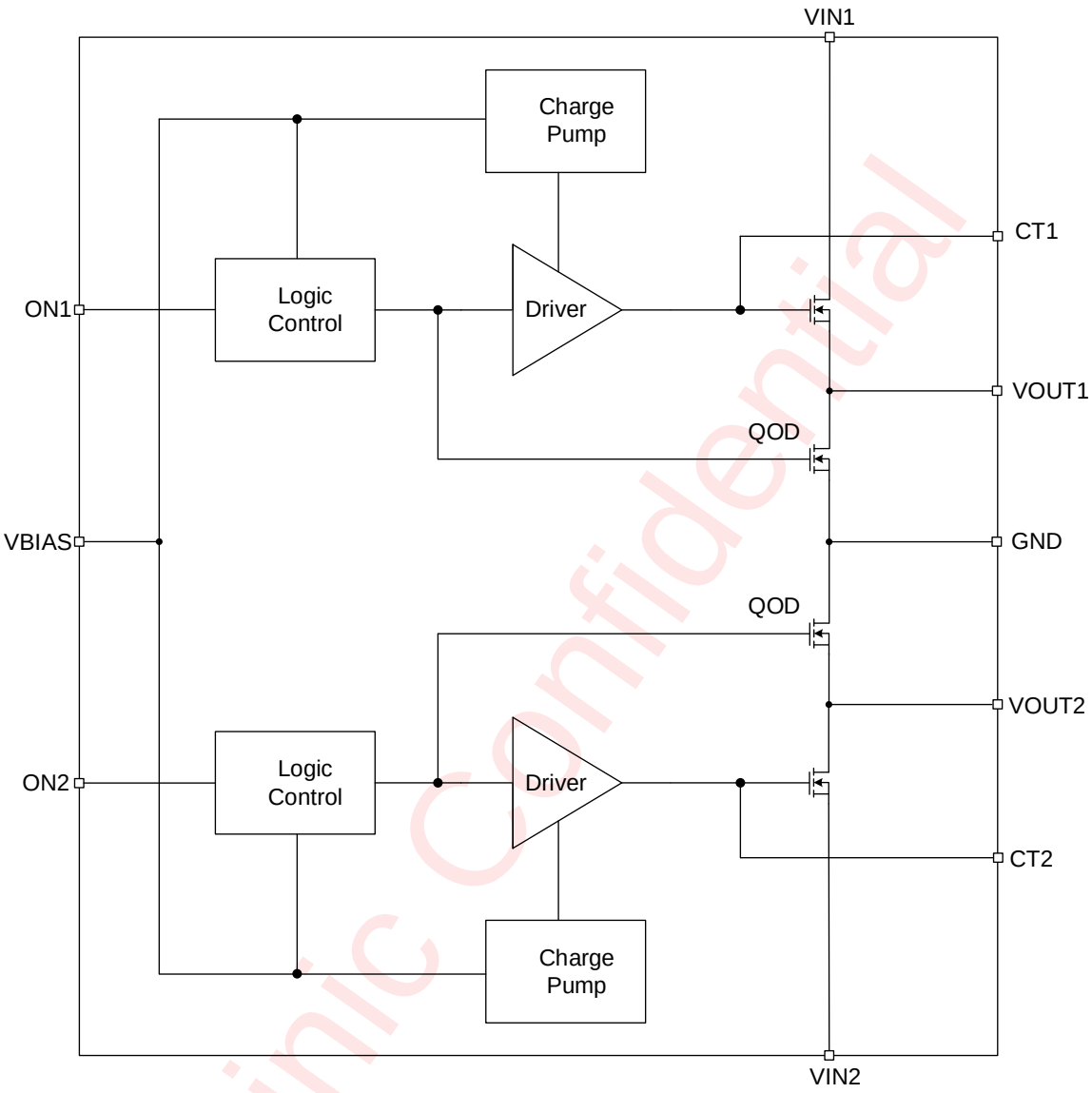


Figure 3. Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW35142ADNR	-40℃~105℃	DFN3mmX2mmX0.75mm-14L	K2B5	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS	RANGE
Input voltage range V_{IN}	-0.3V to 6V
BIAS voltage range V_{BIAS}	-0.3V to 6V
Enable control voltage range	-0.3V to 6V
Output voltage range	-0.3V to 6V
Junction-to-ambient thermal resistance θ_{JA}(NOTE2)	60°C/W
Operating free-air temperature range	-40°C to 105°C
Maximum operating junction temperature T_{JMAX}	150°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD	
HBM (Human body model)(NOTE3)	±2kV
CDM(Charged device model) (NOTE4)	±1.5kV
Latch-Up	
Latch-Up(NOTE5)	+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Thermal resistance from junction to ambient is highly dependent on PCB layout.

NOTE3: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE4: All pins. Test Condition: ESDA/JEDEC JS-002-2018.

NOTE5: Test Condition: JEDEC STANDARD NO.78F JANUARY 2022.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN1} V_{IN2}	Input voltage	0.6		V_{BIAS}	V
V_{ON1} V_{ON2}	EN voltage	0		V_{BIAS}	V
V_{OUT1} V_{OUT2}	Output voltage	0		V_{IN}	V
V_{BIAS}	Power supply	2.5		5.5	V
C_{T1} C_{T2}	Slew rate control	0	1000		pF
C_{IN}	Input capacitance	1			μF
C_{OUT}	Output capacitance		0.1		μF

Electrical Characteristics—V_{BIAS}=5V

Unless noted otherwise, V_{BIAS} voltage range of 2.5 V to 5.5 V, operating temperature range of –40°C to +85°C. Typical values are guaranteed for V_{BIAS}=V_{IN}=V_{ON}=5V, TA = 25°C.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
$I_{Q, VBIAS}$	V_{BIAS} quiescent current for both channels	$V_{IN1,2}$=5V, $V_{ON1,2}$=5V, no load		17	47	80	μA
	V_{BIAS} quiescent current for single channel	V_{IN1}=5V, V_{ON1}=5V, V_{ON2}=0V no load		8.5	23	40	μA
$I_{SD, VBIAS}$	V_{BIAS} shutdown current for both channels	$V_{ON1,2}$=0V, $V_{OUT1,2}$=0V		1	20	210	nA
$I_{SD, VIN}$	V_{IN} shutdown current for each channel	V_{ON}=0V, V_{OUT}=0V	V_{IN}=5V	2	8	830	nA
			V_{IN}=3.3V		5		nA
			V_{IN}=1.8V		2		nA
			V_{IN}=0.6V		1		nA
I_{ON}	ON pin leakage current for each channel	V_{ON}=5V		0	1	30	nA
R_{on}	On-resistance	I_{OUT}=-200mA, V_{IN}=0.6 to 5V		9.7	17.5	30	mΩ
R_{DISC}	Output discharge resistance	V_{IN}=V_{OUT}=5V, V_{ON}=0V		68	100	145	Ω
V_{IH}	ON input high threshold level			1.2			V
V_{IL}	ON input low threshold level					0.4	V
T_{SD}	Over temperature threshold	Junction Temperature Rising			160		°C
$T_{SD, HYS}$	Over temperature hysteresis	Junction Temperature Falling			30		°C

Electrical Characteristics—V_{BIAS}=2.5V(NOTE6)

Unless noted otherwise, V_{BIAS} voltage range of 2.5 V to 5.5 V, operating temperature range of –40°C to +85°C. Typical values are guaranteed for V_{BIAS}=V_{IN}=V_{ON}=2.5V, TA = 25°C.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
$I_{Q, VBIAS}$	V_{BIAS} quiescent current for both channels	$V_{IN1,2}$=2.5V, $V_{ON1,2}$=2.5V, no load			40		μA
	V_{BIAS} quiescent current for single channel	V_{IN1}=2.5V, V_{ON1}=2.5V, V_{ON2}=0V no load			20		μA
$I_{SD, VBIAS}$	V_{BIAS} shutdown current for both channels	$V_{ON1,2}$=0V, $V_{OUT1,2}$=0V			10		nA
$I_{SD, VIN}$	V_{IN} shutdown current for each channel	V_{ON}=0V, V_{OUT}=0V	V_{IN}=2.5V		4		nA
			V_{IN}=1.8V		3		nA
			V_{IN}=1.2V		2		nA
			V_{IN}=0.6V		1		nA
I_{ON}	ON pin leakage current for each channel	V_{ON}=2.5V			1		nA
R_{on}	On-resistance	I_{OUT}=-200mA, V_{IN}=0.6 to 2.5V			18.5		mΩ
R_{DISC}	Output Discharge Resistance	V_{IN}=V_{OUT}=2.5V, V_{ON}=0V			117		Ω
V_{IH}	ON input high threshold level			1.2			V
V_{IL}	ON input low threshold level					0.4	V
T_{SD}	Over temperature threshold	Junction Temperature Rising			160		°C
$T_{SD, HYS}$	Over temperature hysteresis	Junction Temperature Falling			30		°C

NOTE6: MIN/MAX value of V_{BIAS}=5V covers that of V_{BIAS}=2.5V. Please refer to V_{BIAS}=5V for MIN/MAX value.

Switching Characteristics

Unless noted otherwise, V_{BIAS} voltage range of 2.5 V to 5.5 V, operating temperature range of –40°C to +85°C.
Typical values are guaranteed for V_{BIAS}=V_{IN}=V_{ON}=5V, TA = 25°C.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}=5V, V_{BIAS}=5V						
t_D	ON Delay time	R_L=10Ω, C_L=0.1μF, CT=1nF		950		μs
t_{ON}	Turn-on time			1950		μs
t_R	Rising time			2000		μs
t_{OFF}	Turn-off time			1.7		μs
t_F	Falling time			2.5		μs
V_{IN}=0.6V, V_{BIAS}=5V						
t_D	ON Delay time	R_L=10Ω, C_L=0.1μF, CT=1nF		700		μs
t_{ON}	Turn-on time			950		μs
t_R	Rising time			470		μs
t_{OFF}	Turn-off time			3.8		μs
t_F	Falling time			2.1		μs
V_{IN}=2.5V, V_{BIAS}=2.5V						
t_D	ON Delay time	R_L=10Ω, C_L=0.1μF, CT=1nF	150	1100	1550	μs
t_{ON}	Turn-on time		550	1900	3600	μs
t_R	Rising time		600	1700	3600	μs
t_{OFF}	Turn-off time			3.5		μs
t_F	Falling time			4.5		μs
V_{IN}=0.6V, V_{BIAS}=2.5V						
t_D	ON Delay time	R_L=10Ω, C_L=0.1μF, CT=1nF		980		μs
t_{ON}	Turn-on time			1300		μs
t_R	Rising time			560		μs
t_{OFF}	Turn-off time			5.1		μs
t_F	Falling time			2.9		μs

Timing Diagram

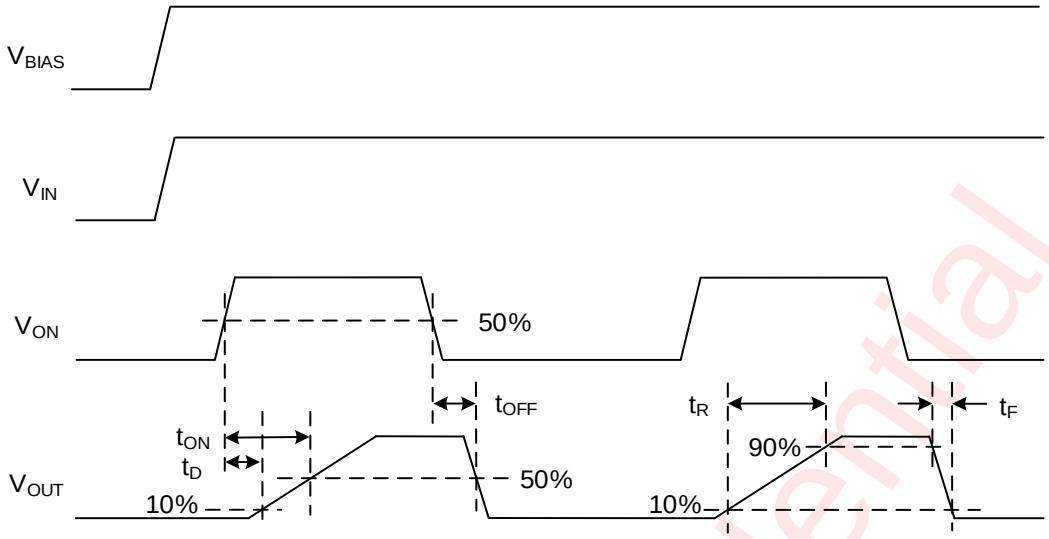


Figure 4. AW35142A Timing Diagram

Typical Characteristics

Ambient temperature is 25°C, C_{IN} =1μF, C_{OUT}=0.1μF, C_T=1Nf, unless otherwise noted.

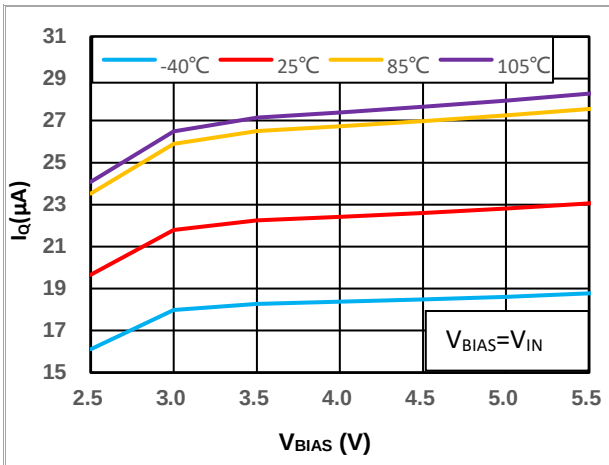


Figure 5 Quiescent Current vs. V_{BIAS}, Single Channel

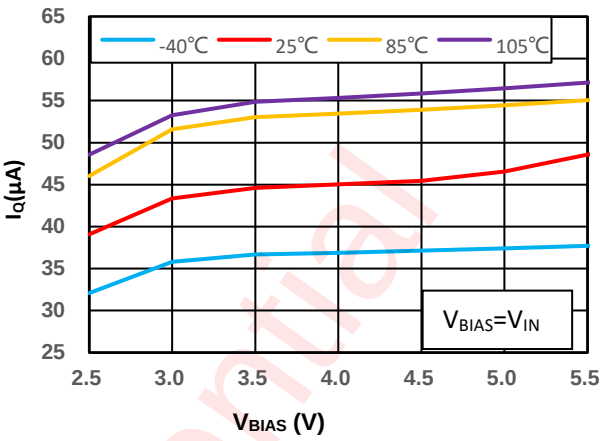


Figure 6 Quiescent Current vs. V_{BIAS}, Both Channels

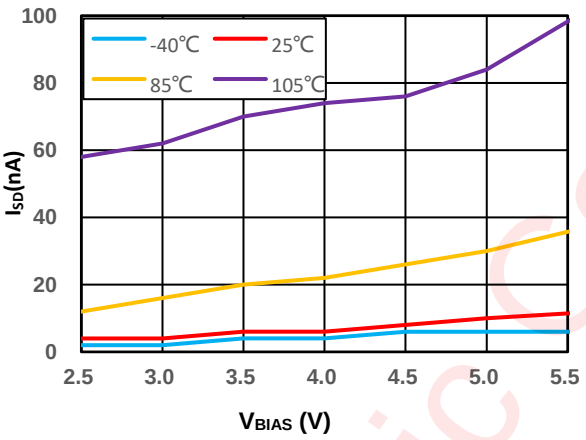


Figure 7 V_{BIAS} Shutdown Current vs. V_{BIAS}, Both Channels

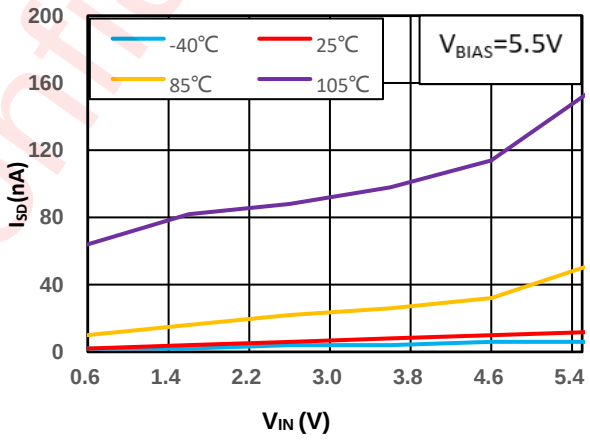


Figure8 V_{IN} Shutdown Current vs. V_{IN}, Both Channels

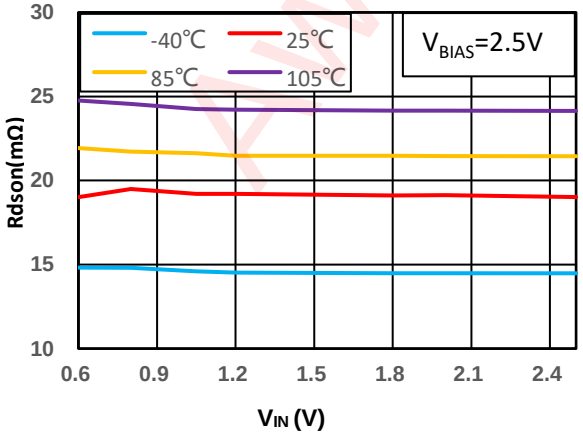


Figure 9 Rdson vs. V_{IN}

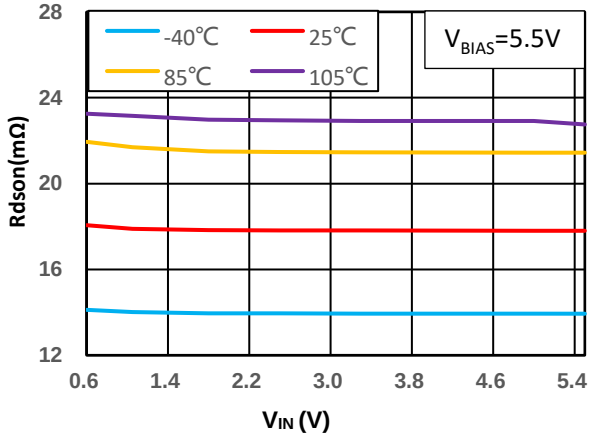


Figure 10 Rdson vs. V_{IN}

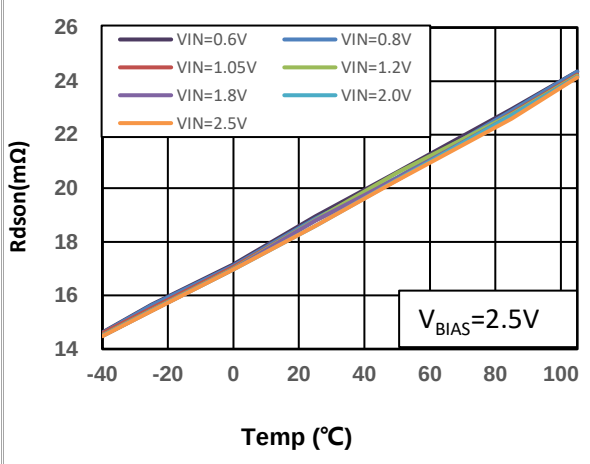


Figure 11 Rdson vs. Temp (I_{OUT}=-200Ma)

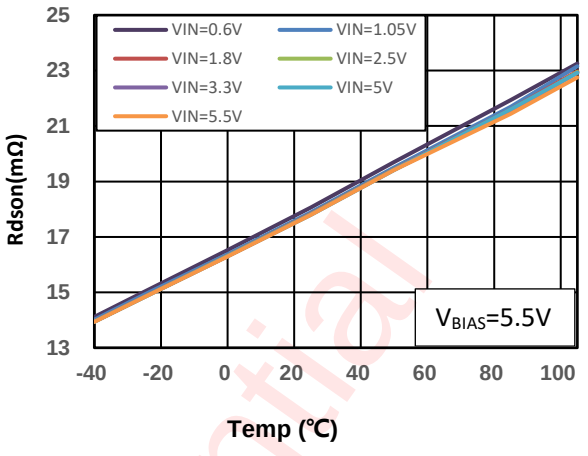


Figure 12 Rdson vs. Temp (I_{OUT}=-200Ma)

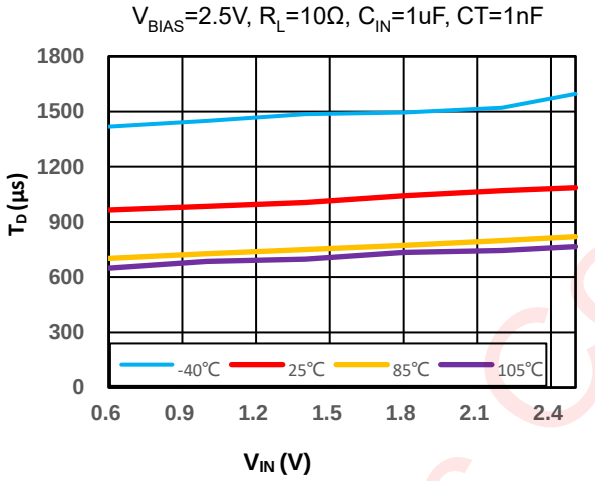


Figure 13 Turn On Delay vs. V_{IN}

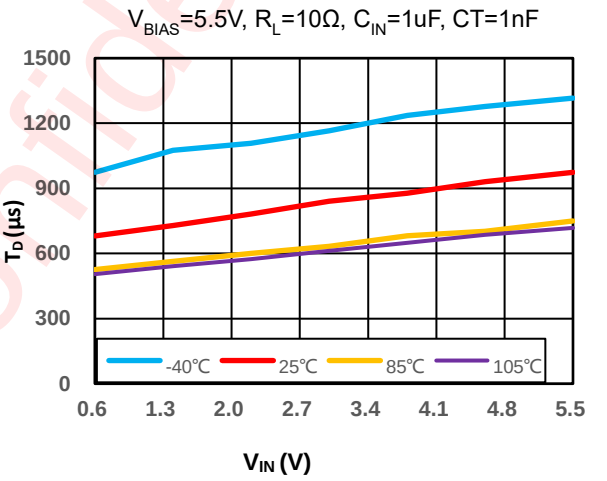


Figure 14 Turn On Delay vs. V_{IN}

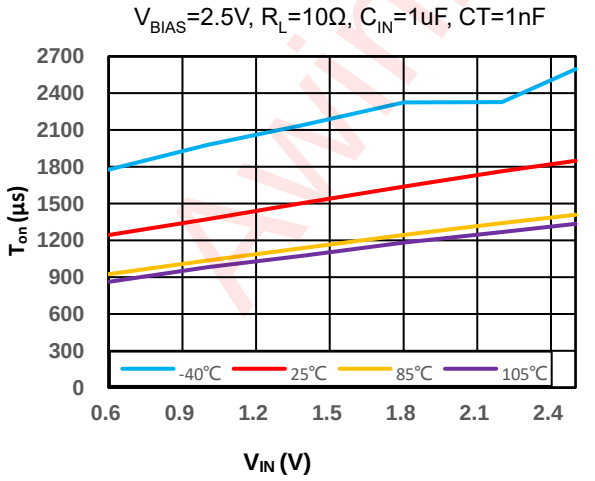


Figure 15 Turn On vs. V_{IN}

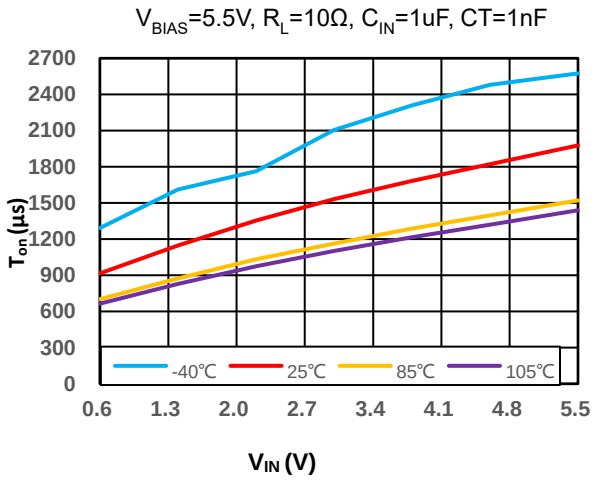


Figure 16 Turn On vs. V_{IN}

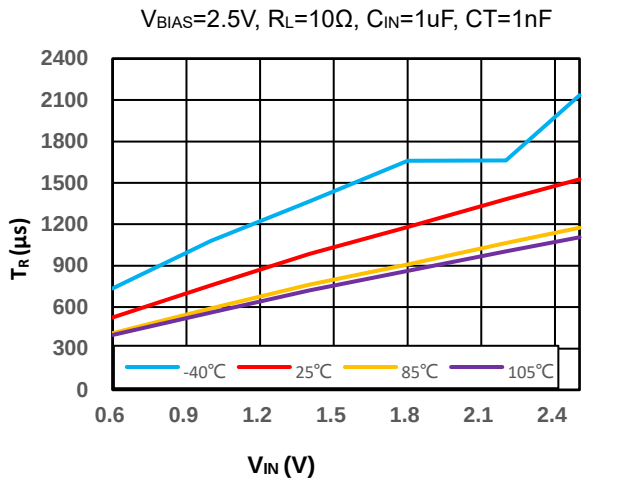


Figure 17 Rise Time vs. V_{IN}

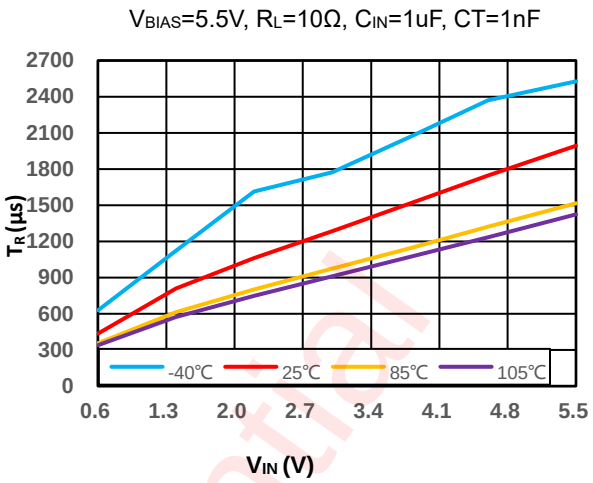


Figure 18 Rise Time vs. V_{IN}

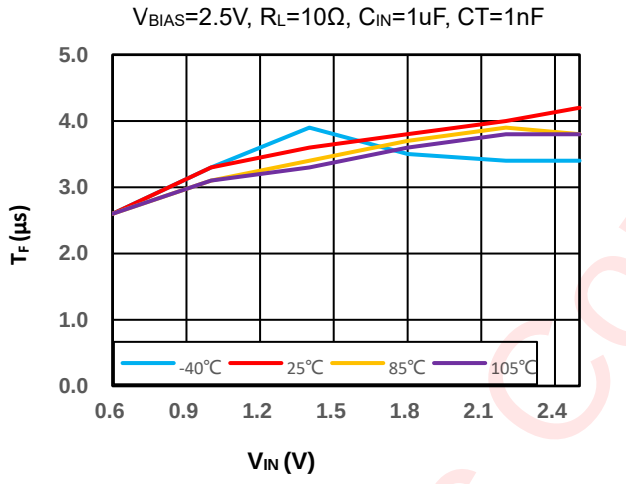


Figure 19 Fall Time vs. V_{IN}

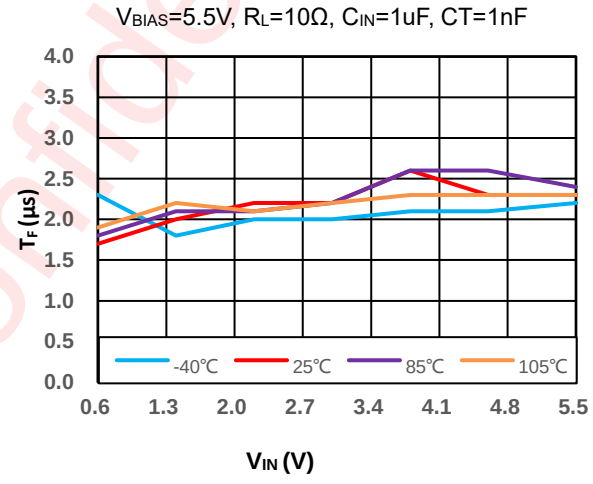


Figure 20 Fall Time vs. V_{IN}

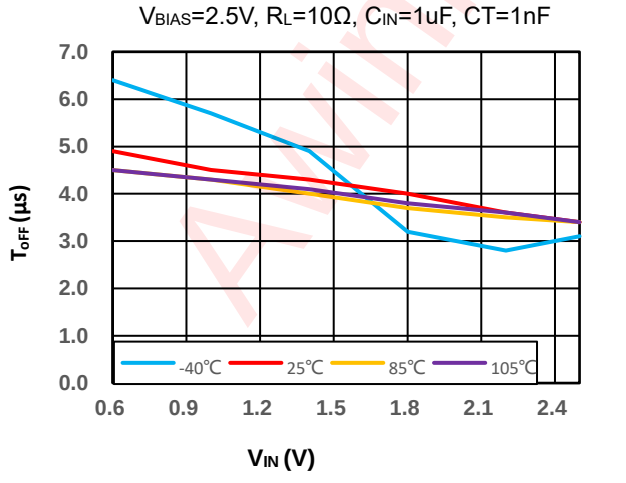


Figure 21 Turn Off vs. V_{IN}

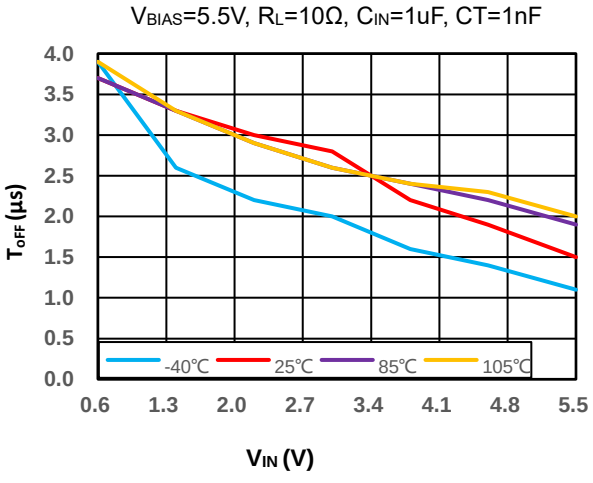


Figure 22 Turn Off vs. V_{IN}

V_{BIAS}=2.5V, V_{IN}=0.6V, C_L=0.1μF, CT=1Nf, R_L=10Ω

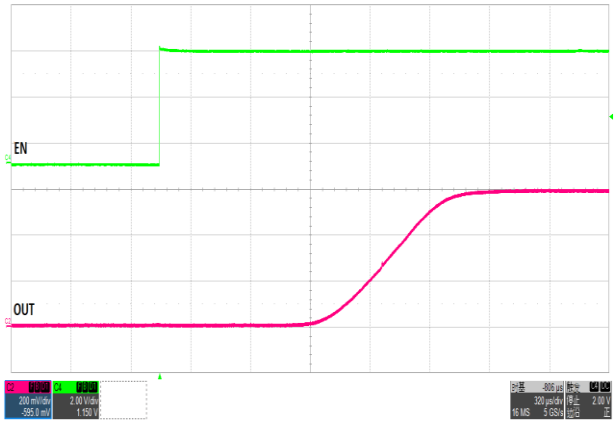


Figure 23 Turn On Response

V_{BIAS}=2.5V, V_{IN}=0.6V, C_L=0.1μF, CT=1Nf, R_L=10Ω

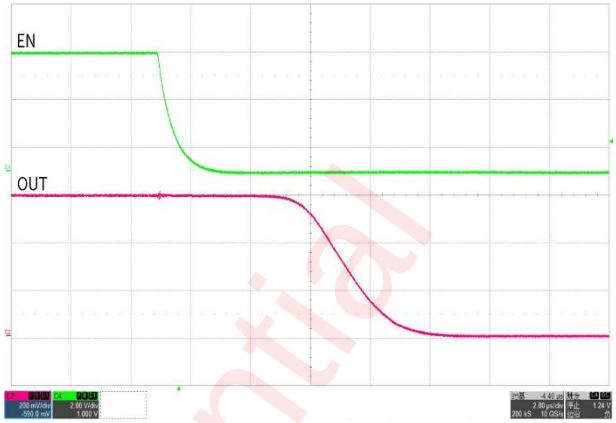


Figure 24 Turn Off Response

V_{BIAS}=V_{IN}=5V, C_L=0.1μF, CT=1Nf, R_L=10Ω

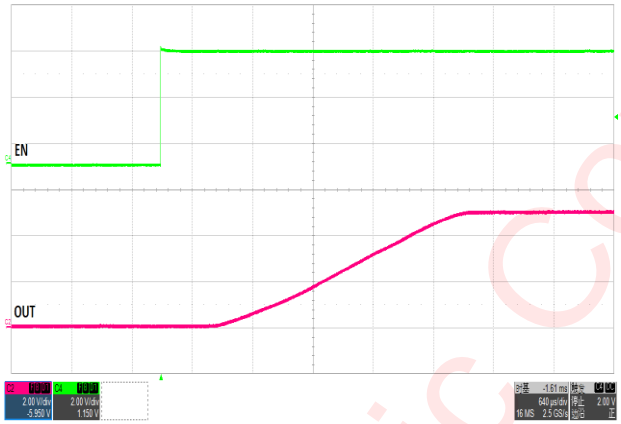


Figure 25 Turn On Response

V_{BIAS}=V_{IN}=5V, C_L=0.1μF, CT=1Nf, R_L=10Ω

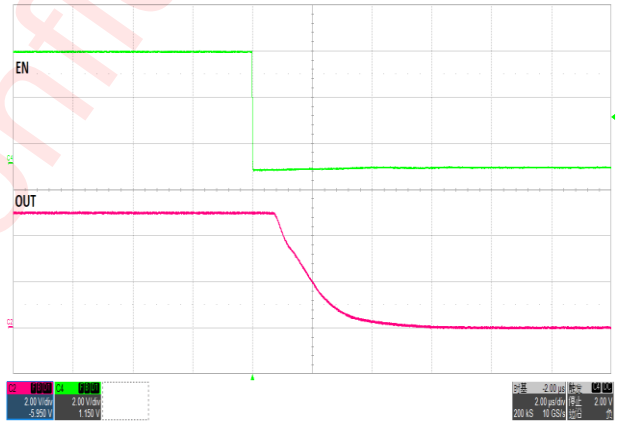


Figure 26 Turn Off Response

Detailed Functional Description

The AW35142A is a both channels, 18Mω Ron (typical) N-type MOSFET load switch which can reduce the voltage drop in high current rails, the device can support 6A continuous current and controlled by the ON pin. In order to control the inrush current, the device has a configurable slew rate time for different applications by the CT pin.

Turn On/Off Control

The switch on/off controlled by ON pin which compatible standard GPIO logic. The device is enable or disable when the ON pin voltage higher than VIH or lower than VIL. Floating the ON pin is forbidden, it must be tied high or low.

Table 1. Functional Table

EN	IN to OUT	OUT to GND
Low	OFF	ON
High	ON	OFF

Slew Rate Control

The AW35142A provides an adjustable soft start time which can limit the inrush current when the switch is on. The slew rate time is controlled by the CT capacitor. This feature reduces the interference to the power supply.

Quick Output Discharge (QOD)

The AW35142A includes the Quick Output Discharge (QOD) feature, in order to discharge the application capacitor connected on OUT pin. When ON pin is set to low level (disable state), a discharge resistance with a typical value of 100Ω is connected between the output and ground, pull down the output and prevent it from floating when the device is disabled.

Over Temperature Protection (OTP)

When the junction temperature exceeds 160°C, the internal OTP circuit turn off the load switch. There is a temperature hysteresis 30°C, in other words, the OTP circuit can turn on the switch only if the junction temperature is below 130°C.

Adjustable Rise Time

The output rise time can be set by the capacitor between CT pin and GND. The slew rate can be calculated by the below formula approximately.

Equation (1) accounts for 10% to 90% measurement on V_{OUT} and does not apply for CT < 100Pf, Use Table 2 to determine rise times for when CT=0Pf.

$$SR=0.63 \times CT + 128 \quad (1)$$

Where

- SR is the slew rate (in μs/V)
- CT is the capacitance value on the CT pin (in Pf)
- The units for the constant 128 is in μs/V.

Rise times shown below are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady condition.

Table 2. Rise time vs. CT

Rise time(μs)，V_{OUT}(10%~90%)，C_{IN}=1Mf，C_{OUT}=0.1Mf，V_{BIAS}=5V，R_L=10Ω							
CT/Pf	Vin=5V	Vin=3.3V	Vin=1.8V	Vin=1.5V	Vin=1.2V	Vin=1.05V	Vin=0.6V
0	266	228	189	176	161	149	103
220	795	613	443	400	353	317	203
470	1345	1024	712	636	555	501	313
1000	2415	1813	1240	1096	949	849	521
2200	5148	3852	2581	2279	1966	1765	1064
4700	10747	8112	5432	4779	4128	3670	2202
10000	20865	15799	10570	9347	8013	7199	4332

V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} and I_Q performance, make sure $V_{IN} \leq V_{BIAS}$. If $V_{IN} > V_{BIAS}$, the device is still functional. In this condition, R_{ON} will not change greatly, as shown in Figure 27, but it exhibits I_{Q_VIN} greater than what is listed in the Electrical Characteristics table. See Figure 28 for an example of a typical device, and notice the increasing I_{Q_VIN} as V_{IN} exceeds V_{BIAS} voltage. Make sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS}.

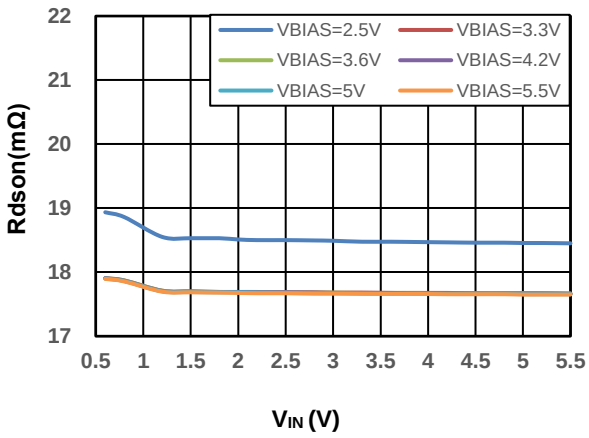


Figure 27 Rdson vs. V_{IN}(I_{OUT}=-200Ma)

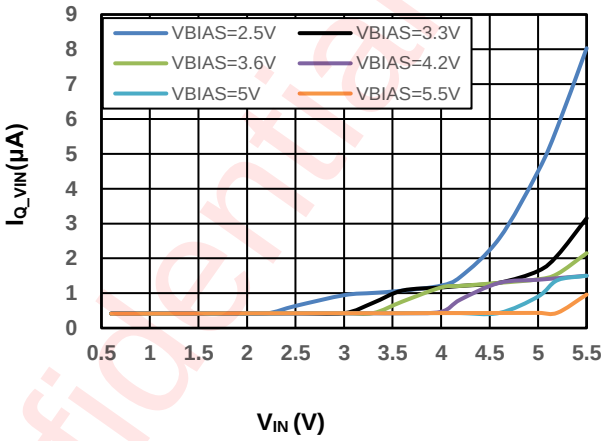


Figure28 I_{Q_VIN} vs. V_{IN}, No load

Application Information

Parallel Configuration

To increase current capabilities and to lower R_{ON}, both channels can be placed in parallel as seen in Figure 29. With this configuration, the CT1 and CT2 pins can be tied together to use one capacitor, C_{CT}.

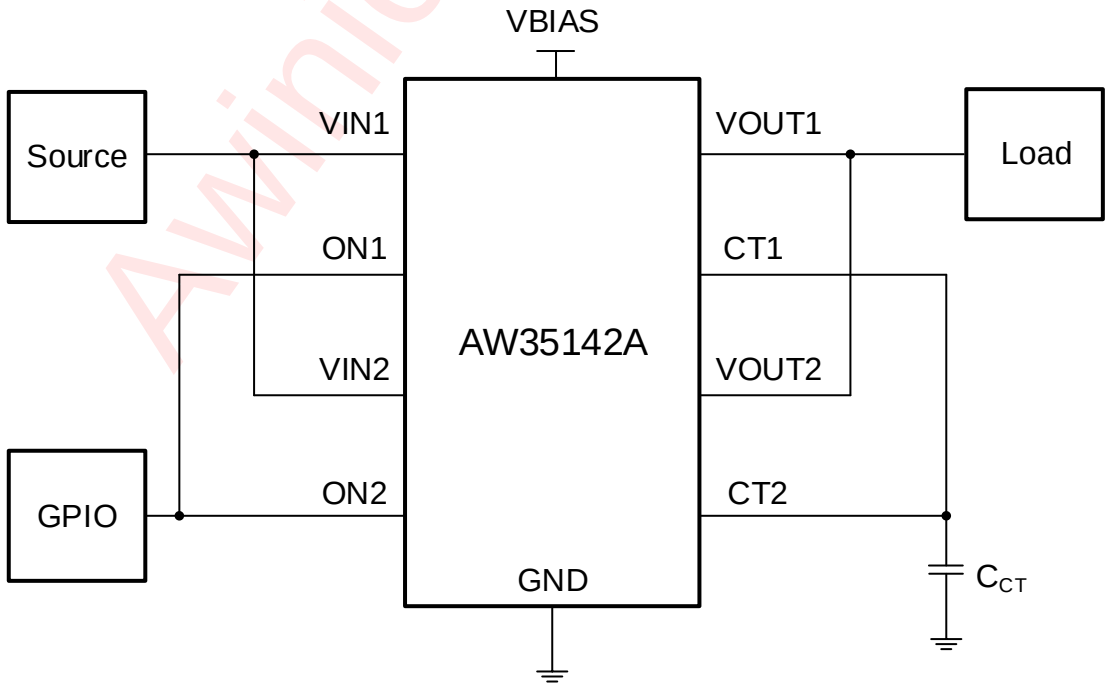


Figure 29 Parallel Configuration

PCB Layout Consideration

AW35142A is a low ON-Resistance load switch, to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

1. All the peripherals should be placed as close to the device as possible. Place the capacitor C_{IN}, C_{BIAS} and C_T on the top layer (same layer as the AW35142A) and close to IN, OUT and CT pin, and place the output capacitor C_{OUT} on the top layer (same layer as the AW35142A) and close to OUT pin.

2. The AW35142A integrates an up to 6A NMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R_{\Theta ja}$ of the package can be decreased, allowing higher power dissipation. Power lines will flow large current, please route them on PCB as straight, wide and short as possible, as in figure 27.

3. Use rounded corners on the power trace from the power supply connector to AW35142A to decrease EMI coupling.

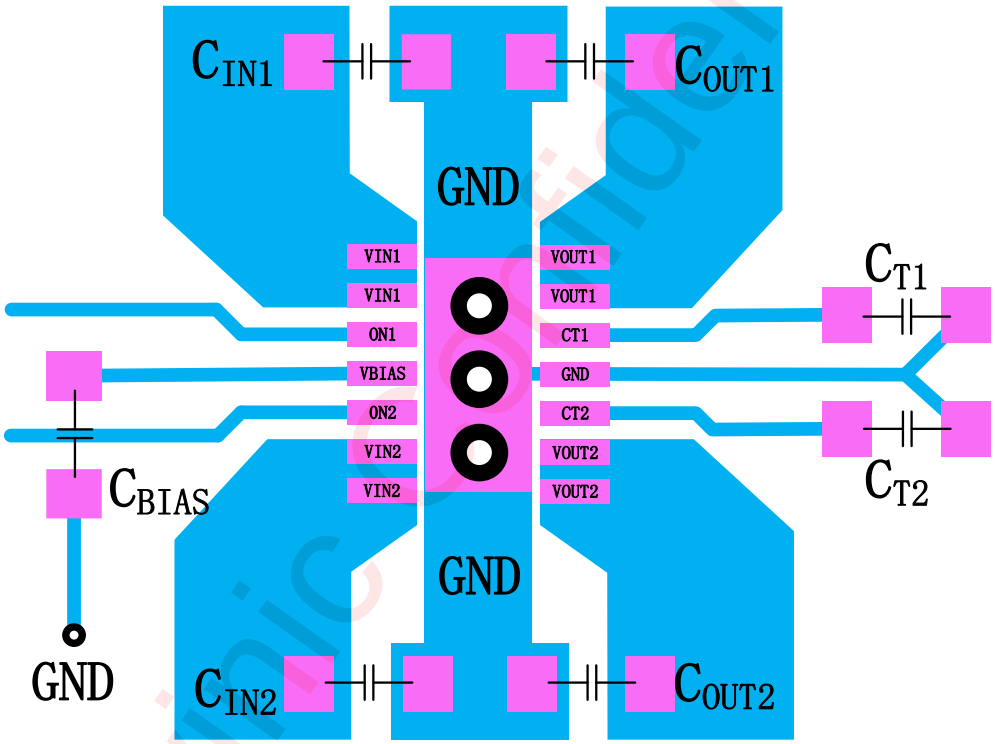
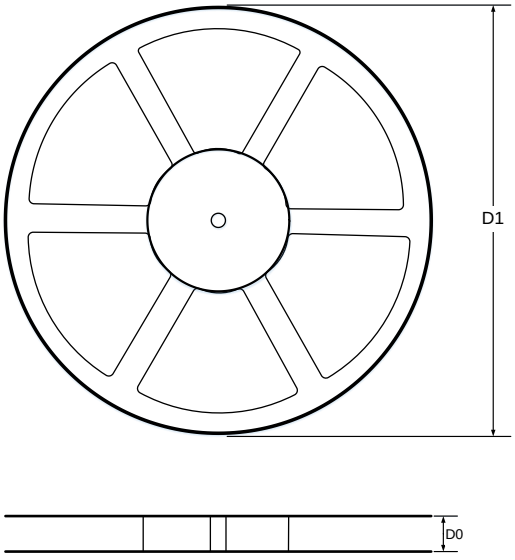


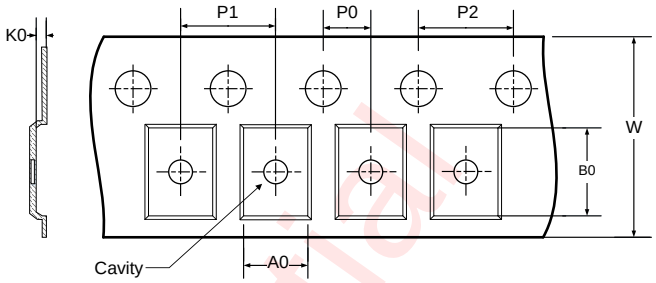
Figure 30 PCB layout example

Tape And Reel Information

REEL DIMENSIONS

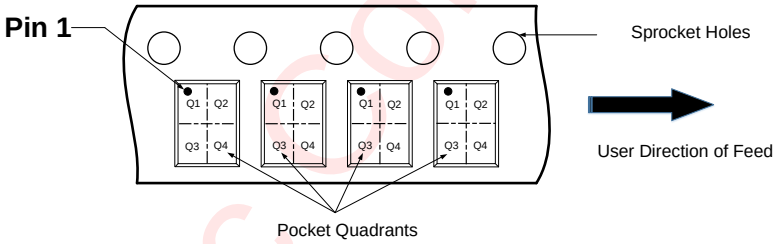


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



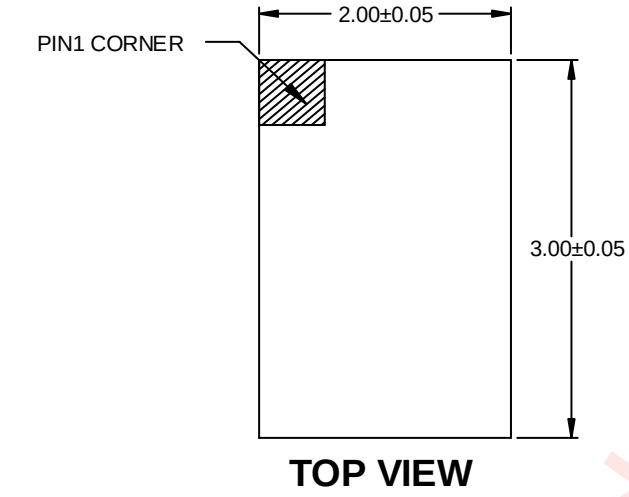
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

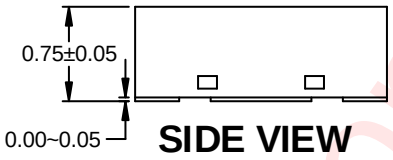
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2.3	3.2	1	2	4	4	8	Q1

All dimensions are nominal

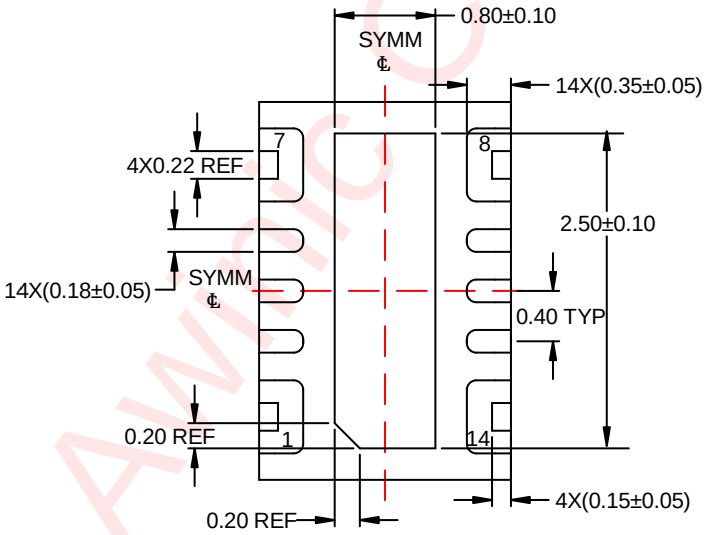
Package Description



TOP VIEW



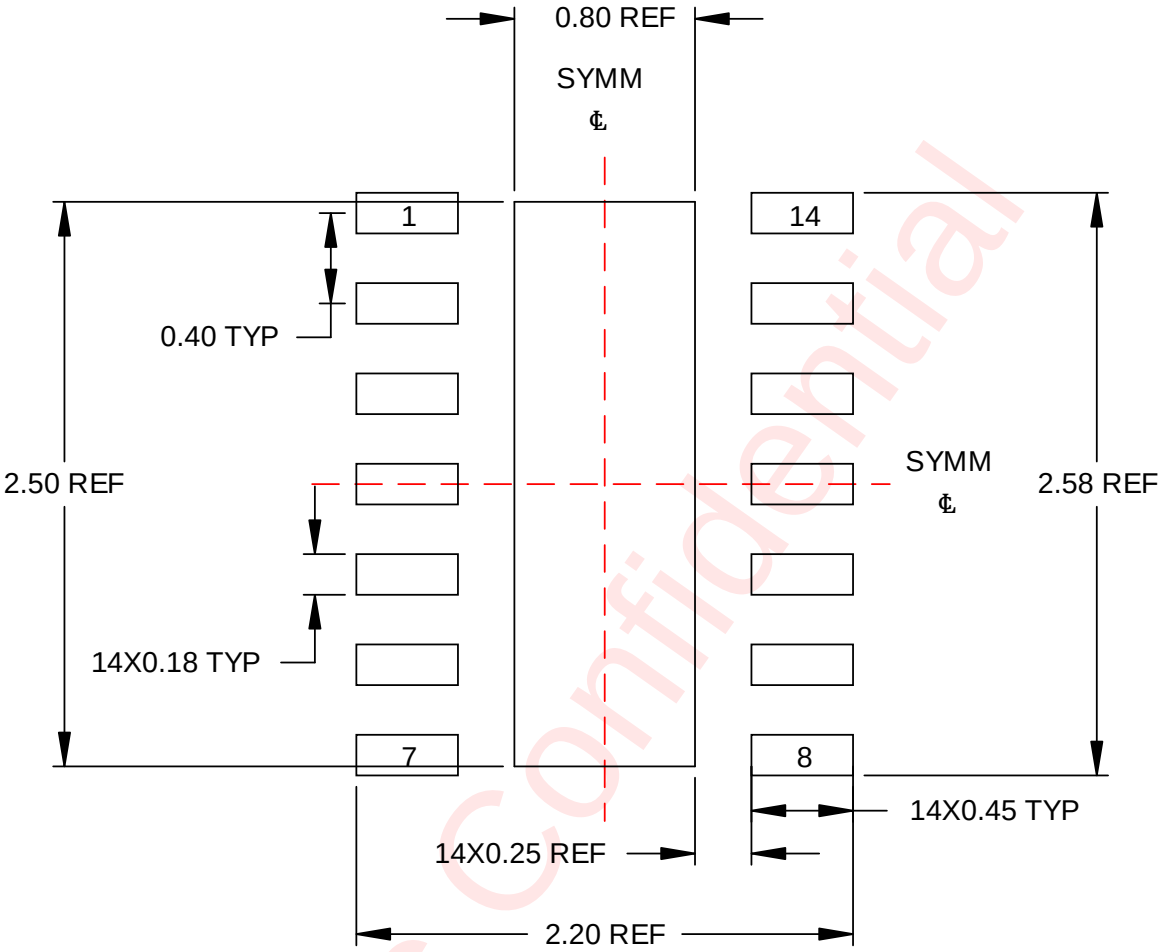
SIDE VIEW

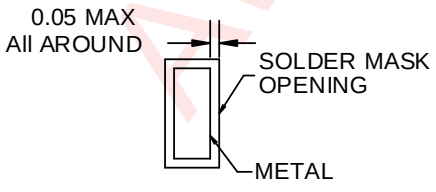


BOTTOM VIEW

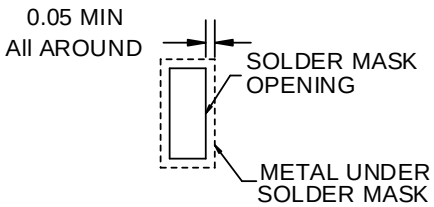
Unit：mm

Land Pattern Data





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Sep 2022	Datasheet V1.0 Released
V1.1	Jan 2023	Add V_{IN} and V_{BIAS} Voltage Range; Add figure 27、figure 28、figure 29; Add Application Information;
V1.2	Apr. 2023	Add Adjustable Rise Time section.(P13~P14)
V1.3	Feb. 2024	Correct Figure 24
V1.4	Jan. 2025	Correct t_D, t_{ON}, t_R, t_{OFF}, t_F while V_{IN}=0.6V, V_{BIAS}=5V(P7)

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