GENERAL DESCRIPTION

The LW52XX Series is a group of voltage regulators with high accuracy, high speed, low drop-out, high ripple rejection and fast discharge function.

The current limiter's fold-back circuit operates as a short circuit protection as well as the output current limiter for the output pin.

Output voltage is selectable from 1.2V to 5.0V which fixed by laser trimming technologies, Step=100mV.

The LW52XX Series is available in SOT23, SOT23-3L, SOT23-5L and DFN1x1-4L packages

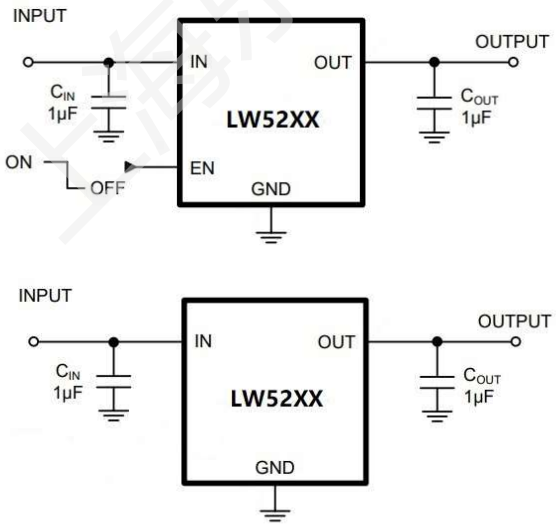
FEATURES

- Low Quiescent Current: 40μA(Typ.)
- Operating Voltage Range: from 1.5V to 6.0V
- Output Voltage Range: from 1.2V to 5.0V
- Maximum Output Current: 500mA
- Output Accuracy: ±1.5% @+25℃
- Low Dropout Voltage: 250mV@500mA/3.3V
- High PSRR: 95dB@1KHz, 10mA
- Fast-Start Function：25μs@3.3V
- Excellent Line and Load Transient Response
- Current Limiting Protection
- Output Short-Circuit Protection
- Over-Temperature Protection
- Fast Discharge Function
- Stable with 1μF Output Capacitor

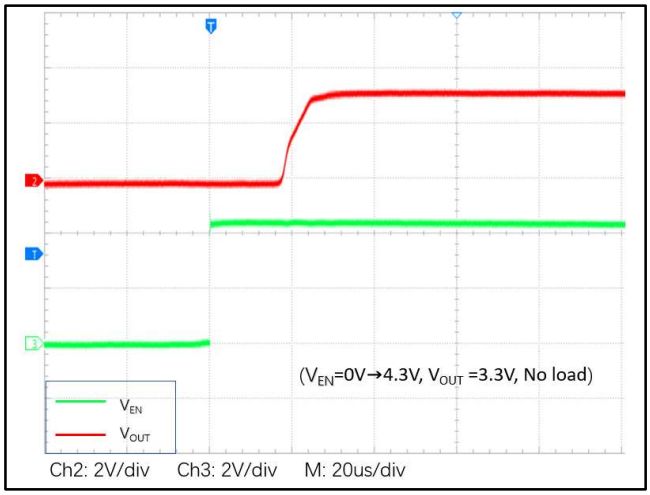
APPLICATIONS

- Battery-Powered Devices
- Reference Voltage Sources
- Other Low Voltage Power Suppliers

TYPICAL APPLICATION CIRCUIT



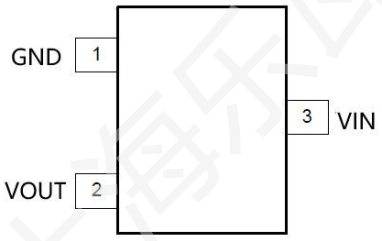
TYPICAL PERFORMANCE CHARACTERISTICS



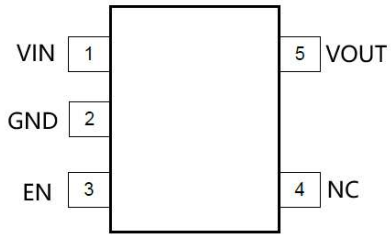
PIN DESCRIPTION:

PIN No			SYMBOL	DESCRIPTTION
SOT23/ SOT23-3L	SOT23-5L	DFN1x1-4L		
3	1	4	VIN	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the Recommended Operating Conditions table and the Input and Output Capacitor Requirements section. Place the input capacitor as close to the output of the device as possible.
1	2	2	GND	Ground pin.
--	3	3	EN	Enable pin. Drive EN greater than $V_{EN(HI)}$ to turn on the regulator. Drive EN less than $V_{EN(LO)}$ to put the low-dropout regulator (LDO) into shutdown mode.
--	4	--	NC	No internal connection. Ground this pin for better thermal performance.
2	5	1	VOUT	Regulated output voltage pin. Connect a low-equivalent series resistance (ESR) capacitor to this pin. For best transient response, use the nominal recommended value or larger capacitor from OUT to GND. An internal pulldown resistor prevents a charge from remaining on OUT when the regulator is in shutdown mode ($V_{EN} < V_{EN\ (LOW)}$).
--	--	Thermal Pad	Pad	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

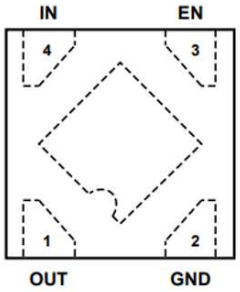
PIN ASSIGNMENT



SOT23/SOT23-3L



SOT23-5L



DFN1x1-4L

MARK INFORMATION:

SOT23

XX: VOLTAGE

YY: DATE CODE

SOT23-3/5L

XX: VOLTAGE

YY: DATE CODE

DFN1x1-4L

X: VOLTAGE

1.2V	1.5V	1.8V	2.2V	2.5V	2.8V	2.9V	3.0V	3.3V	3.6V	4.2V	5.0V
C	D	G	U	H	J	V	L	M	P	S	T

ABSOLUTE MAXIMUM RATINGS (1):

(T_A =25℃, unless otherwise specified.)

SYMBOL	ITEM		RATING	UNIT
V_{IN}	Supply Voltage		-0.3~7.0	V
V_{EN}	EN Pin Voltage		-0.3~7.0	V
V_{OUT}	V_{OUT} Pin Voltage		-0.3~ (V_{IN}+0.3)	V
$V_{(ESD)}$	ESD Susceptibility, HBM(2)		±4000	V
$R_{\theta JA}$	Junction-to-ambient Thermal Resistance(3)	SOT23	319	℃/W
		SOT23-3L	290	
		SOT23-5L	285	
		DFN1x1-4L	280	
T_J	Junction Temperature Range		-40~150	℃
T_{STG}	Storage Temperature Range		-40~150	℃
T_{SOLDER}	Lead Temperature (Soldering)		260℃, 10s	

Note:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

2. per ANSI/ESDA/JEDEC JS-001

3. Device mounted on FR-4 PCB, Refer to JESD51-3 for detailed information on the board construction

RECOMMENDED OPERATING RANGE:

SYMBOL	ITEM	VALUE	UNIT
V_{IN}	V_{IN} Supply Voltage	1.5~6.0	V
V_{EN}	EN Pin Voltage	0~6.0	V
V_{OUT}	V_{OUT} Pin Voltage	1.2~5.0	V
I_{OUT}	Output Current	0~500	mA
T_J	Junction Temperature Range	-40~125	℃

ELECTRICAL CHARACTERISTICS:

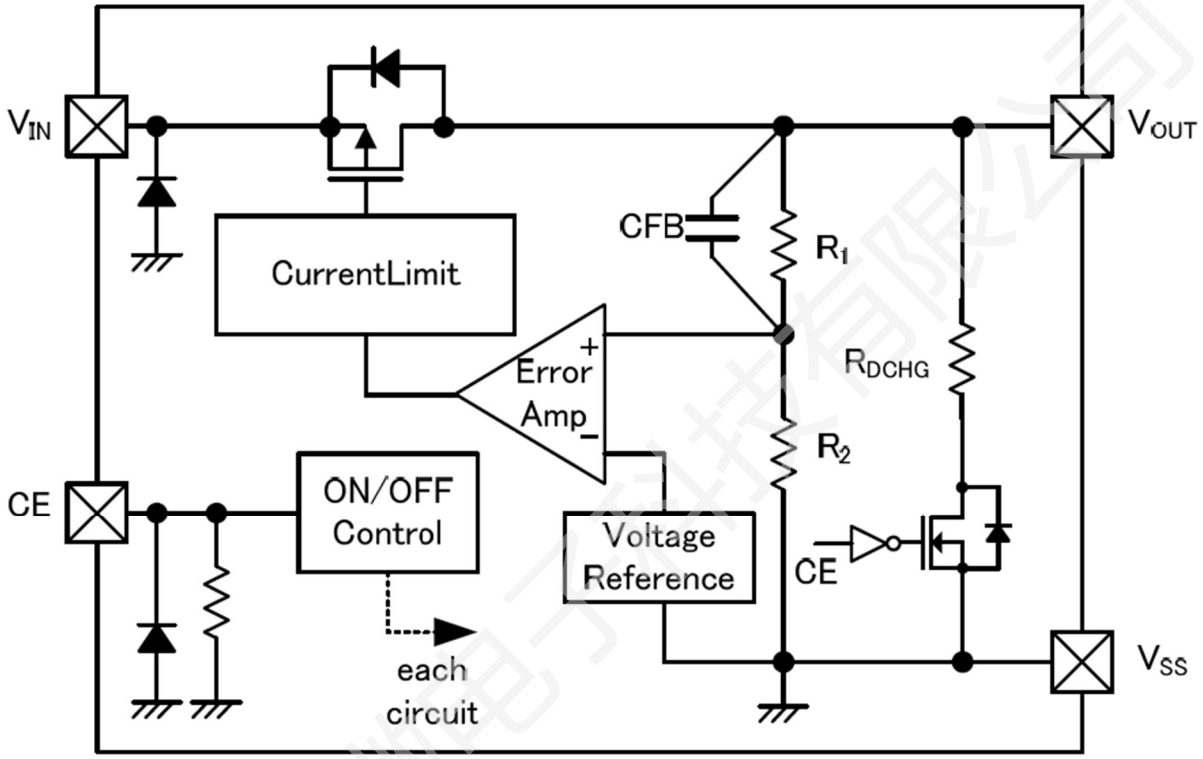
(V_{IN}=$V_{OUT(NOM)}$+1V or 2V, whichever is greater, C_{IN}= C_{OUT}=1μF, unless otherwise specified, typical values are at T_A = 25℃.)

Symbol	Parameter	Test Conditions		MIN	TYP	MAX	Units
V_{IN}	Input Voltage			1.5		6.0	V
V_{OUT}	Output Accuracy	I_{OUT}= 1mA		-1.5		+1.5	%
I_{LIM}	Current Limit(1)			515	700		mA
I_Q	Quiescent Current	V_{IN}= V_{EN}=V_{OUT}+1V, No Load			40	60	μA
I_{SHD}	Shutdown Current	V_{IN}=6.0, V_{EN}=0V				0.1	μA
V_{DROP}	Dropout Voltage (1) (2)	I_{OUT}=100mA, V_{OUT}=1.2V			310		mV
		I_{OUT}=500mA, V_{OUT}=1.2V			840		
		I_{OUT}=100mA, V_{OUT}=2.8V			55		
		I_{OUT}=500mA, V_{OUT}=2.8V			280		
		I_{OUT}=100mA, V_{OUT}=3.3V			50		
		I_{OUT}=500mA, V_{OUT}=3.3V			250		
ΔV_{OUT}/ (ΔV_{IN}*$V_{OUT(NOM)}$)	Line Regulation	V_{IN}= V_{OUT} +1V to 6V, I_{OUT}=1mA			0.1	0.25	%/V
ΔV_{OUT}	Load Regulation	1mA≤I_{OUT}≤500mA			20	50	mV
I_{SHORT}	Short Current(1)	V_{OUT}=0V			80		mA
V_{ENH}	EN High Voltage	V_{IN}=1.5V to 6.0V, I_{OUT}=1mA		1.5			V
V_{ENL}	EN Low Voltage					0.5	V
T_{STR}	Startup Time	From V_{EN} 'L'→'H' to 95%*V_{OUT}, C_{OUT}=1uF, No Load			25		μs
PSRR	Power Supply Rejection Ratio	V_{IN}= 4.3V, V_{OUT}=3.3V C_{IN} =None, V_{PP}=0.5V I_{OUT}=10mA	f=217Hz		85		dB
			f=1KHz		95		
			f=10KHz		75		
			f=100KHz		55		
T_{SD}	Thermal Shutdown	Temperature rising			160		℃
△T_{SD}	TSD Hysteresis	Temperature falling			20		℃
R_{DSCHG}	Output Discharge Resistance	V_{IN}=6V, V_{EN}=0V			150		Ω

NOTES:

1. Guaranteed by design
2. The dropout voltage is defined as V_{IN} - V_{OUT}, when V_{OUT} =95%*$V_{OUT(NOM)}$

SIMPLIFIED BLOCK DIAGRAM:



DETAIL OPERATION DESCRIPTION:

The LW52XX Series is a low power consumption low drop-out voltage regulator. It consists of a current limiter circuit, a driver transistor, a precision voltage reference and an error correction circuit, and is compatible with low ESR ceramic capacitors. The current limiter's fold-back circuit operates as a short circuit protection as well as the output current limiter.

Current Limiting and Short-Circuit Protection

The current limit circuitry prevents damage to the MOSFET switch and the hub downstream port but can deliver load current up to the current limit threshold through the switch. When a heavy load or short circuit is applied to an enabled switch, a large transient current may flow until the current limit circuitry responds. Once this current limit threshold is exceeded the device enters constant current mode until the thermal shutdown occurs or the fault is removed.

TYPICAL OPERATING CHARACTERISTICS:

（*Tested under* T_A *=25*°C, C_{IN}=C_{OUT}=1μF, unless otherwise specified）

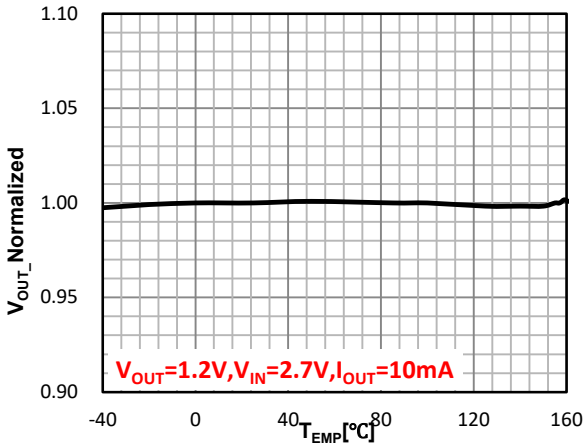


Figure 1. V_{OUT} vs Temperature

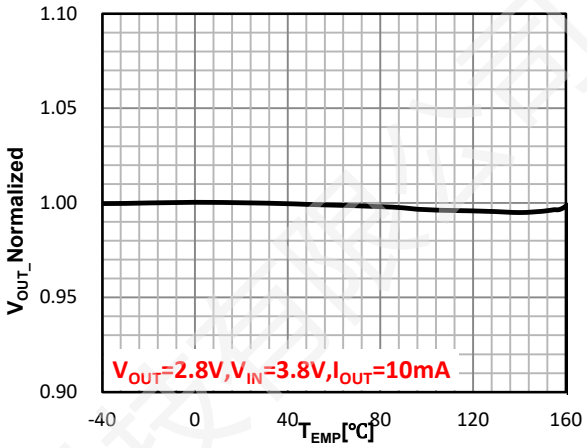


Figure 2. V_{OUT} vs Temperature

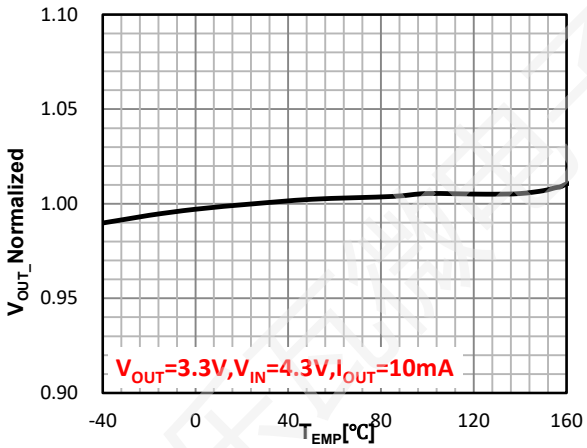


Figure 3. V_{OUT} vs Temperature

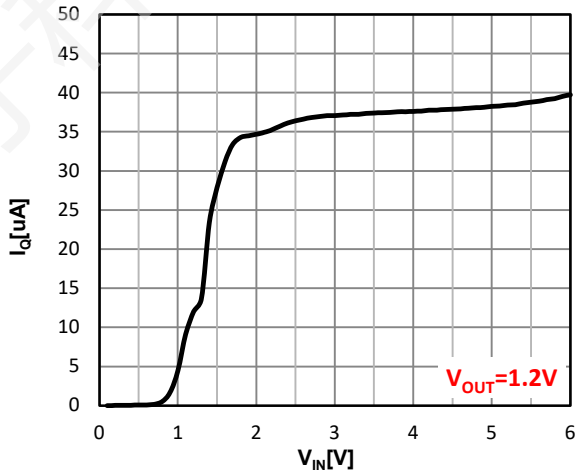


Figure 4. I_Q vs V_{IN}

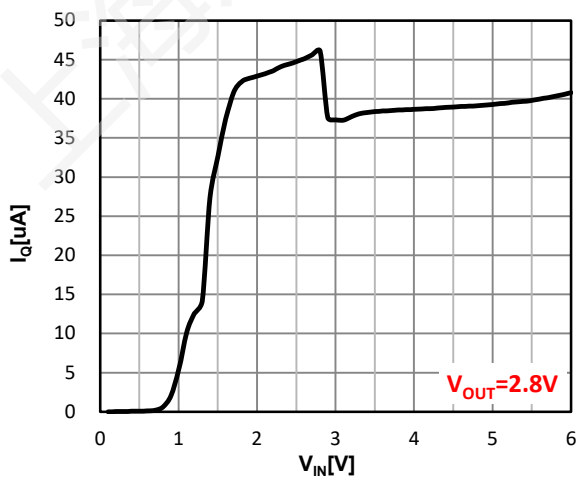


Figure 5. I_Q vs V_{IN}

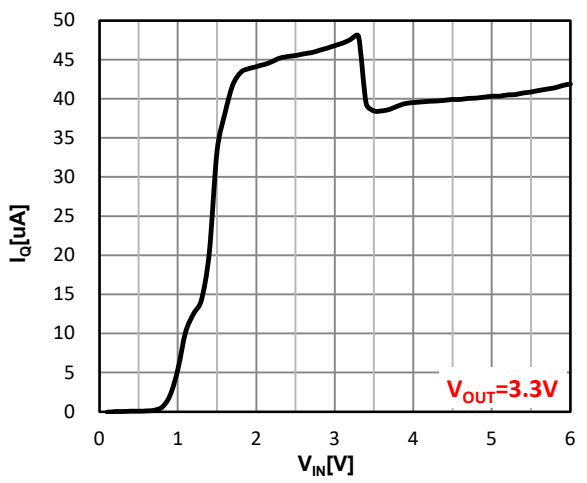


Figure 6. I_Q vs V_{IN}

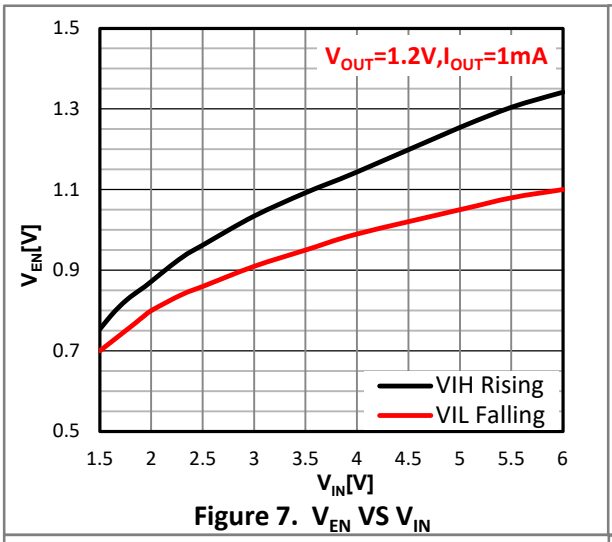


Figure 7. V_{EN} VS V_{IN}

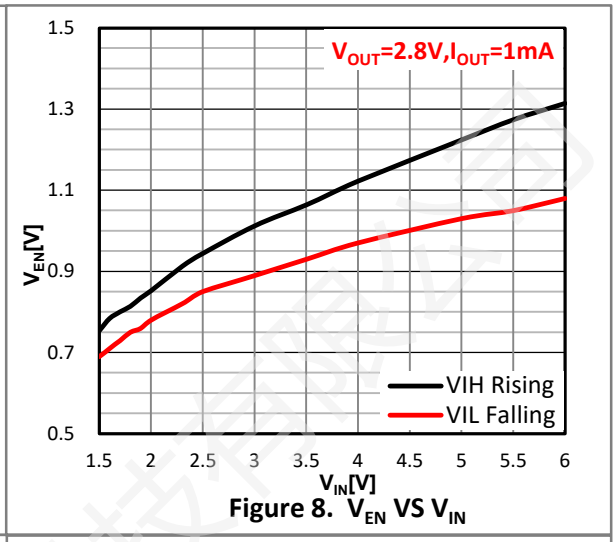


Figure 8. V_{EN} VS V_{IN}

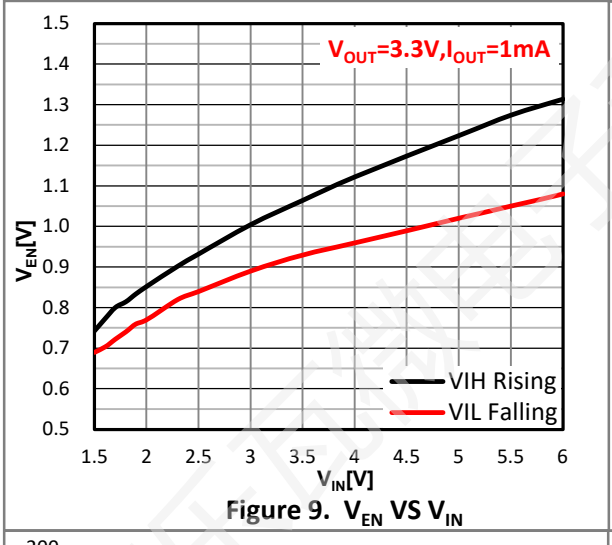


Figure 9. V_{EN} VS V_{IN}

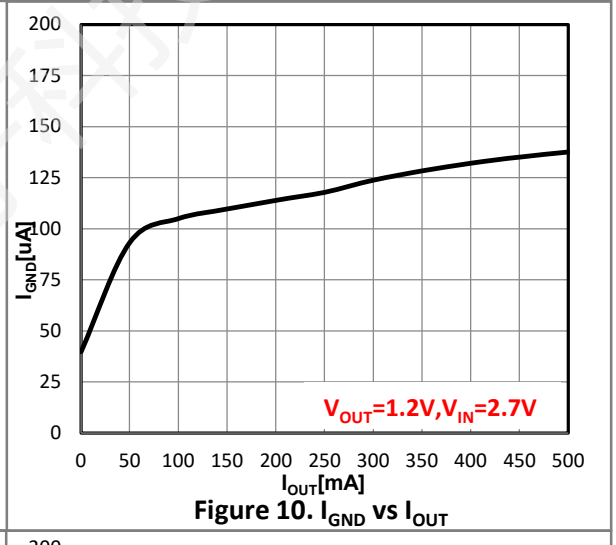


Figure 10. I_{GND} vs I_{OUT}

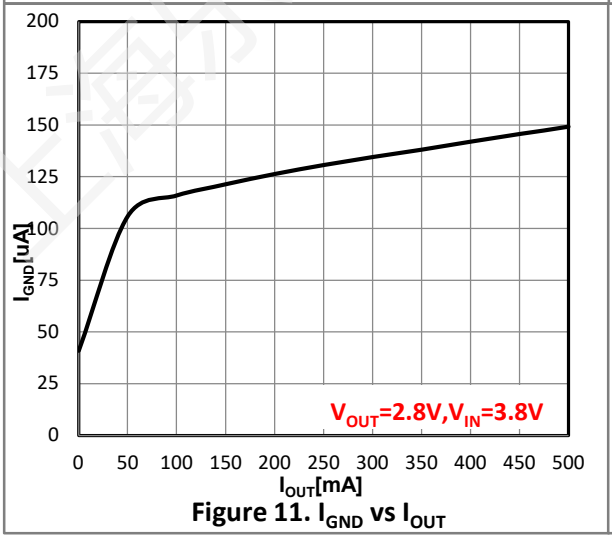


Figure 11. I_{GND} vs I_{OUT}

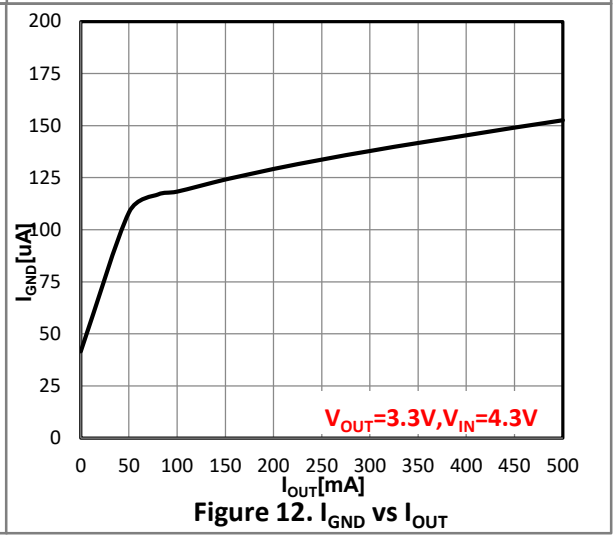


Figure 12. I_{GND} vs I_{OUT}

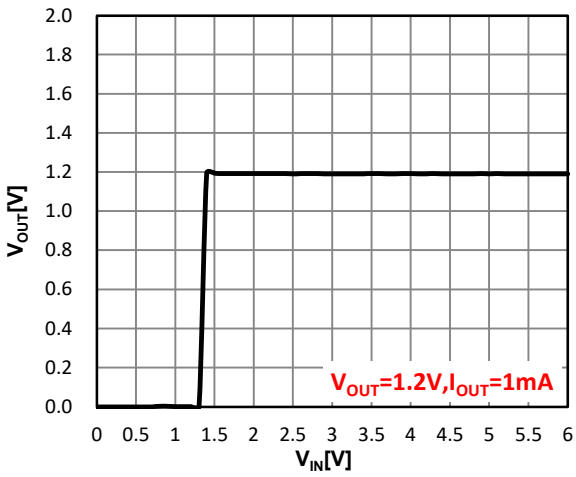


Figure 13. V_{OUT} vs V_{IN}

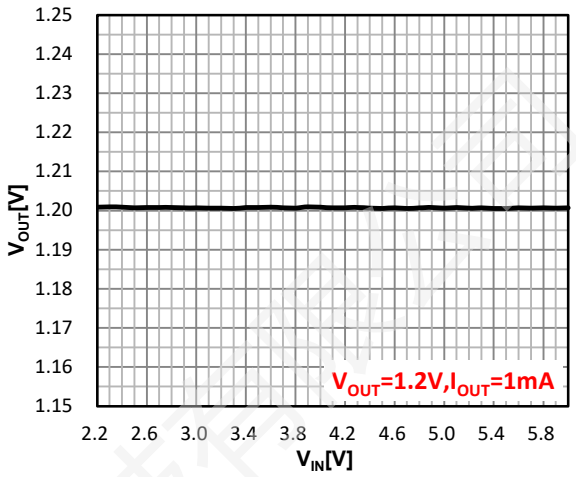


Figure 14. Line Regulation

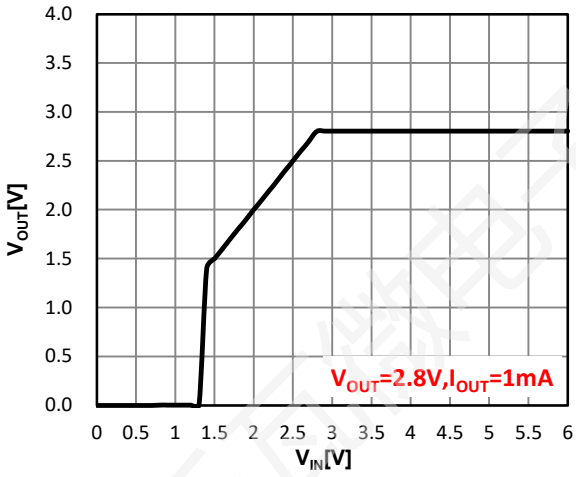


Figure 15. V_{OUT} vs V_{IN}

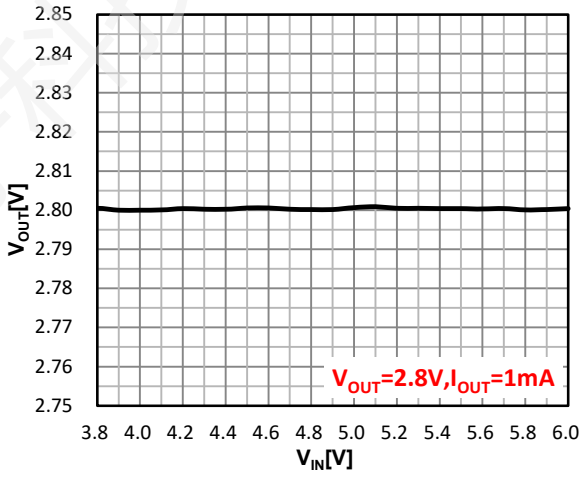


Figure 16. Line Regulation

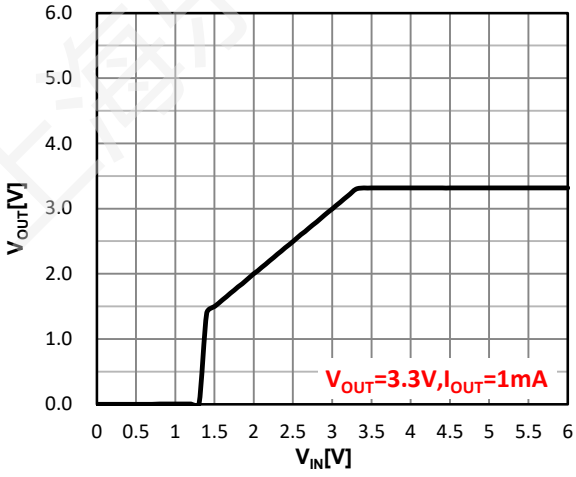


Figure 17. V_{OUT} vs V_{IN}

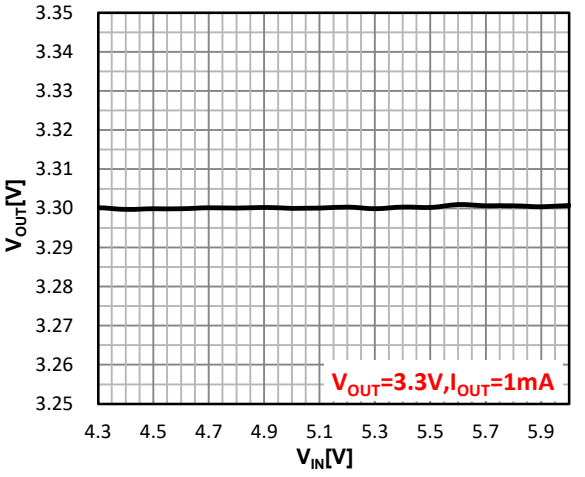


Figure 18. Line Regulation

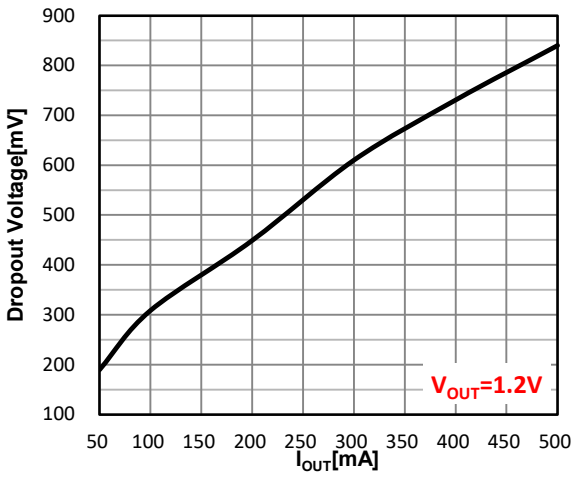


Figure 19. Dropout Voltage VS I_{OUT}

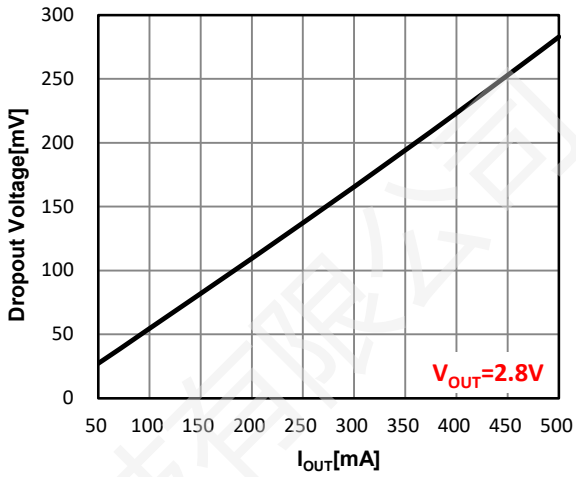


Figure 20. Dropout Voltage VS I_{OUT}

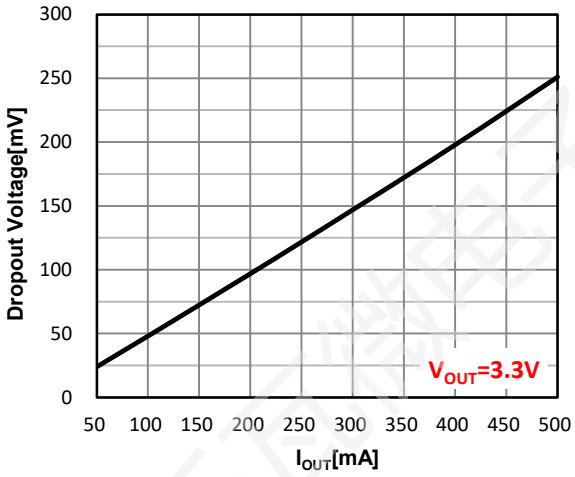


Figure 21. Dropout Voltage VS I_{OUT}

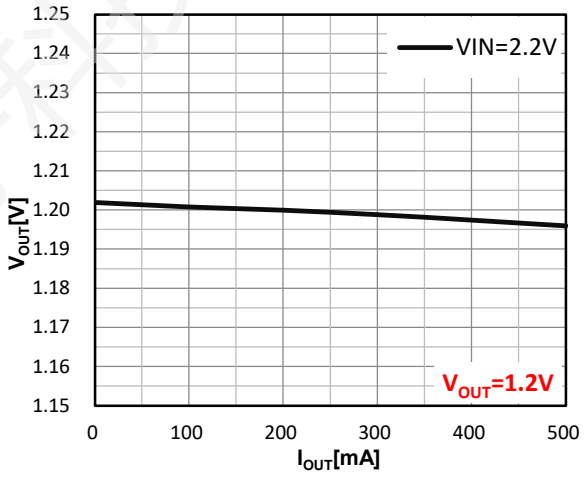


Figure 22. Load Regulation

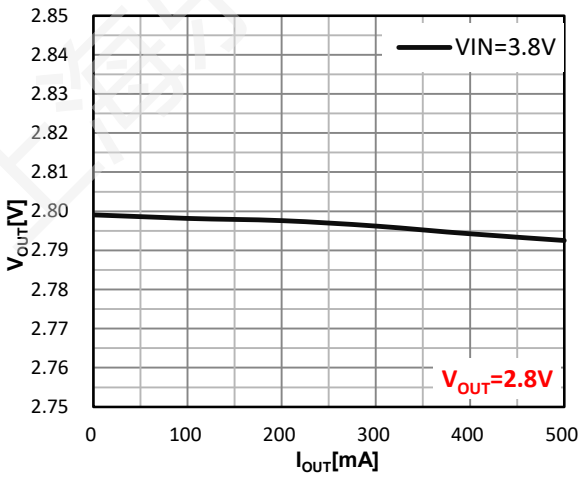


Figure 23. Load Regulation

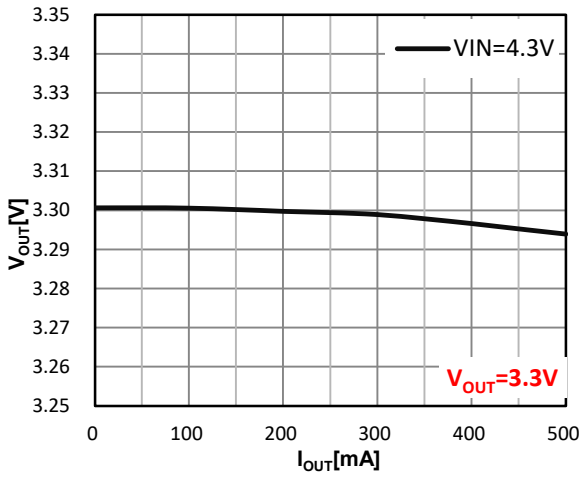
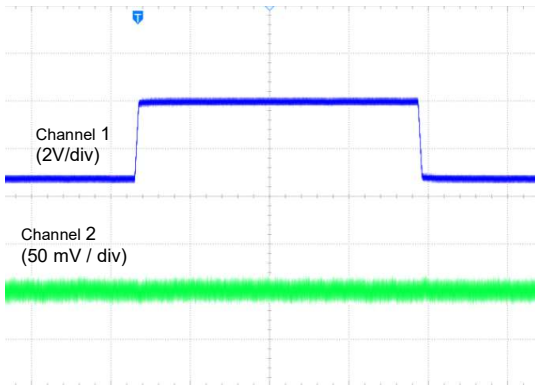


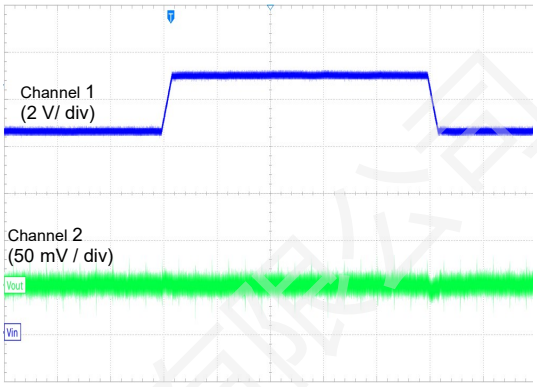
Figure 24. Load Regulation



Time (50 us / div)

Channel 1 = V_{IN}, Channel 2 =V_{OUT}, V_{IN}=2.7V→6.0V,
Tr=Tf=5us, V_{OUT}=1.2V, I_{OUT}=10mA

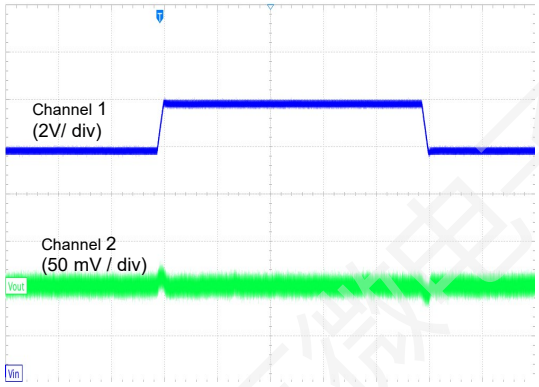
Figure 25. Line Transient



Time (50 us / div)

Channel 1 = V_{IN}, Channel 2 =V_{OUT}, V_{IN}=3.8V→6.0V,
Tr=Tf=5us, V_{OUT}=2.8V, I_{OUT}=10mA

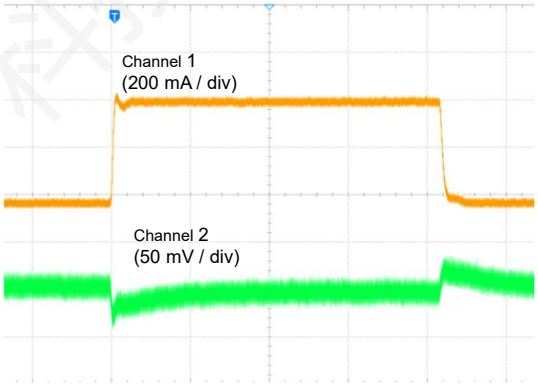
Figure 26. Line Transient



Time (50 us / div)

Channel 1 = V_{IN}, Channel 2 =V_{OUT}, V_{IN}=4.3V→6.0V,
Tr=Tf=5us, V_{OUT}=3.3V, I_{OUT}=10mA

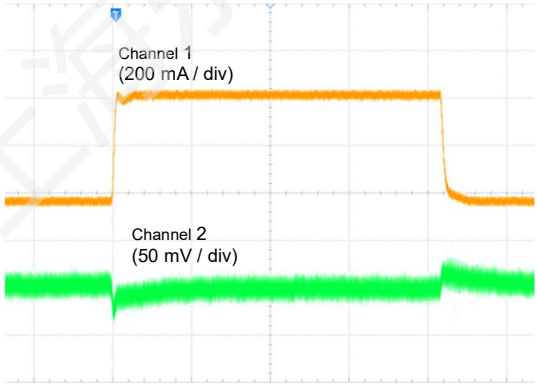
Figure 27. Line Transient



Time (200 us / div)

Channel 1 = I_{OUT}, Channel 2 =V_{OUT}, V_{IN}=3.0V, V_{OUT}=1.2V,
C_{IN}= C_{OUT}=1uF

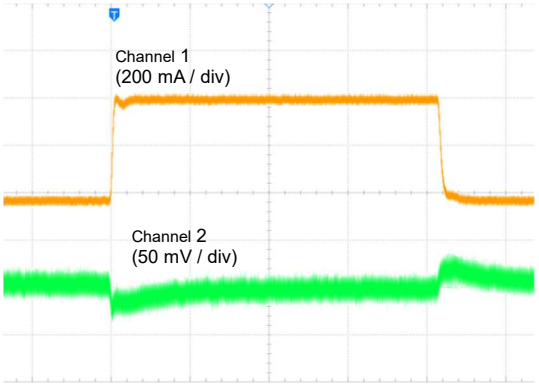
Figure 28. Load Transient (1 mA → 500 mA)



Time (200 us / div)

Channel 1 = I_{OUT}, Channel 2 =V_{OUT}, V_{IN}=3.8V, V_{OUT}=2.8V,
C_{IN}= C_{OUT}=1uF

Figure 29. Load Transient (1 mA → 500 mA)



Time (200 us / div)

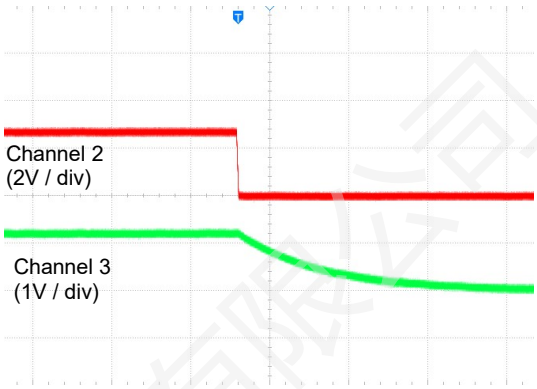
Channel 1 = I_{OUT}, Channel 2 =V_{OUT}, V_{IN}=4.3V, V_{OUT}=3.3V,
C_{IN}= C_{OUT}=1uF

Figure 30. Load Transient (1 mA → 500 mA)

Time (50 us / div)

Channel 2 =EN, Channel 3 =V_{OUT} ,V_{IN}=2.7V, EN=0→2.7V, V_{OUT}=1.2V, C_{IN}= C_{OUT}=1uF, No Load

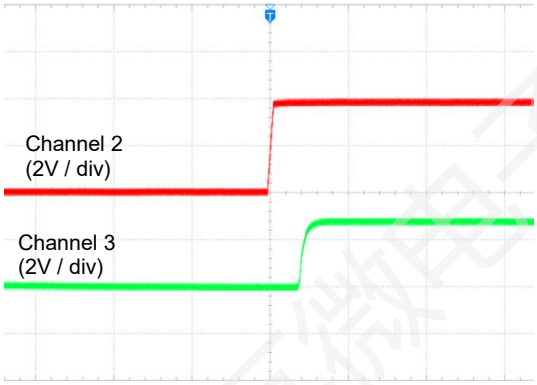
Figure 31. Start-Up with Enable



Time (200 us / div)

Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=2.7V, EN=2.7→0V, V_{OUT}=1.2V, C_{IN}= C_{OUT}=1uF,No Load

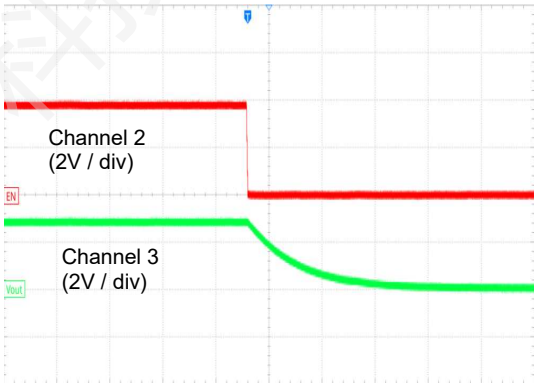
Figure 32. Shut-Down with Enable



Time (50 us / div)

Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=3.8V, EN=0→3.8V, V_{OUT}=2.8V, C_{IN}= C_{OUT}=1uF, No Load

Figure 33. Start-Up with Enable



Time (200 us / div)

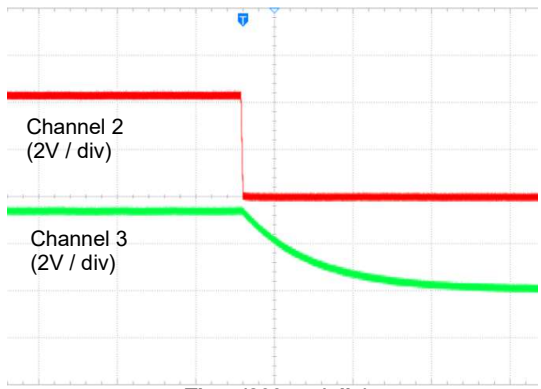
Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=3.8V, EN=3.8→0V, V_{OUT}=2.8V, C_{IN}= C_{OUT}=1uF, No Load

Figure 34. Shut-Down with Enable

Time (50 us / div)

Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=4.3V, EN=0→4.3V, V_{OUT}=3.3V, C_{IN}= C_{OUT}=1uF, No Load

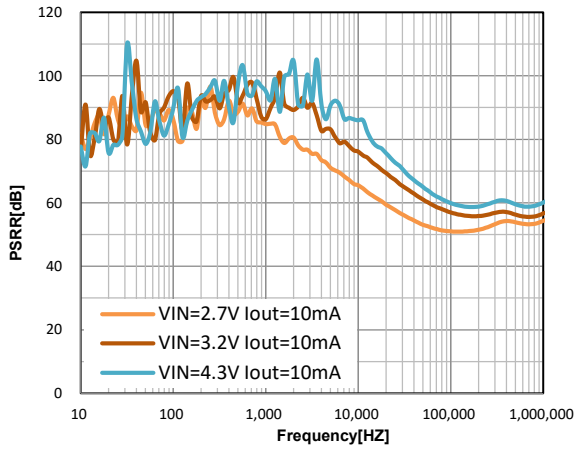
Figure 35. Start-Up with Enable



Time (200 us / div)

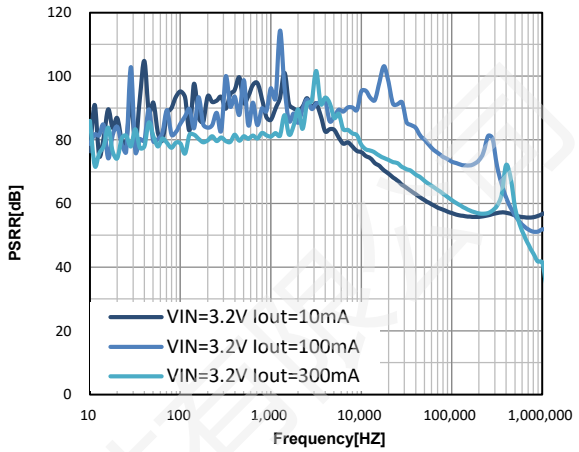
Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=4.3V, EN=4.3→0V, V_{OUT}=3.3V, C_{IN}= C_{OUT}=1uF, No Load

Figure 36. Shut-Down with Enable



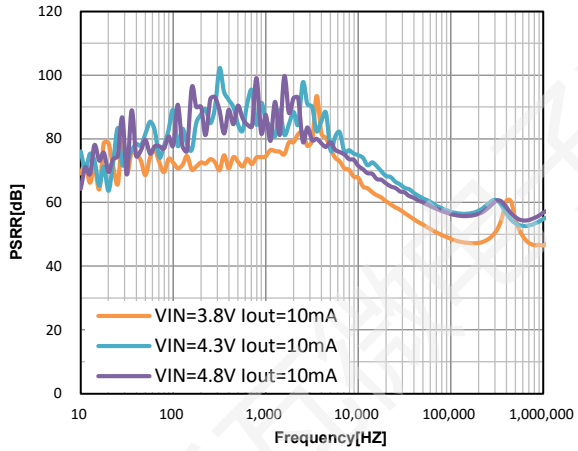
V_{OUT}=1.2V,V_{PP}=0.5V,C_{IN}=non,C_{OUT}=1uF,I_{OUT}=10mA

Figure 37. PSRR vs Frequency



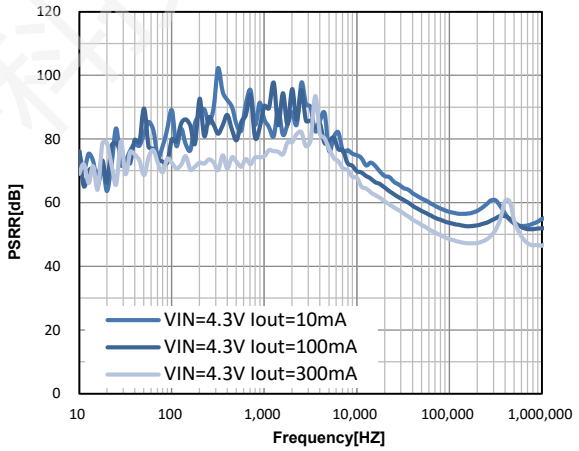
V_{OUT}=1.2V, V_{PP}=0.5V,C_{IN}=non,C_{OUT}=1uF,V_{IN}=V_{OUT}+2V

Figure 38. PSRR vs Frequency



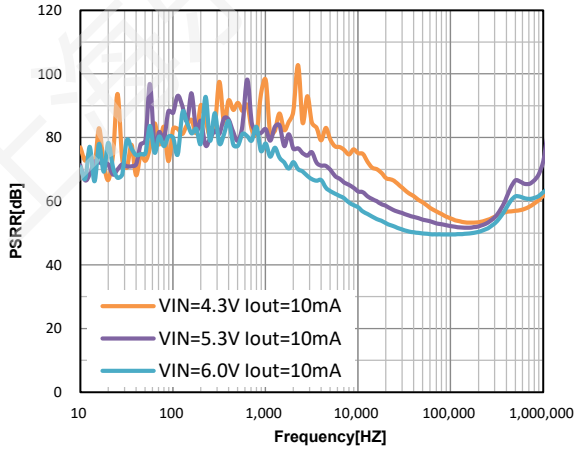
V_{OUT}=2.8V, V_{PP}=0.5V,C_{IN}=non, C_{OUT}=1uF,I_{OUT}=10mA

Figure 39. PSRR vs Frequency



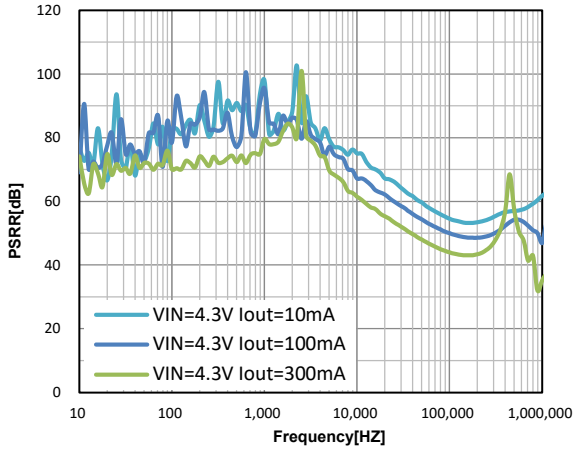
V_{OUT}=2.8V, V_{PP}=0.5V,C_{IN}=non, C_{OUT}=1uF,V_{IN}=V_{OUT}+1.5V

Figure 40. PSRR vs Frequency



V_{OUT}=3.3V, V_{PP}=0.5V,C_{IN}=non, C_{OUT}=1uF,I_{OUT}=10mA

Figure 41. PSRR vs Frequency



V_{OUT}=3.3V, V_{PP}=0.5V,C_{IN}=non, C_{OUT}=1uF,V_{IN}=V_{OUT}+1V

Figure 42. PSRR vs Frequency

APPLICATION INFORMATION:

- **Input Capacitor Selection**

Like any low-dropout regulator, the external capacitors used with the LW52XX Series must be carefully selected for regulator stability and performance. Using a capacitor whose value is >=1μF on the LW52XX Series input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance less than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

- **Output Capacitor Selection**

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LW52XX Series is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF on the LW52XX Series output ensures stability. An appropriate output capacitor can reduce noise and improve load transient response and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the LW52XX Series and returned to a clean analog ground.

- **Layout considerations**

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the PCB be designed with separate ground planes for VIN and VOUT, with each ground plane connected only at the GND pin of the device.

ORDER INFORMATION:

LW52①②③④⑤⑥

Designator	Item	Symbol	Description
①②	Output Voltage	12~50	e.g.1.2V→①=1,②=2
③④⑤⑥	Packages	N23C	SOT23
		N23D	SOT23-3L
		A23E	SOT23-5L
		N11E	DFN1x1-4L

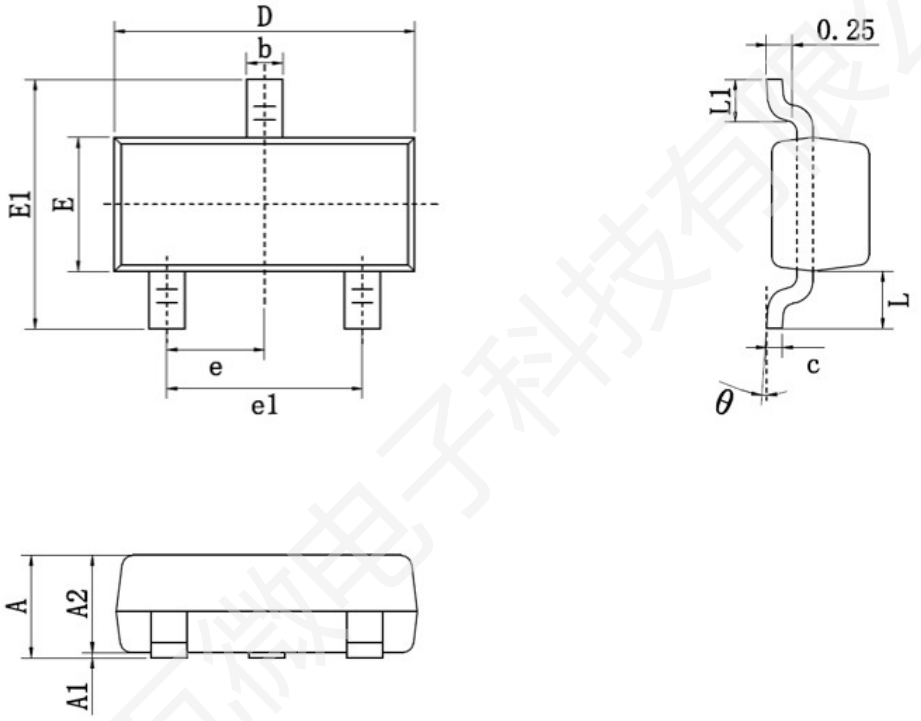
Part #	Output Voltage	Package	Shipping
LW5212N23C	1.2V	SOT23	3000 Pcs/ Tape & Reel
LW5215N23C	1.5V		
LW5218N23C	1.8V		
LW5222N23C	2.2V		
LW5225N23C	2.5V		
LW5228N23C	2.8V		
LW5230N23C	3.0V		
LW5233N23C	3.3V		
LW5236N23C	3.6V		
LW5242N23C	4.2V		
LW5250N23C	5.0V		
LW5212N23D	1.2V	SOT23-3L	3000 Pcs/ Tape & Reel
LW5215N23D	1.5V		
LW5218N23D	1.8V		
LW5222N23D	2.2V		
LW5225N23D	2.5V		
LW5228N23D	2.8V		
LW5230N23D	3.0V		
LW5233N23D	3.3V		
LW5236N23D	3.6V		
LW5242N23D	4.2V		
LW5250N23D	5.0V		

Part #	Output Voltage	Package	Shipping
LW5212A23E	1.2V	SOT23-5L	3000 Pcs/ Tape & Reel
LW5215A23E	1.5V		
LW5218A23E	1.8V		
LW5222A23E	2.2V		
LW5225A23E	2.5V		
LW5228A23E	2.8V		
LW5229A23E	2.9V		
LW5230A23E	3.0V		
LW5233A23E	3.3V		
LW5236A23E	3.6V		
LW5242A23E	4.2V		
LW5250A23E	5.0V		
LW5212N11E	1.2V	DFN1x1-4L	10000 Pcs/ Tape & Reel
LW5215N11E	1.5V		
LW5218N11E	1.8V		
LW5222N11E	2.2V		
LW5225N11E	2.5V		
LW5228N11E	2.8V		
LW5230N11E	3.0V		
LW5233N11E	3.3V		
LW5236N11E	3.6V		
LW5242N11E	4.2V		
LW5250N11E	5.0V		

If customers have special output voltage requirements, please contact us.

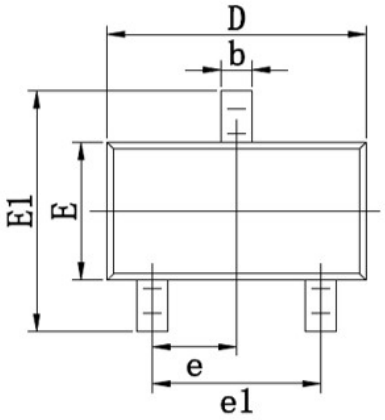
PACKAGE OUTLINE:

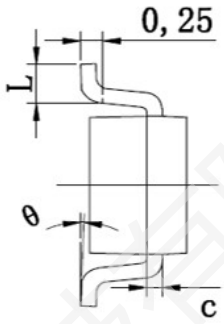
SOT23 Package

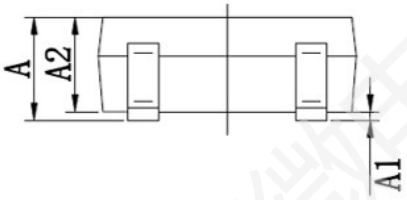


COMMON IN DIMENSION (MM)			
Symbol	**Min.**	**Nom.**	**Max.**
A	—	—	1.150
A1	0.000	—	0.100
A2	0.900	0.950	1.050
b	0.300	0.400	0.500
c	0.100	0.150	0.200
D	2.800	2.900	3.000
E	1.200	1.300	1.400
E1	2.250	2.400	2.550
e	0.950 TYP		
e1	1.800	1.900	2.000
L	0.550 REF		
L1	0.290	—	0.500

SOT23-3L Package

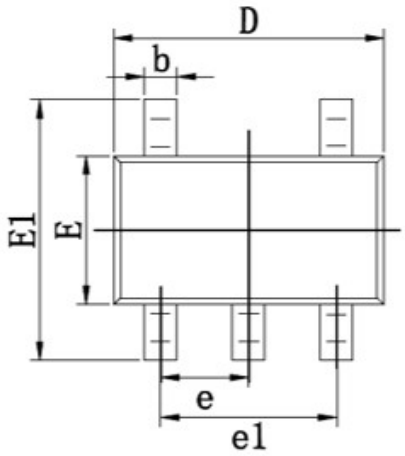


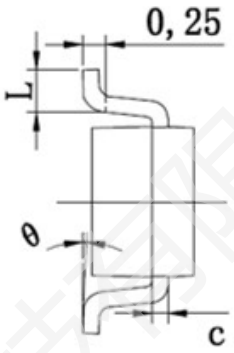


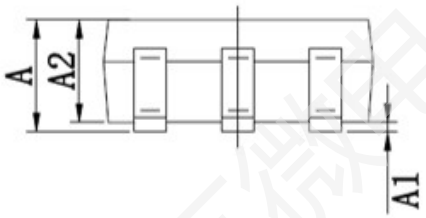


COMMON DIMENSION (MM)			
PKG	SOT23-3L		
Symbol	MIN	NOM	MAX
A	—	—	1.300
A1	0.010	—	0.150
A2	1.050	1.100	1.150
b	0.300	0.350	0.400
c	0.125	0.150	0.175
D	2.870	2.920	2.980
E	1.550	1.610	1.670
E1	2.650	2.850	3.000
e	0.95 BSC		
e1	1.800	1.900	2.000
L	0.300	0.450	0.600
θ	0°	4°	8°

SOT23-5L Package

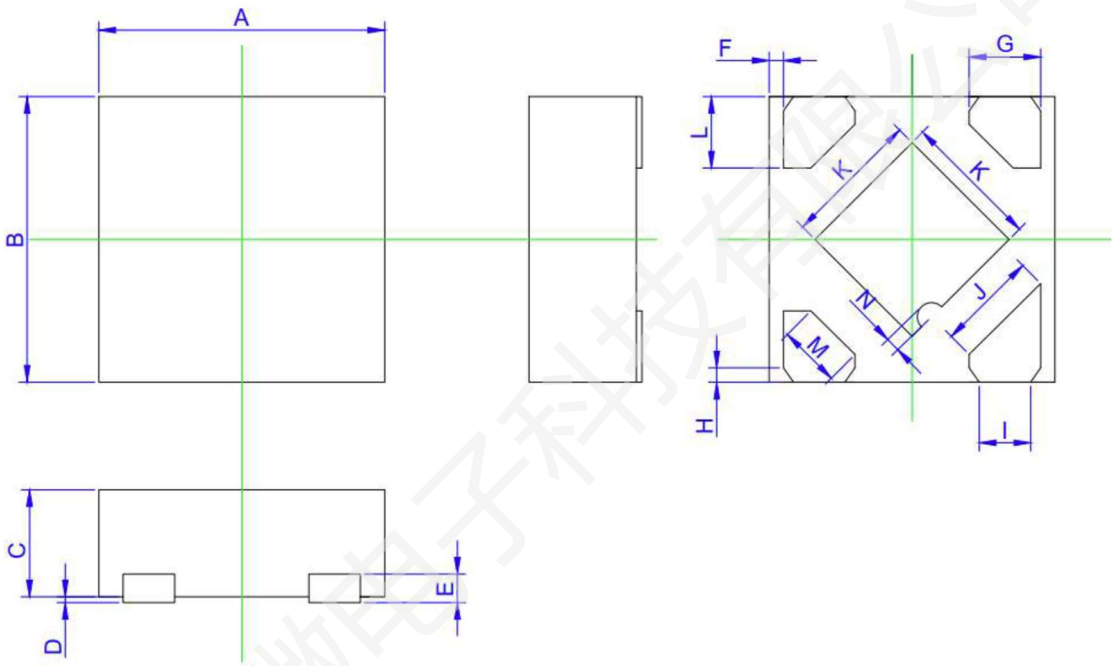






COMMON DIMENSION (MM)			
PKG	SOT23-5L		
Symbol	MIN	NOM	MAX
A	—	—	1.300
A1	0.010	—	0.150
A2	1.050	1.100	1.150
b	0.300	0.350	0.400
c	0.125	0.150	0.175
D	2.870	2.920	2.980
E	1.550	1.610	1.670
E1	2.650	2.850	3.000
e	0.95 BSC		
e1	1.800	1.900	2.000
L	0.300	0.450	0.600
θ	0°	4°	8°

DFN1x1-4L Package



符号	标准	下公差	上公差	下限值	上限值
A	1.0	0.03	0.03	0.97	1.03
B	1.0	0.03	0.03	0.97	1.03
C	0.375	0.03	0.03	0.345	0.405
D	0.02	0.005	0.02	0.015	0.04
E	0.10REF				
F	0.05REF				
G	0.25REF				
H	0.05REF				
I	0.18REF				
J	0.34REF				
K	0.48REF				
L	0.25REF				
M	0.245REF				
N	0.06REF				

Revision History:

Revision	Date	Descriptions
Rev 0.1	Oct.2021	Initial Version
Rev 0.2	Jan.2022	Update Feature and Electrical Characteristics
Rev 0.3	Mar.2022	Update Feature and Electrical Characteristics
Rev 0.4	May.2022	Define package type
Rev 1.0	Jun.2022	Formal Version
Rev 1.1	Aug.2022	Add Test Condition for Typical Operating Chracteristics 13
Rev 1.2	Sep.2022	Adjust Order Information
Rev 1.3	Apr. 2023	Add TSD hysteresis in EC Table
Rev 1.4	Jun. 2023	Modify Typical Operating Characteristcs 9-12
Rev 1.5	July. 2026	Update Electrical Characteristics And Typical Operating Characteristics

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