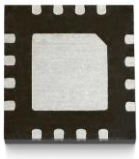
DATA SHEET

RELEASE Ø DATA SHEET



GRF5603

RFID Power Amplifier 865 to 928 MHz

FEATURES

- 250 mA Native Mode Quiescent Current Consumption
- Flexible Biasing for Linearity Optimization
- 5 V Supply Voltage
- 50 Ω Single-ended Input and Output Impedance
- Digital Shutdown
- Rugged Design is Extremely Resilient to Mismatched Loads
- -40 to 85 °C Operating Temperature Range
- Compact 3 x 3 mm QFN-16 Package
- ETSI EN 302 208 Mask Compliance at 33 dBm P_{OUT}

Reference: 5 V / 250 mA I_{CCQ} / 902 MHz

- Gain: 32 dB
- OIP3: 44.8 dBm
- OP1dB: 37 dBm
- Evaluation Board Noise Figure: 2.6 dB

APPLICATIONS

- RFID
- General Purpose Amplifier
- ISM Band Linear Applications

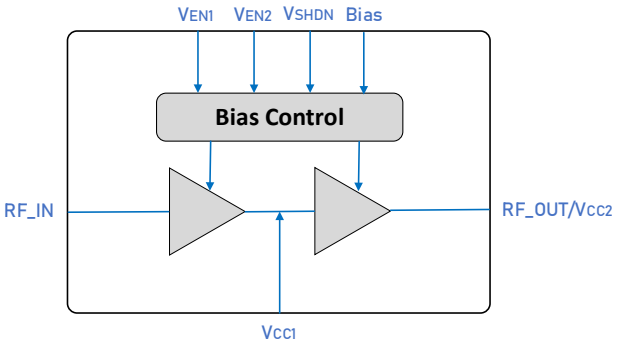
DESCRIPTION

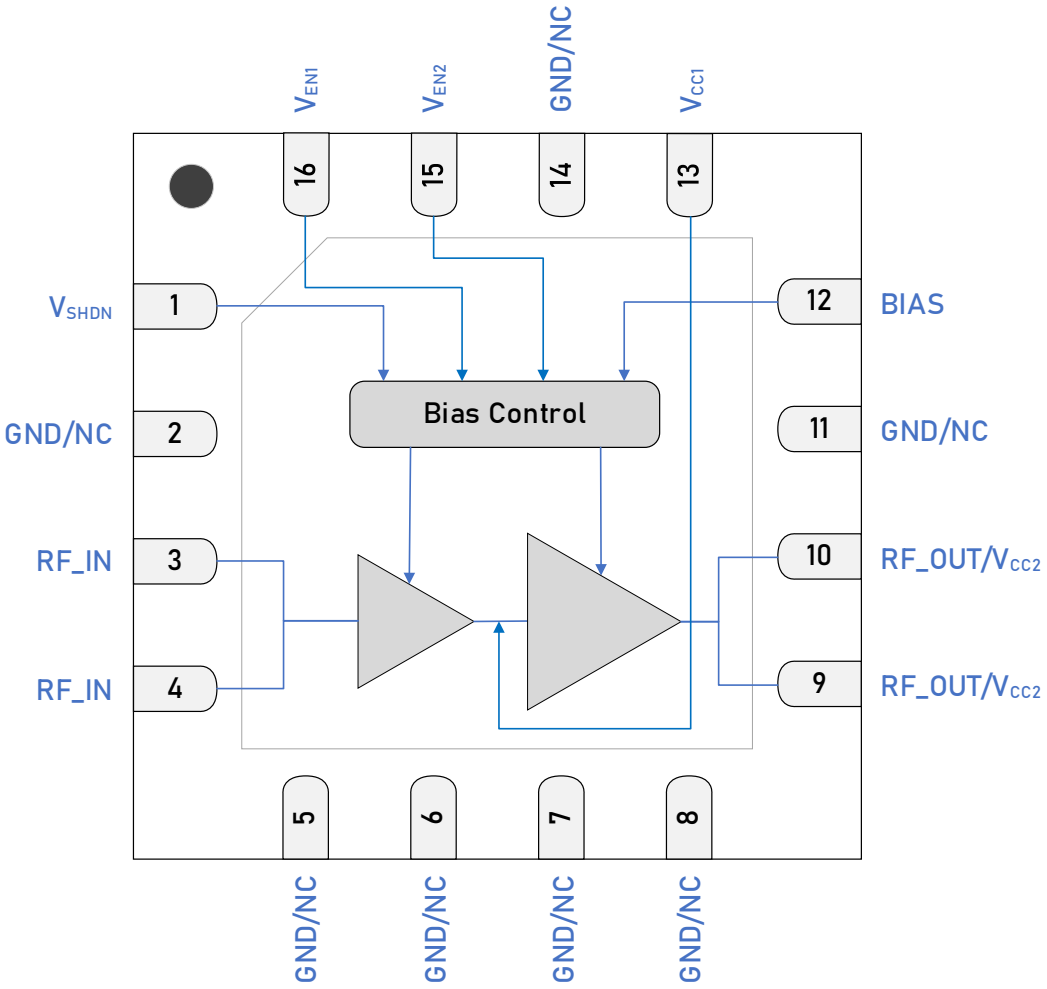
The GRF5603 is a high gain, two-stage InGaP HBT power amplifier designed for 865 to 928 MHz RFID applications.

Please consult with the GRF applications engineering team for custom tuning/evaluation board data and device S-parameters.

Additional tunes can be found on the GRF5603 "Custom Tunes" product page: GRF5603 Custom Tunes

BLOCK DIAGRAM





3 x 3 mm QFN-16 Pin Out (Top View)

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Pin Assignments

Pin	Name	Description	Note
1	V_{SHDN}	Digital Shutdown Pin	$V_{SHDN} \geq 1.8$ V (Logic HIGH) disables device. $V_{SHDN} \leq 0.8$ V (Logic LOW) enables device.
2, 5, 6, 7, 8, 11, 14	GND/NC	Ground or No Connect	No internal connection to die. These pins can be left unconnected or connected to ground (recommended). Use a via as close to the pin as possible if grounded.
3, 4	RF_IN	RF Input	Pins 3 and 4 tied together on system board. An external DC blocking capacitor must be used.
9, 10	RF_OUT/V_{CC2}	PA Output/Bias Voltage	Pins 9 and 10 tied together on system board. V_{CC2} must be applied to this pin through an RF choke.
12	Bias	Bias Circuit Supply	Connect to V_{CC2} through external resistor.
13	V_{CC1}	Bias Voltage	Connect to V_{CC1} through external inductor with capacitive termination above (see applications schematic).
15	V_{EN2}	Enable2 Voltage Input	V_{EN2} and series resistor sets I_{CCQ} for the output stage. $V_{EN2} \leq 0.2$ volts disables stage 2.
16	V_{EN1}	Enable1 Voltage Input	V_{EN1} and series resistor sets I_{CCQ} for the input stage. $V_{EN1} \leq 0.2$ volts disables stage 1. Connecting an external de-coupling capacitor to ground is required for optimal NF performance.
PKG BASE	GND	Ground	Provides DC and RF ground for the amplifier as well as thermal heat sink. Recommend multiple 8-mil vias beneath the package for optimal RF and thermal performance. Refer to evaluation board top layer graphic on schematic page.

Truth Table

Pin	Logic	Condition
V_{SHDN}	LOW	Full Operation
	HIGH	All Amplifiers Off
V_{EN1}	LOW	Stage 1 Amplifier Off
	HIGH	Stage 1 Amplifier On
V_{EN2}	LOW	Stage 2 Amplifier Off
	HIGH	Stage 2 Amplifier On

ON/OFF Options:

Off State has two options.

Option 1: offers convenience of a single shutdown pin. Option 2: with minimal leakage.

Option	Device State	V_{CC}	V_{EN1}	V_{EN2}	V_{SHDN}	Comments
1	OFF	High	High	High	High	V_{EN} currents exist approximately 0.8 mA per, Vcc leakage = 9 uA.
2	OFF	High	Low	Low	Low	V_{EN} currents = 0, Vcc leakage = 9 uA.
3	ON	High	High	High	Low	V_{EN} currents = 0.4 mA per, I_{CCQ} = 250 mA.

Absolute Ratings

Parameter		Symbol	Min.	Max.	Unit
Supply Voltage		V_{CC}	3	5.25	V
RF Input Power	Load VSWR = 1:1, 50 Ω, V_{CC} = 5 V, CW Tone, 100% Duty Cycle, $T_{PKG\ BASE}$ = 25 °C.	$P_{IN\ MAX-1:1}$		15	dBm
	Load VSWR ≤ 8:1, all phase angles, V_{CC} = 5 V, CW Tone, 100% Duty Cycle, $T_{PKG\ BASE}$ = -40 to 85 °C.	$P_{IN\ MAX-8:1}$		4	
Operating Temperature (package base).		$T_{PKG\ BASE}$	-40	85	°C
Maximum Junction Temperature (MTTF > 10^6 hours).		$T_{J\ MAX}$		190	°C
Maximum Dissipated Power Stage 1. DC only (no RF applied).		$P_{DISS\ MAX}$		700	mW
Maximum Dissipated Power Stage 2. DC only (no RF applied).		$P_{DISS\ MAX}$		1800	mW
Shutdown Voltage		V_{SHDN}		* 4.0	V

Electrostatic Discharge

Human Body Model		HBM	TBD		V

Storage

Storage Temperature		T_{STG}	-65	150	°C
Moisture Sensitivity Level		MSL		1	--

* V_{SHDN} = 4 V yields I_{SHNDN} = 382 µA. I_{SHDN} decreases linearly vs V_{SHDN} (to 73 µA with V_{SHDN} = 1.8 V).

Said linear relationship can be used to insert/scale Bias R on V_{SHDN} line for higher V_{SHDN} voltage: use the pin condition V_{SHDN_pin}/I_{SHDN} = 2.4V/155µA.

Calculate Bias R for V_{SHDN}/I_{SHDN} = 4V/155µA: Bias R = (4-2.4)/(0.000155) = 10.3 kΩ.

Caution! ESD Sensitive Device.
Exceeding Absolute Maximum Rating conditions may cause permanent damage.

Note: For additional information, please refer to *Manufacturing Note MN-001 — Package and Manufacturing Information.*

RoHS compliant

All Guerrilla RF products are provided in RoHS compliant lead (Pb)-free packaging requiring no exemptions. Additional information for this topic can be found at this link - *Environmental and Restricted Substance Statement Library*

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Recommended Operating Conditions

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	3	5	5.25	V	
RF Frequency Range	F_{RF}	865		928	MHz	Typical application schematic using the 865 to 928 MHz tuning set **(note 1)**.
Operating Temperature (package base)	$T_{PKG\ BASE}$	-40		85	°C	
RF_IN Port Impedance	Z_{RFIN}		50		Ω	Single-ended with 3 element match.
RF_OUT Port Impedance	Z_{RFOUT}		50		Ω	Single-ended with 5 element match.

Note 1: Operation outside of this range is supported by using different custom tunes. Examples of other optimized tunes can be found here: GRF5603 Custom Tunes

Note 2: Contact the Guerrilla RF applications team for guidance on optimizing the tuning of the device for alternative bands.

Nominal Operating Parameters – General

The following conditions apply unless noted otherwise: typical application schematic using the 865 to 928 MHz tuning set. $V_{CC}/V_{EN1}/V_{EN2}$ = 5 V, V_{SHDN} = LOW, I_{CCQ} = 250 mA, F_{TEST} = 902 MHz, M1 = 6.8 kΩ, M5 = 6.8 kΩ, 50 Ω system impedance, $T_{PKG\ BASE}$ = 25 °C. Evaluation board losses are included within the specifications.

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Supply Quiescent Current	I_{CCQ}		250		mA	I_{CCQ1} + I_{CCQ2}. No RF applied.
Enable Current 1	$I_{ENABLE1}$		0.6		mA	$V_{CC}/V_{EN1}/V_{EN2}$ = 5 V, V_{SHDN} = 0 V.
Enable Current 2	$I_{ENABLE2}$		0.7		mA	$V_{CC}/V_{EN1}/V_{EN2}$ = 5 V, V_{SHDN} = 0 V.
Operating Temperature Range	$T_{PKG\ BASE}$	-40		85	°C	Measured on package base.
Logic Input Low	V_{IL}	0		0.8	V	Applies to V_{SHDN} Input.
Logic Input High	V_{IH}	1.8		4	V	Applies to V_{SHDN} Input.
Logic Current Low	I_{IL}		1.3		nA	Applies to V_{SHDN} Input, V_{IL} ≤ 0.8 V.
Logic Current High	I_{IH}		72		µA	Applies to V_{SHDN} Input, V_{IH} = 1.8 V.
			280			Applies to V_{SHDN} Input, V_{IH} = 3.3 V.
Switching Rise Time	T_{RISE}		20		ns	Applies to V_{SHDN} Input.
Switching Fall Time	T_{FALL}		20		ns	Applies to V_{SHDN} Input.

Disabled Mode

Supply Quiescent Current	$I_{CCQ-SHDN}$		10		µA	V_{CC} = 5 V, $V_{SHDN}/V_{EN1}/V_{EN2}$ = HIGH.
Enable Current 1	$I_{ENABLE1-SHDN}$		0.7		mA	V_{CC} = 5 V, $V_{SHDN}/V_{EN1}/V_{EN2}$ = HIGH.
Enable Current 2	$I_{ENABLE2-SHDN}$		0.7		mA	V_{CC} = 5 V, $V_{SHDN}/V_{EN1}/V_{EN2}$ = HIGH.

Thermal Data: Stage 1 and Stage 2

Stage 1: Thermal Resistance (Infrared Scan). DC only (no RF applied).	Θ_{JC}		62		°C/W	
Stage 2: Thermal Resistance (Infrared Scan). DC only (no RF applied).	Θ_{JC}		19.5		°C/W	
See plot of Die temperature vs. P_{OUT}	Tj				°C	On standard evaluation board **(note 2)**.

Note 2: MTTF > 10^6 hours for T_J ≤ 190 °C.

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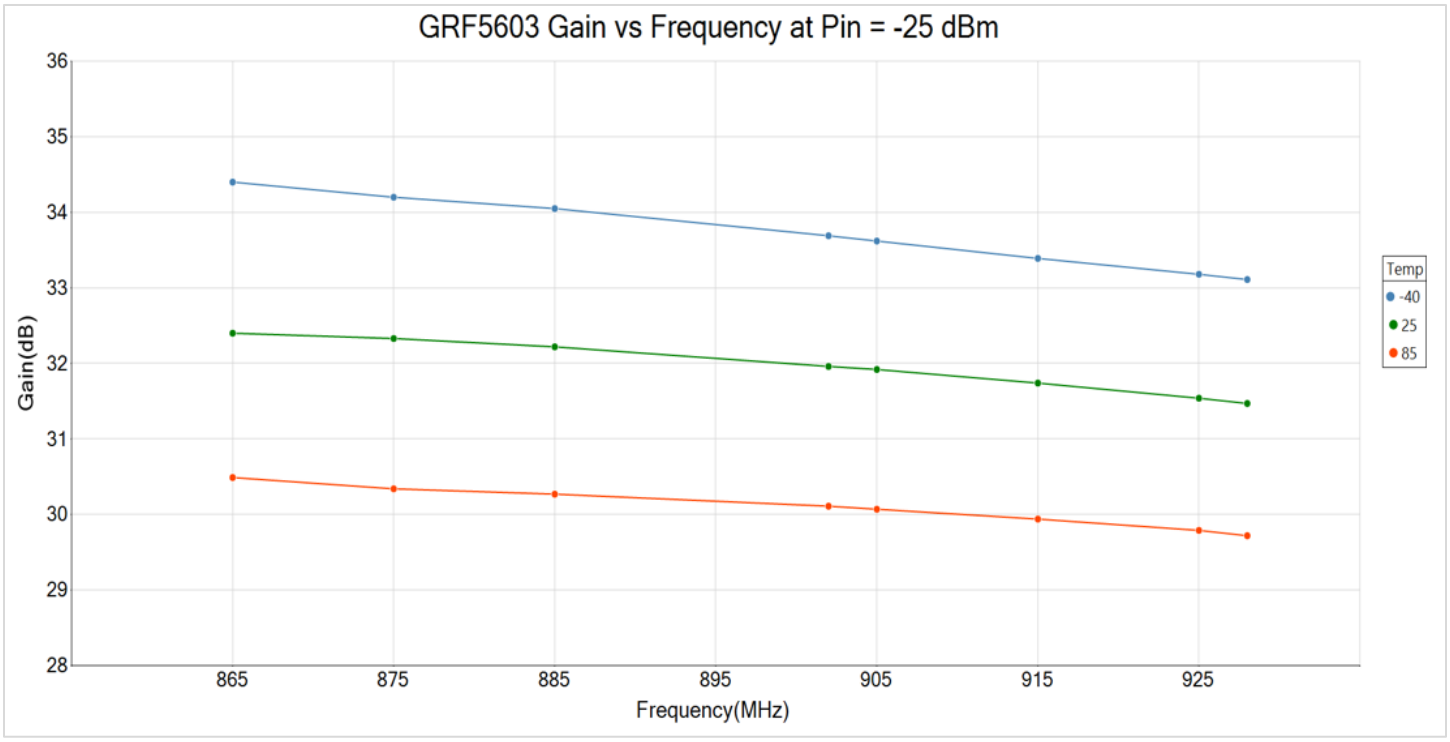
Nominal Operating Parameters – RF: 865 to 928 MHz

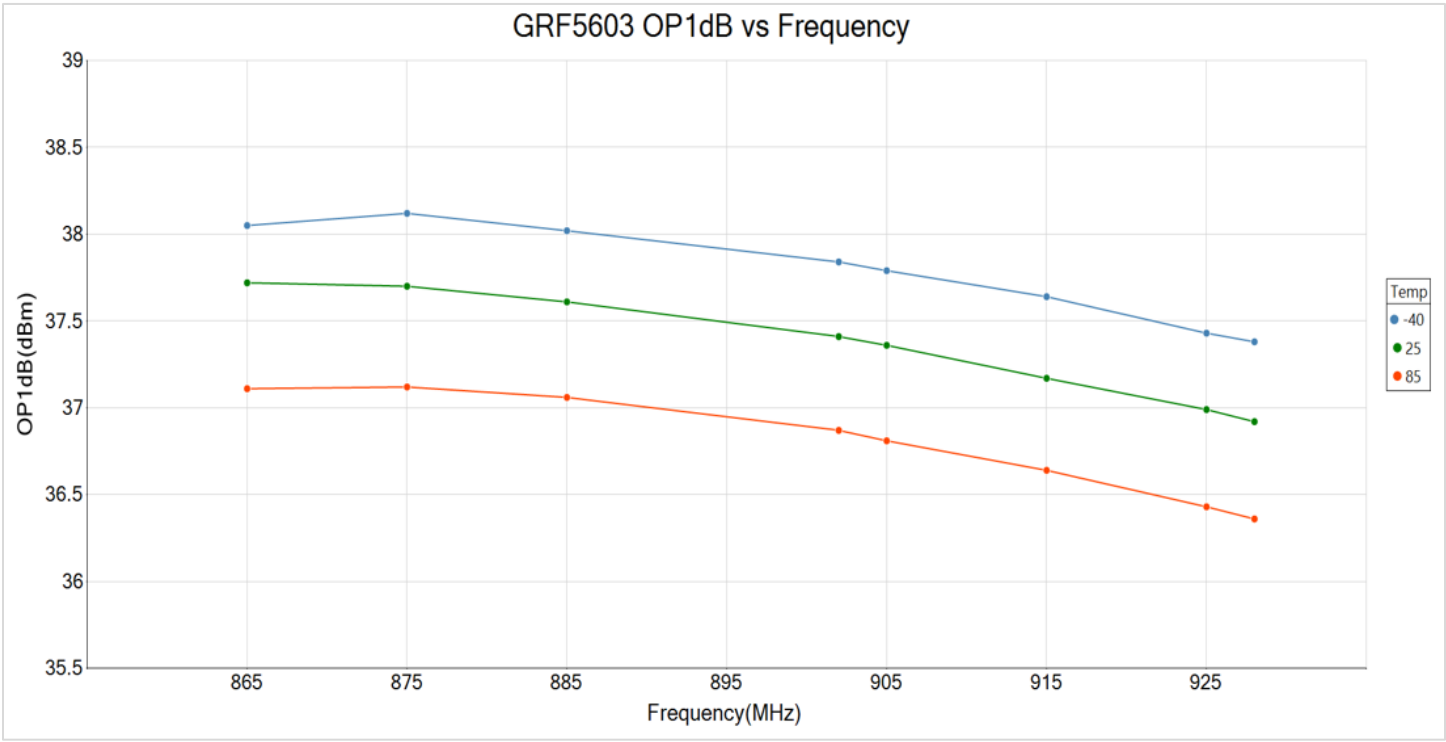
The following conditions apply unless noted otherwise: typical application schematic using the 865 to 928 MHz tuning set. $V_{CC}/V_{EN1}/V_{EN2}$ = 5 V, V_{SHDN} = LOW, I_{CCQ} = 250 mA, F_{TEST} = 902 MHz, M1 = 6.8 kΩ, M5 = 6.8 kΩ, 50 Ω system impedance, $T_{PKG\ BASE}$ = 25 °C. Evaluation board losses are included within the specifications.

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Small Signal Gain	S21		32		dB	F_{TEST} = 902 MHz, V_{CC} = 5 V, P_{IN} = -25 dBm.
Standby Mode Gain	$S21_{STBY}$		-35		dB	Disabled mode: $V_{SHDN}/V_{EN1}/V_{EN2}$ = HIGH, P_{IN} = 0 dBm.
Input Return Loss	S11		< -14		dB	F_{RF} = 865 to 928 MHz.
Output Return Loss	S22		< -12		dB	F_{RF} = 865 to 928 MHz.
Reverse Isolation	S12		< -43		dB	F_{RF} = 865 to 928 MHz.
Noise Figure	NF		2.6		dB	On standard evaluation board.
Output 3rd Order Intercept Point	OIP3		44.8		dBm	22 dBm P_{OUT} per tone at 600 kHz spacing (901.7 and 902.3 MHz).
Output 1 dB Compression Power	OP1dB		37		dBm	V_{CC} = 5 V, Sine wave input.

Note 3: MIN/MAX limits defined using *modelled estimates* that account for part-to-part variations and expected process spreads. As additional production lots are fabricated, accumulated test data will be used to refine the MIN/MAX limits.

GRF5603 Typical Operating Curves: 865 to 928 MHz Tune





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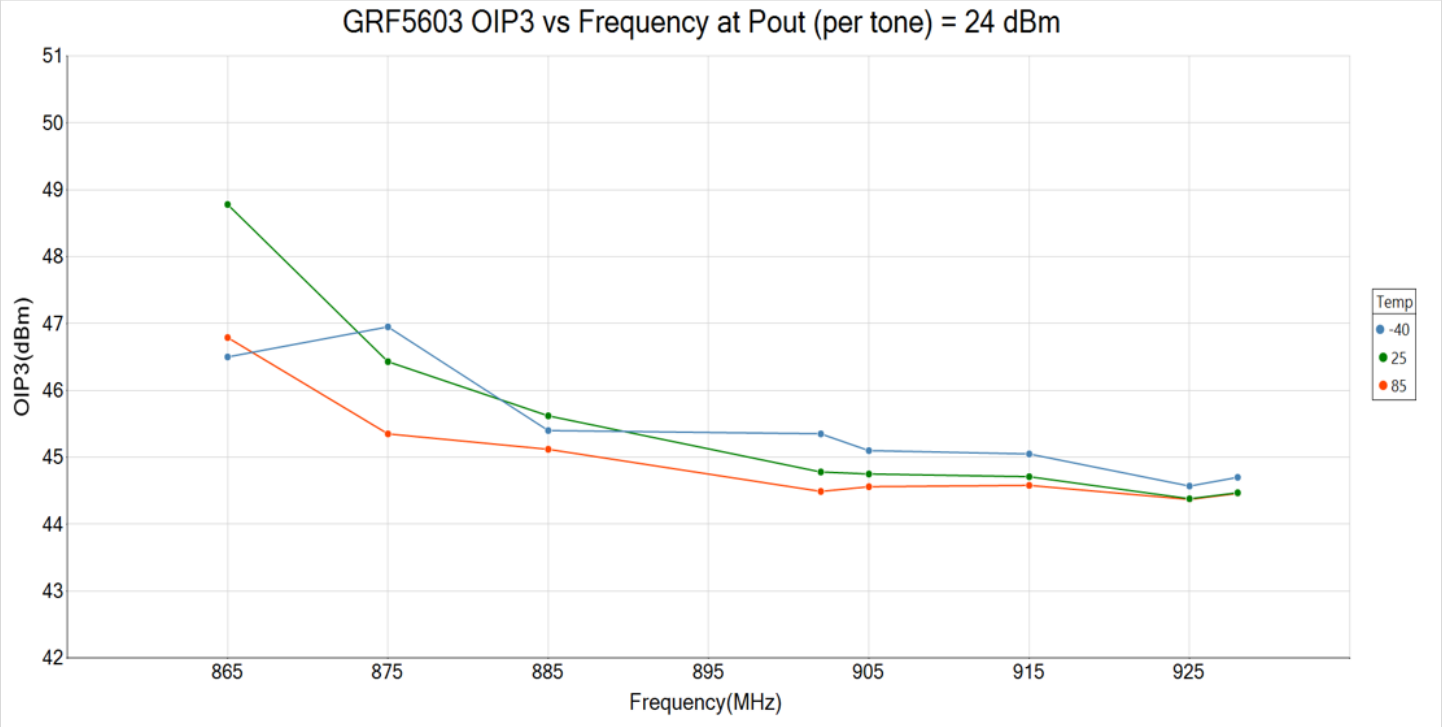
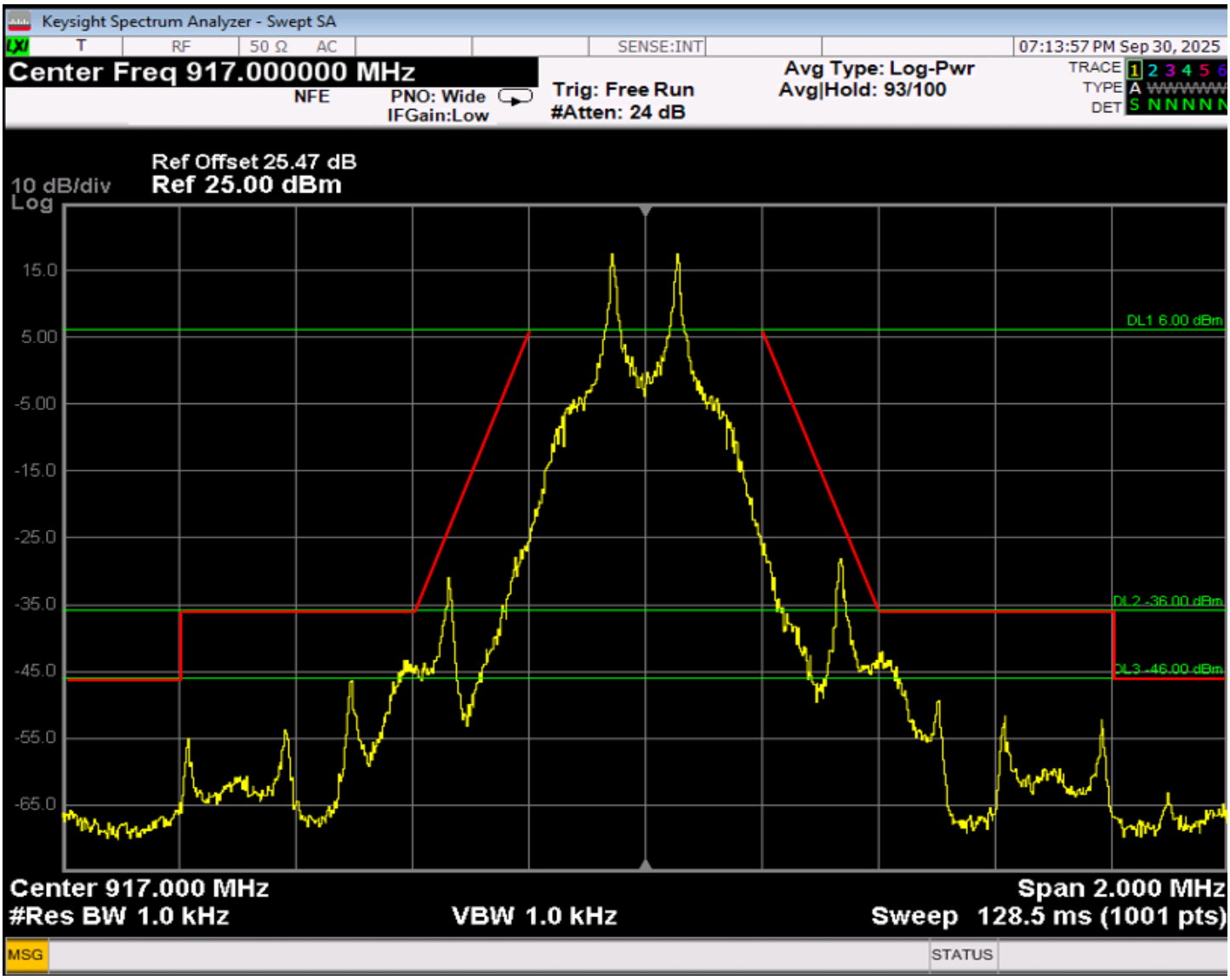
GRF5603 Typical Operating Curves: 865 to 928 MHz Tune



GRF5603: 917 MHz RFID Mask (Signal = 1.5PIE 7.14TARI, P_{OUT} = 33 dBm)



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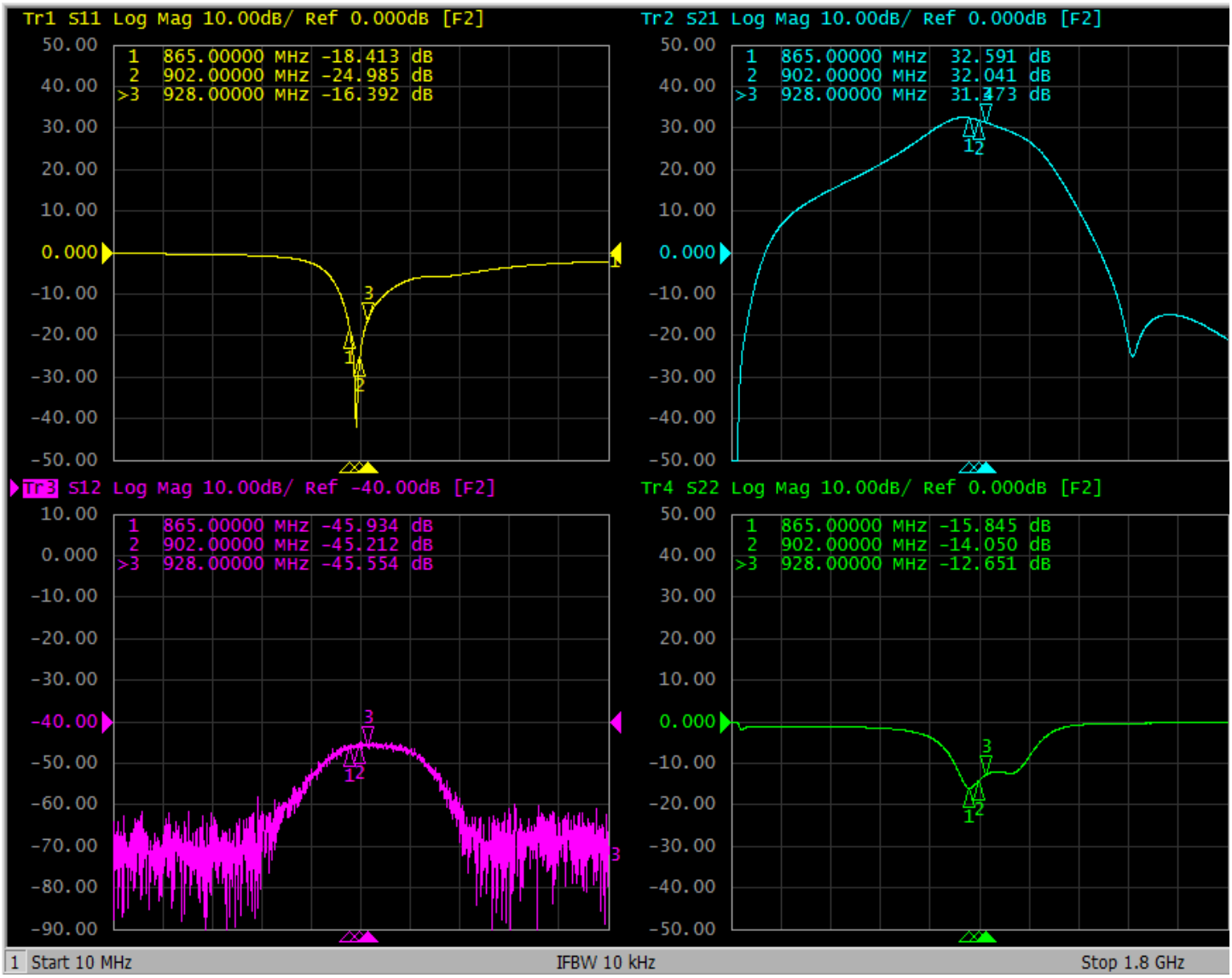
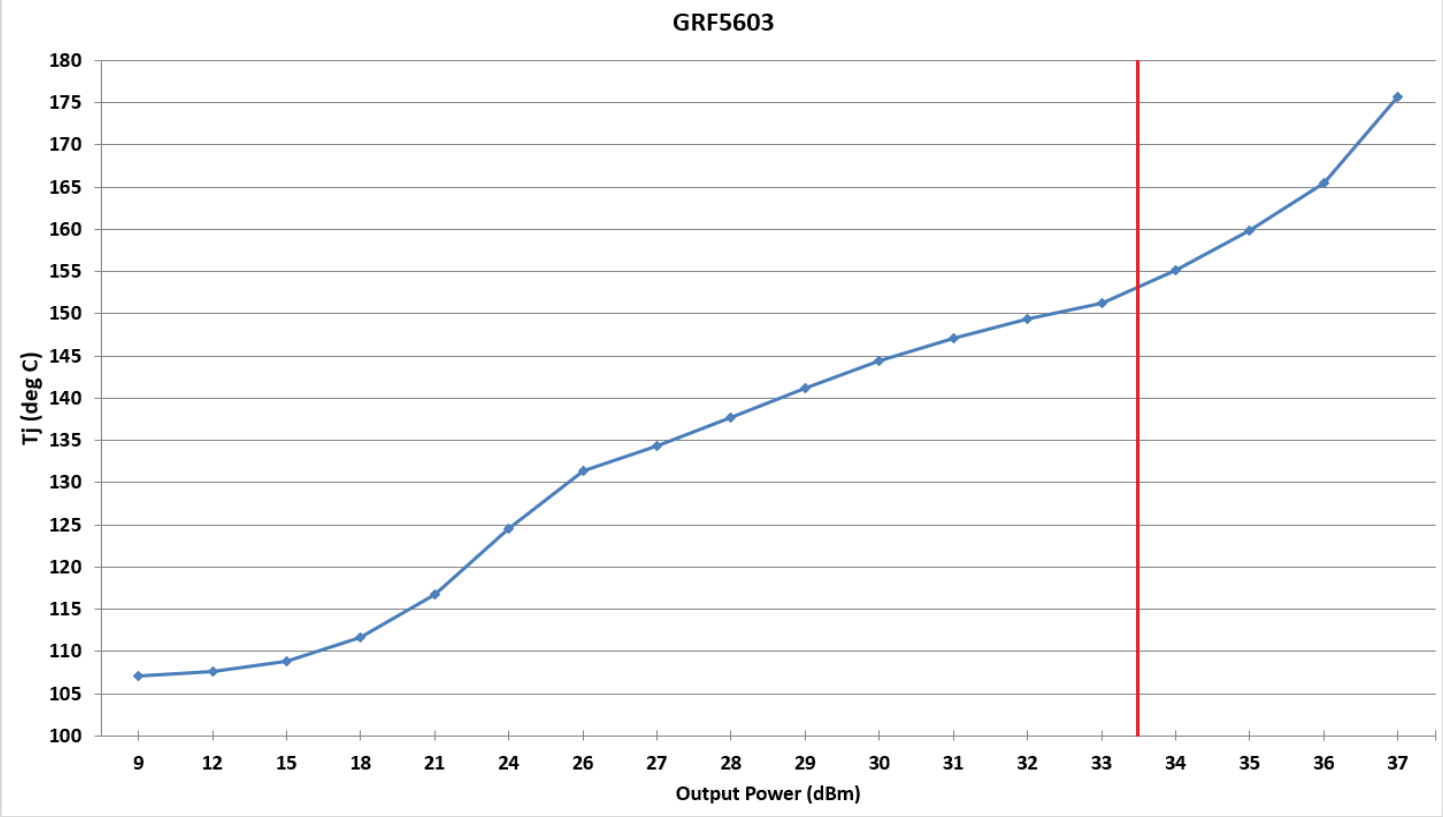
GRF5603 Typical Operating Curves: S-Parameters (865 to 928 MHz Tune)



GRF5603 Typical Operating Curves: Junction Temperature (per application schematic at 85 °C)

GRF5603, being a 2-stage device, sees one of the stages governing junction temperature over power sweep. Red line = 33.5 dBm shows where Tj is equivalent at both stages. At left of red line, stage 2 governs Tj (Q2 Tj is higher). To the right of red line, stage 1 governs Tj (Q1 Tj is higher). Setting bias resistors M1/M5 per application schematic ensures best linearity and yields thermal performance shown in the plot.



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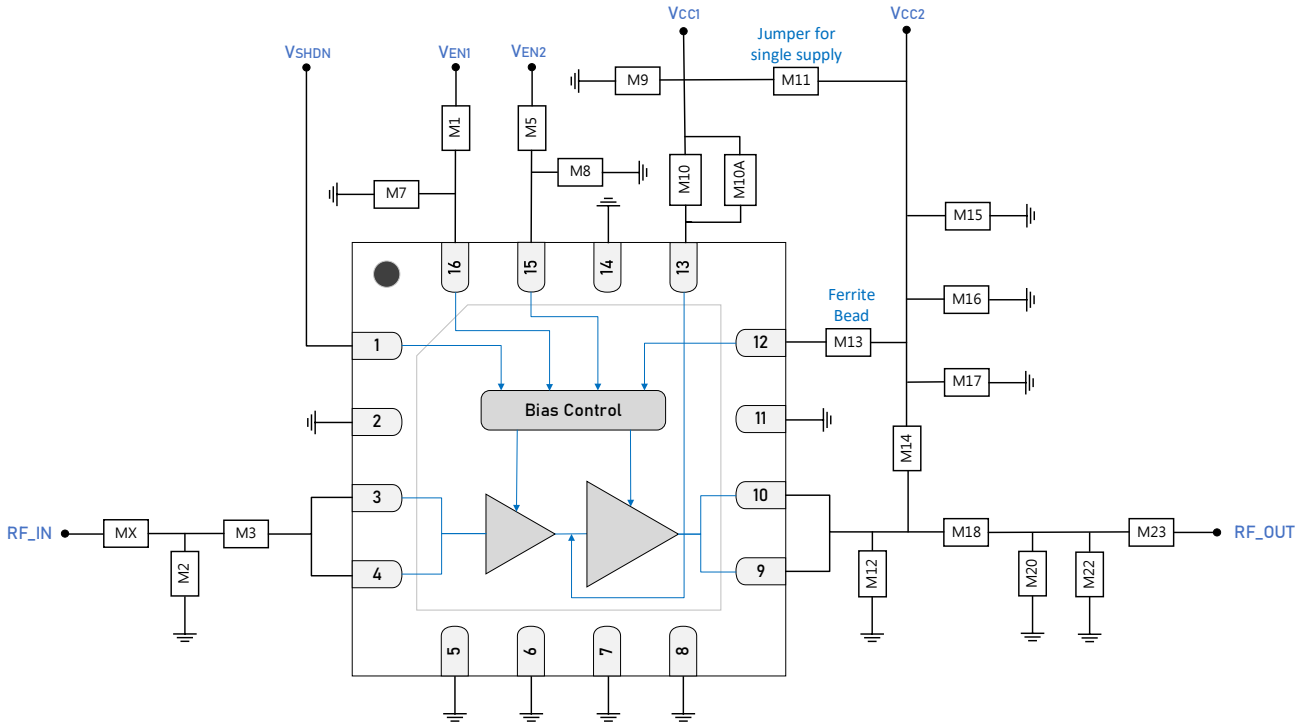
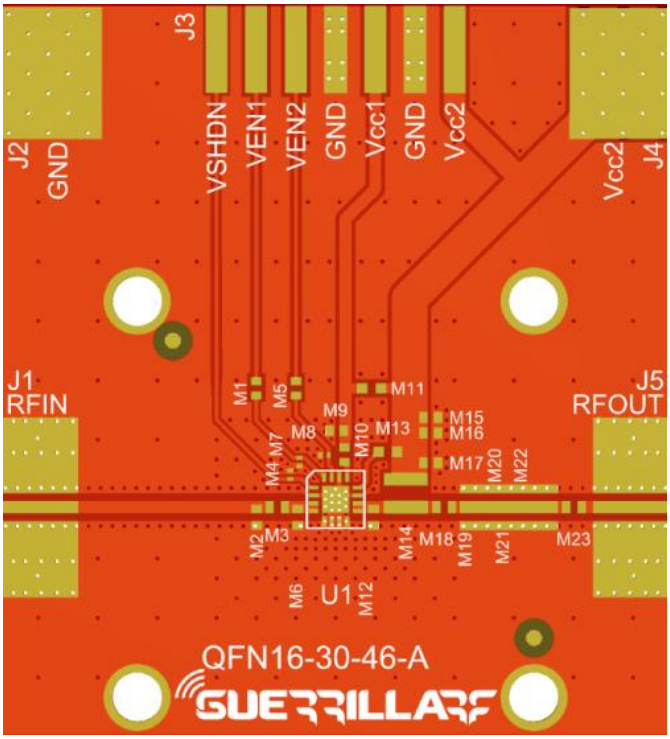


GRF5603 Standard Evaluation Board Schematic



GRF5603 Evaluation Board Assembly Diagram

GRF5603 Evaluation Board Assembly Diagram Reference: 865 to 928 MHz Tune

Component	Type	Manufacturer	Family	Value	Package Size	Substitution
M1, M5	Resistor	Various	1%	6800 Ω	0402	ok
M2	Inductor	Murata	LQG	3.0 nH	0402	ok
M3	Capacitor	Murata	GJM	12 pF	0402	ok
MX	Capacitor	Murata	GJM	47 pF	0402	ok
M4, M6, M19, M21	DNP	--	--	--	--	--
M7	Capacitor	Murata	GJM	22 pF	0402	ok
M8	Capacitor	Murata	GJM	10 pF	0402	ok
M9, M15, M16, M17	Capacitor	Murata	GRM	** 10 µF	0402	ok
M10	Resistor	Various	1%	500 Ω	0402	ok
M10A	Inductor	CoilCraft	0402HP	12 nH	0402	ok
M11	Resistor (jumper)	Various	5%	0 Ω	0402	ok
M12	Capacitor	Murata	GRM	33 pF	0402	ok
M13	Ferrite Bead	Murata	BLM15HG102BH1D	1000 Ω	0402	ok
M14	Inductor	Coilcraft	0908SQ	23 nH	0908	ok
M18	Copper Jumper	Keystone	5113	N/A	0402	ok
M20	Capacitor	Murata	GJM	4.3 pF	0402	ok
M22	Capacitor	Murata	GJM	5.1 pF	0402	ok
M23	Capacitor	Murata	GJM	47 pF	0402	ok
Evaluation Board	QFN16-30-46-A					

Notes:
Standard evaluation board bias: V_{CC} = 5 V, V_{EN1} = V_{EN2} = 5 V, V_{SHDN} = LOW.
** 10 µF must be rated for > 5 V at maximum ambient temperature. Manufacturer Part Number in this case = GRM155C80J106ME11D.

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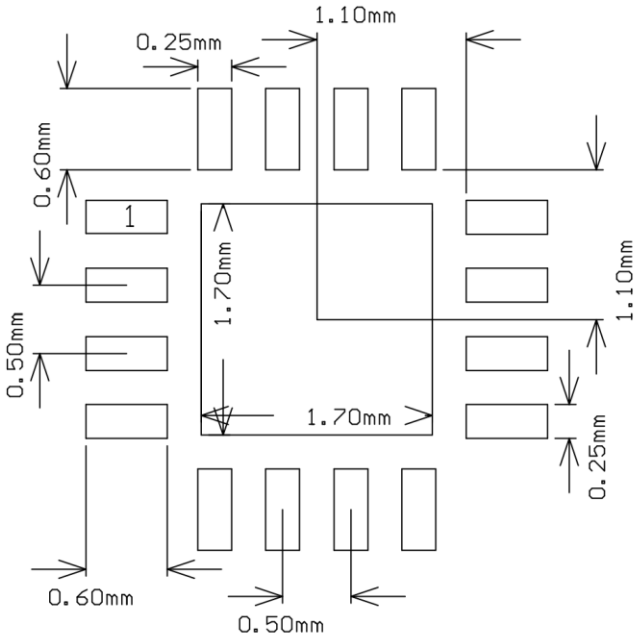
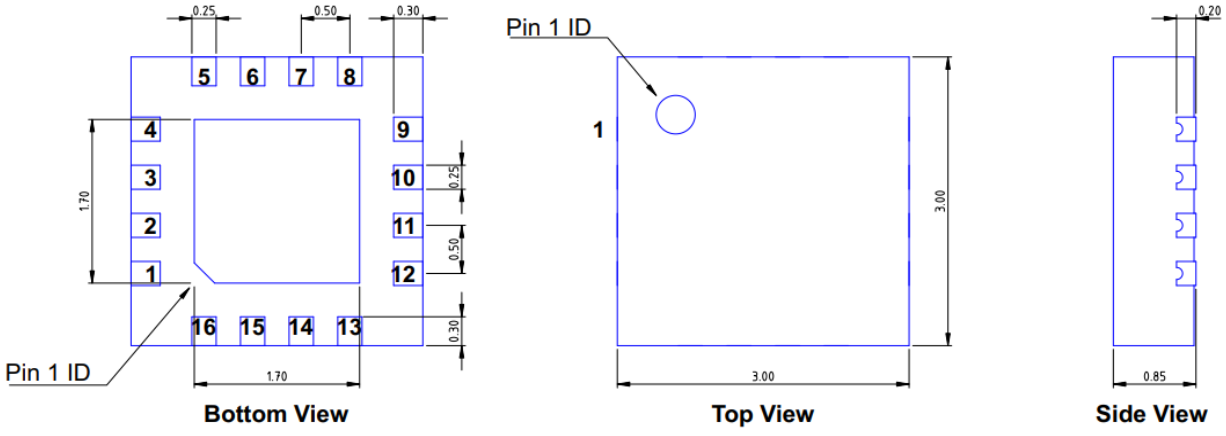


3 x 3 mm QFN-16 Suggested PCB Footprint (Top View)



QFN16 3x3mm
Dimensions in millimeters
Dimensional Tolerance: ±0.05

3 x 3 mm QFN-16 Package Dimensions

Package Marking Diagram

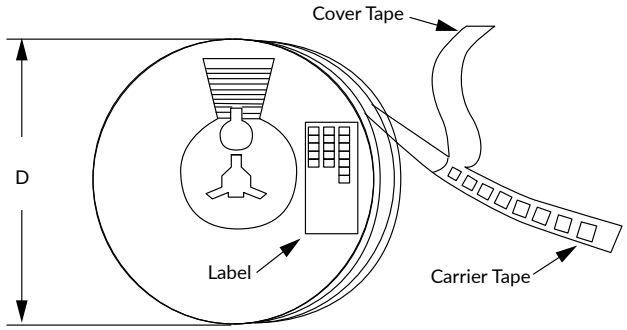
- Line 1: "YY" = YEAR. "WW" = WORK WEEK the device was assembled.
- Line 2: "GRF" = Guerrilla RF.
- Line 3: "XXXX" = Device PART NUMBER.

Tape and Reel Information

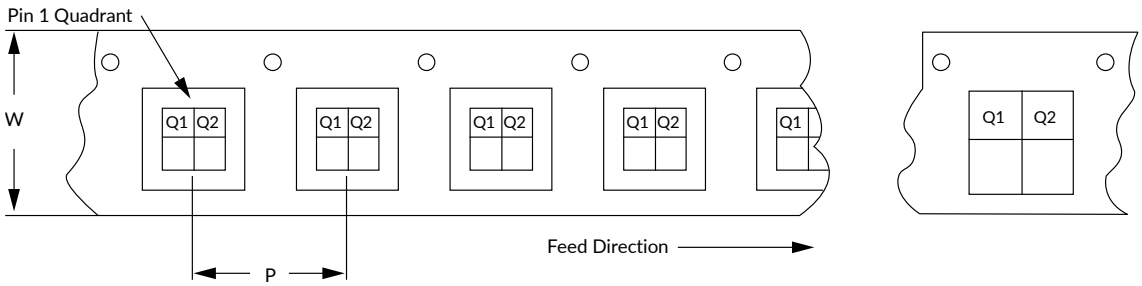
Guerrilla RF's tape and reel specification complies with Electronic Industries Alliance (EIA) standards for "Embossed Carrier Tape of Surface Mount Components for Automatic Handling" (reference EIA-481). See the following page for the Tape and Reel Specification and Device Package Information table, which includes units per reel.

Devices are loaded with pins down into the carrier pocket with protective cover tape and reeled onto a plastic reel. Each reel is packaged in a cardboard box. There are product labels on the reel, the protective ESD bag and the outside surface of the box.

For the Tape and Reel Reference Table, please refer to: *https://www.guerrilla-rf.com/prodFiles/Manufacturing/MN001.pdf*



Tape and Reel Packaging with Reel Diameter Noted (D)



Carrier Tape Width (W), Pitch (P), Feed Direction and Pin 1 Quadrant Information

Revision History

Revision Date	Description of Change
April 15, 2025	Preliminary Data Sheet.
October 2, 2025	Release Ø Data Sheet.

Datasheet Classifications

Data Sheet Status	Notes
Advance	S-parameter and NF data based on EM simulations for the fully packaged device using foundry-supplied transistor S-parameters. Linearity estimates based on device size, bias condition and experience with related devices.
Preliminary	All data based on limited evaluation board measurements taken within the Guerrilla RF Applications Lab. All parametric values are subject to change pending the collection of additional data.
Release Ø	All data based on measurements taken with *production-released* material. TYP values are based on a combination of ATE and bench-level measurements, with MIN/MAX limits defined using *modelled estimates* that account for part-to-part variations and expected process spreads. Although unlikely, future refinements to the TYP/MIN/MAX values may be in order as multiple lots are processed through the factory.
Release A-Z	All data based on measurements taken with production-released material *derived from multiple lots which have been fabricated over an extended period of time.* MIN/MAX limits may be refined over previous releases as more statistically significant data is collected to account for process spreads.