

Ultra-Low Noise, High PSRR, 300 mA Low-Dropout Linear Regulator

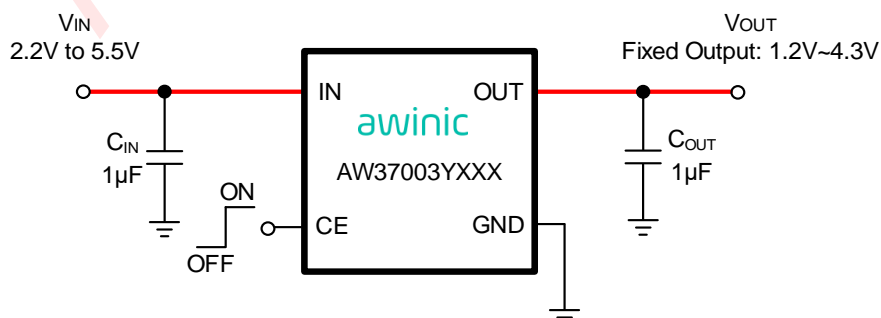
Features

- Input voltage range: 2.2V to 5.5V
- Available in fixed voltage option: 1.2V, 1.8V, 2.2V, 2.25V, 2.8V, 2.85V, 2.9V, 3.0V, 3.3V
- Rated output current: 300mA
- Quiescent current: typical 22 μ A
- Typical 0.1 μ A shutdown current
- Typical 100mV dropout voltage ($I_{OUT}=300mA$, 2.8V output)
- Power supply rejection ratio: typical 92dB ($I_{OUT}=10mA$, freq=1kHz, 2.8V output)
- Noise: typical 15 μ Vrms ($I_{OUT}=50mA$, BW=10Hz to 100kHz, 2.8V output)
- Built-in output short protection: typical 130mA when output short to ground
- DFN 1mmX1mmX0.37mm-4L package and SOT 23-5L package

Applications

Battery-powered equipment
Smart phone
Digital camera
Other portable electronic device

Typical Application Circuit



General Description

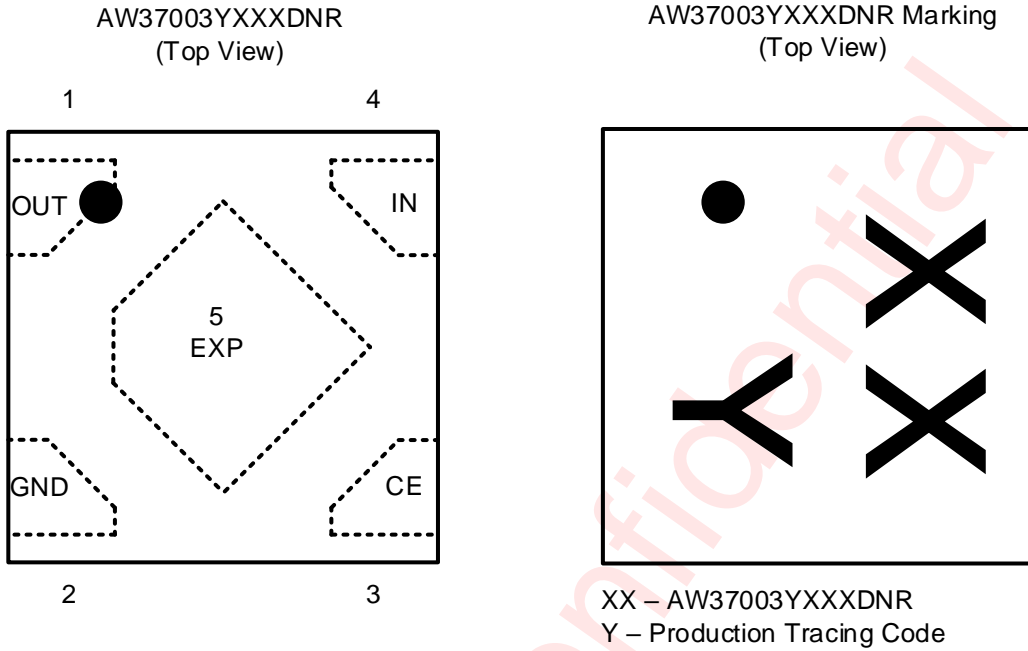
AW37003YXXX is a low dropout voltage regulator featuring low ON resistance, high PSRR, low Noise, good load/line transient response and smooth soft-start.

AW37003YXXX integrates current limit, short circuit protection, thermal shutdown, sufficiently protecting IC from being damaged.

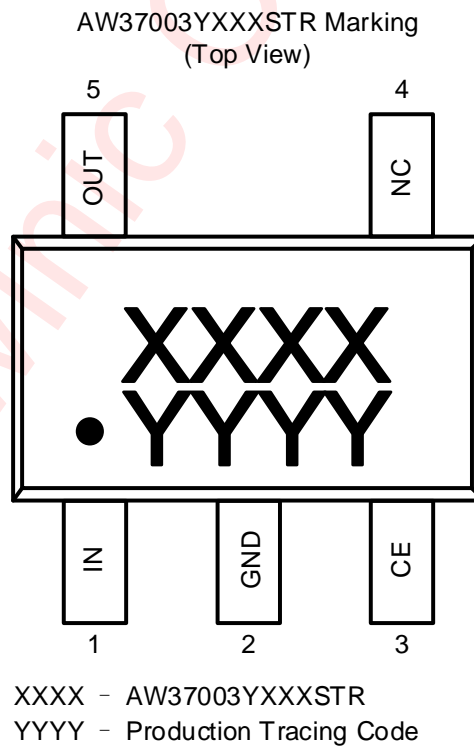
AW37003YXXX is designed to work with a $1\mu F$ or more input ceramic capacitor and a $1\mu F$ or more output ceramic capacitor. The low power dissipation and good dynamic response make AW37003YXXX very suitable for hand-held communication equipment. Tiny package makes high density mounting of the IC on boards possible.

Pin Configuration And Top Mark

DFN 1mmX1mm-4L



SOT 23-5L



Pin Definition

DFN 1mmX1mm-4L

No.	NAME	DESCRIPTION
1	OUT	Regulated output voltage pin. Put a 1 μ F or more ceramic capacitor at the output pin.
2	GND	Ground.
3	CE	Chip enable pin. Built-in 420nA pull-down current. (High Active)
4	IN	Input supply pin. Put a 1 μ F or more bypass capacitor at the power supply.
5	EXP	Expose pad should be tied to ground plane for better power dissipation.

SOT 23-5L

No.	NAME	DESCRIPTION
1	IN	Input supply pin. Put a 1 μ F or more bypass capacitor at the power supply.
2	GND	Ground.
3	CE	Chip enable pin. Built-in 420nA pull-down current. (High Active)
4	NC	Not connected.
5	OUT	Regulated output voltage pin. Put a 1 μ F or more ceramic capacitor at the output pin.

Name Rule

AW37 003 Y XXX ZZZ

Package

DNR: DFN 1mmX1mmX0.37mm-4L
STR: SOT 23-5L

Output Voltage

E.g.
180: Output Voltage 1.8V

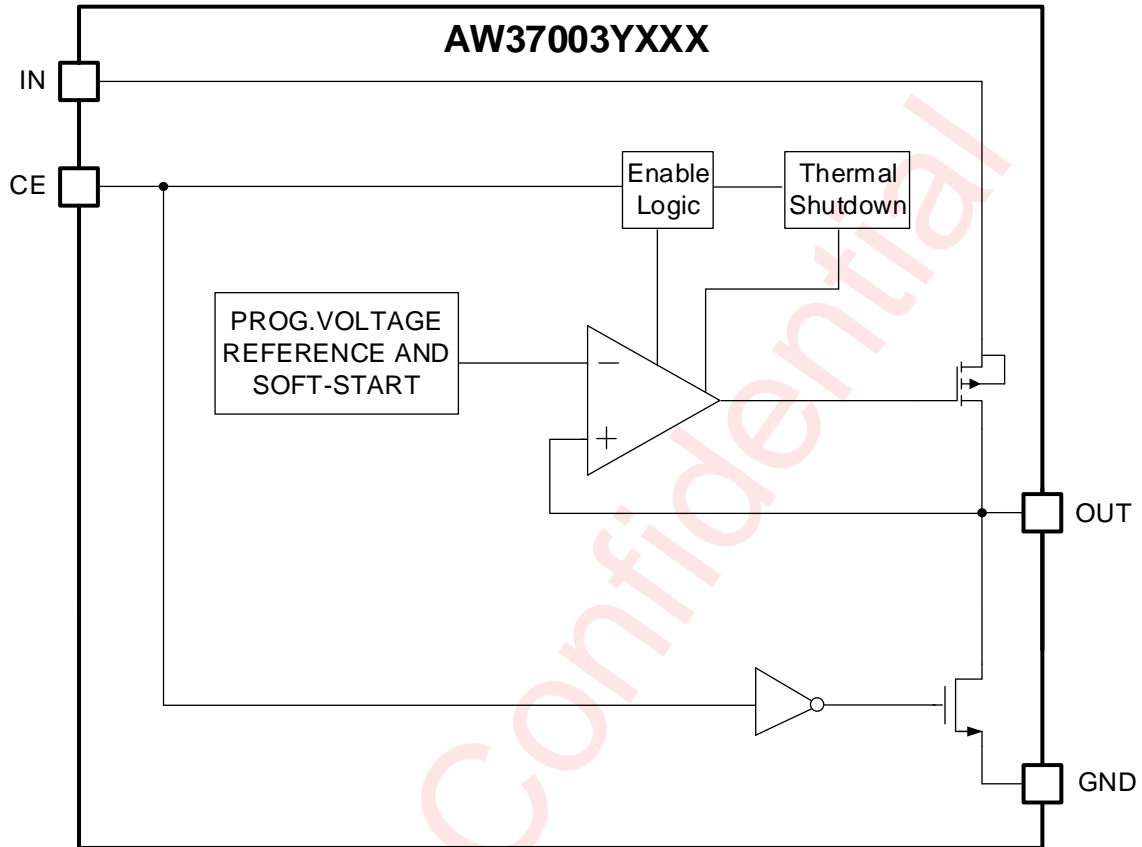
Auto-discharge Function

D: Available
B: Not available

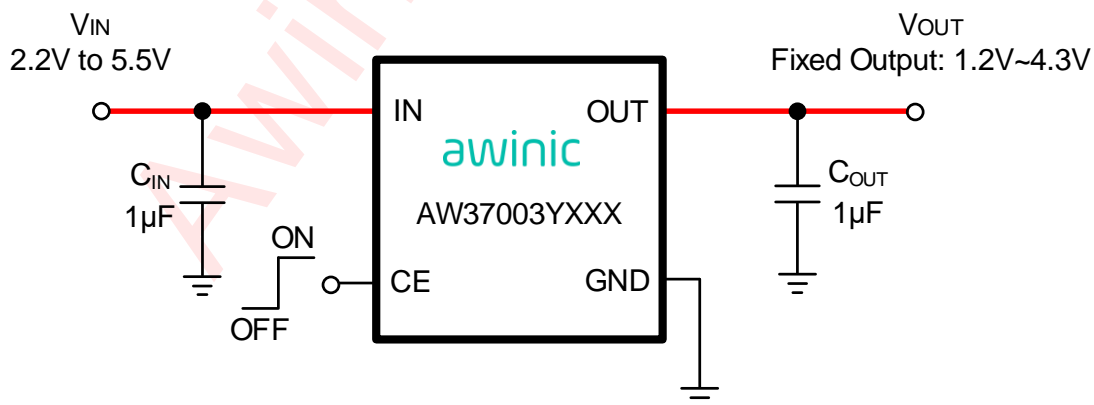
Rated Current

003: Rated Current 300mA

Functional Block Diagram



Typical Application Circuit



AW37003YXXX Application Circuit

Notice for typical application circuits:

Capacitance of C_{IN} and C_{OUT} should be 1 μ F or more.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW37003D120DNR	-40°C~85°C	DFN 1mmX1mm-4L	1U	MSL1	ROHS+HF	9000 units/ Tape and Reel
AW37003D180DNR	-40°C~85°C	DFN 1mmX1mm-4L	CS	MSL1	ROHS+HF	9000 units/ Tape and Reel
AW37003D220DNR	-40°C~85°C	DFN 1mmX1mm-4L	PC	MSL1	ROHS+HF	9000 units/ Tape and Reel
AW37003D225DNR	-40°C~85°C	DFN 1mmX1mm-4L	JG	MSL1	ROHS+HF	9000 units/ Tape and Reel
AW37003D280DNR	-40°C~85°C	DFN 1mmX1mm-4L	32	MSL1	ROHS+HF	9000 units/ Tape and Reel
AW37003D285DNR	-40°C~85°C	DFN 1mmX1mm-4L	Q8	MSL1	ROHS+HF	9000 units/ Tape and Reel
AW37003D290DNR	-40°C~85°C	DFN 1mmX1mm-4L	N7	MSL1	ROHS+HF	9000 units/ Tape and Reel
AW37003D300DNR	-40°C~85°C	DFN 1mmX1mm-4L	2N	MSL1	ROHS+HF	9000 units/ Tape and Reel
AW37003D330DNR	-40°C~85°C	DFN 1mmX1mm-4L	2S	MSL1	ROHS+HF	9000 units/ Tape and Reel
AW37003D120STR	-40°C~85°C	SOT 23-5L	YG68	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37003D180STR	-40°C~85°C	SOT 23-5L	9ND2	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37003D280STR	-40°C~85°C	SOT 23-5L	D999	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37003D300STR	-40°C~85°C	SOT 23-5L	3MR1	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37003D330STR	-40°C~85°C	SOT 23-5L	2R3W	MSL3	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings^(NOTE1)

PARAMETERS		RANGE
Input voltage range		-0.3V to 6.5V
Enable control voltage range		-0.3V to 6.5V
Output voltage range		-0.3V to VIN+0.3V, max. 6.5V
Maximum operating junction temperature T _{J_MAX}		150°C
Recommended operating junction temperature T _{J_REC}		-40°C to 125°C
Operating free-air temperature range		-40°C to 85°C
Storage temperature T _{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
Junction-to-ambient thermal resistance R _{θJA} ^(NOTE2)	DFN 1mmX1mm-4L	215.4°C/W
	SOT 23-5L	177.4°C/W
ESD	HBM (Human body model) ^(NOTE3)	±2kV
	CDM(Charged device model) ^(NOTE4)	±1.5kV
Latch-Up ^(NOTE5)		+IT: 200mA - IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Thermal resistances follow JEDEC 2S2P standards, and is usually highly dependent on PCB layout. Exceptionally, R_{θJC(top)} of DFN 1mmX1mm-4L Package follows SEMI standard G43-87.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS-001-2017.

NOTE4: All pins. Test Condition: ESDA/JEDEC JS-002-2018.

NOTE5: Test Condition: JESD78F.

Electrical Characteristics

$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25^\circ C$ (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range			2.2		5.5	V
V_{OUT_ACC}	Output Voltage Accuracy	DFN 1mmX1mm- 4L	$T_A=25^\circ C$	-1		1	%
			$-40^\circ C \leq T_A \leq 85^\circ C^{(1)}$	-2		2	
		SOT23-5L	$T_A=25^\circ C$	-1.5		1.5	
			$-40^\circ C \leq T_A \leq 85^\circ C^{(1)}$	-2.5		2.5	
V_{OUT}	Output Voltage Range			1.2		4.3	V
$LOAD_{Reg}$	Load Regulation	$1mA \leq I_{OUT} \leq 300mA$			1	10	mV
$LINE_{Reg}$	Line Regulation	$V_{OUT(SET)}+0.5V \leq V_{IN} \leq 5.5V$			0.1		mV
$V_{dropout}$	Dropout Voltage	$I_{OUT}=300mA$, When V_{OUT} falls 100mV below $V_{OUT(SET)}$, - $40^\circ C$ $\leq T_A \leq 85^\circ C$	$V_{OUT(SET)}=1.8V$		170	225	mV
			$V_{OUT(SET)}=2.8V$		100	167	
			$V_{OUT(SET)}=3.3V$		86	168	
I_{SD}	Shutdown Current	$V_{CE}<0.4V$			0.1	1	μA
I_Q	Quiescent Current	$I_{OUT}=0mA$			22		μA
V_{CEH}	CE Input Voltage "H"	$-40^\circ C \leq T_A \leq 85^\circ C$		0.84			V
V_{CEL}	CE Input Voltage "L"	$-40^\circ C \leq T_A \leq 85^\circ C$				0.36	V
PSRR	Power Supply Ripple Rejection	$I_{OUT}=10mA$, $V_{OUT(SET)}=2.8$ V	$f=1kHz$		92		dB
			$f=10kHz$		85		
			$f=100kHz$		60		
			$f=1MHz$		42		
V_N	Output Voltage Noise	$I_{OUT}=50mA$ BW=10Hz to 100kHz	$V_{OUT(SET)}=1.8V$		12		μV_{rms}
			$V_{OUT(SET)}=2.8V$		15		
			$V_{OUT(SET)}=3.3V$		20		
I_{CL}	Output Current Limit	$V_{OUT}=90\%*V_{OUT(SET)}$		300			mA
I_{SC}	Short Current Limit	$V_{OUT}<10\%*V_{OUT(SET)}$			130		mA
R_{DISC}	Auto Discharge Resistance	$V_{CE}<0.36V$			200		Ω
I_{CE}	CE Pull Down Current	$V_{CE}=5V$			420		nA
T_{SDH}	Thermal Shutdown Threshold	Temperature Rising			160		$^\circ C$

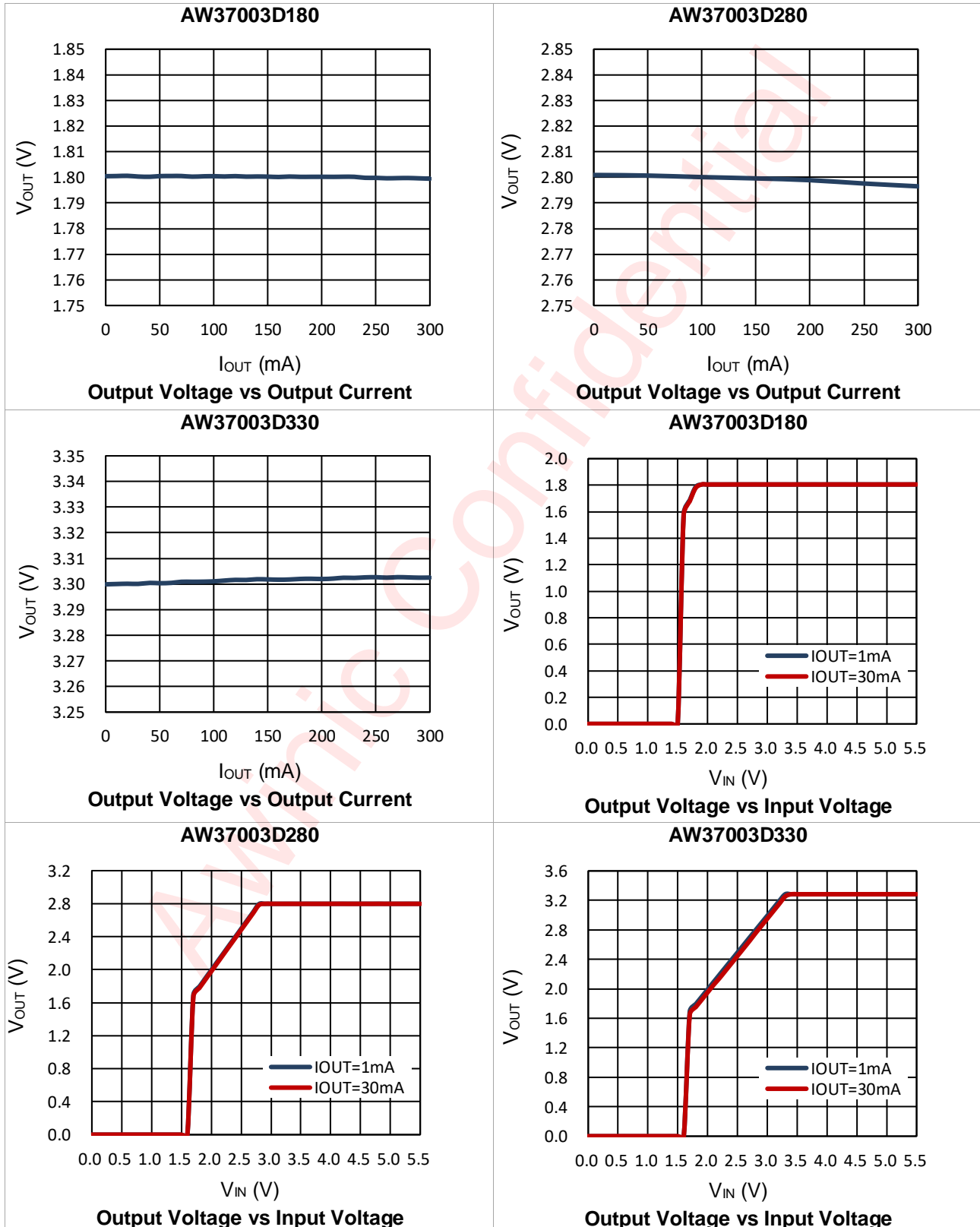
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
T _{SDL}	Thermal Shutdown Reset Threshold	Temperature Falling		135		°C

Note1: Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

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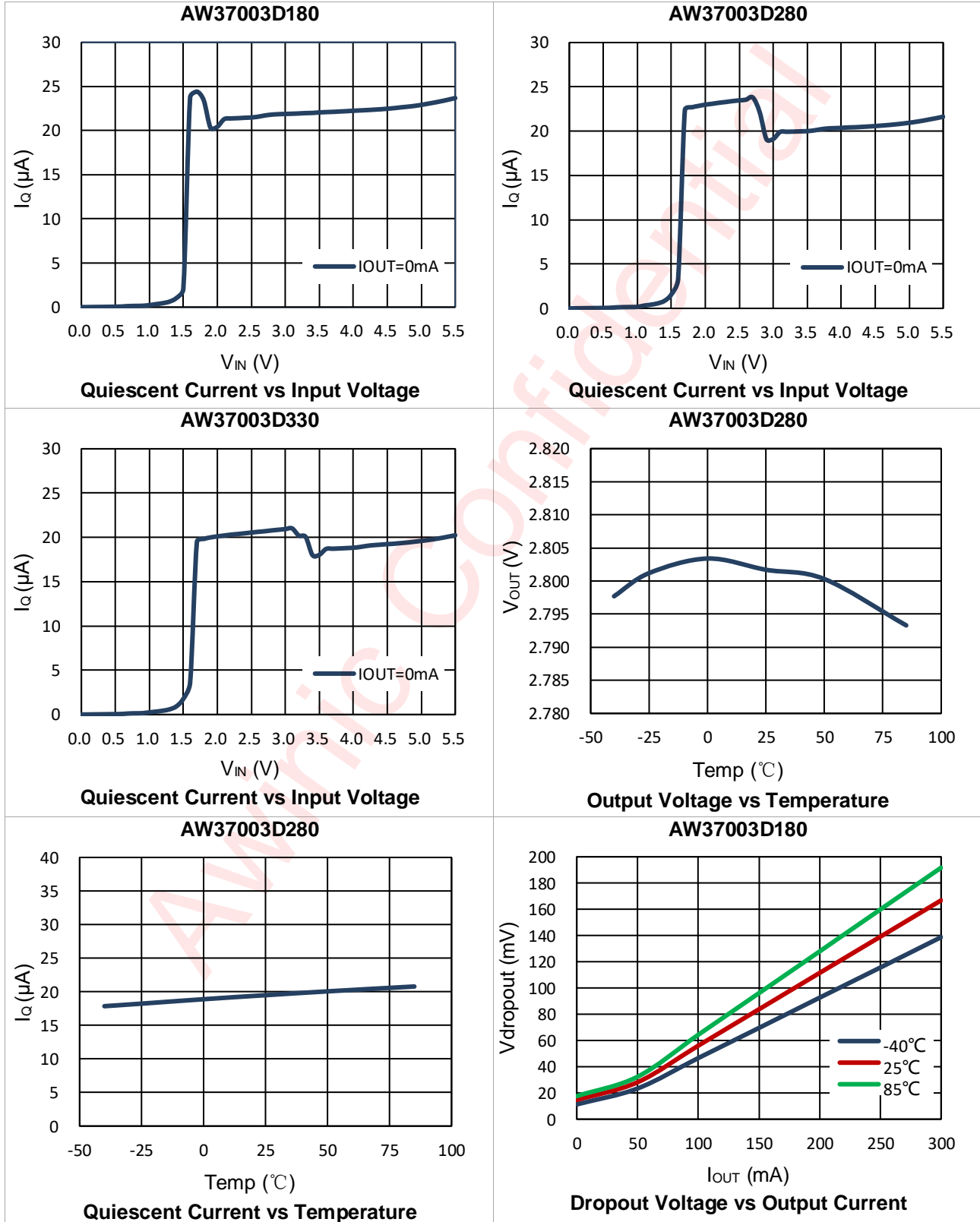
Typical Characteristics

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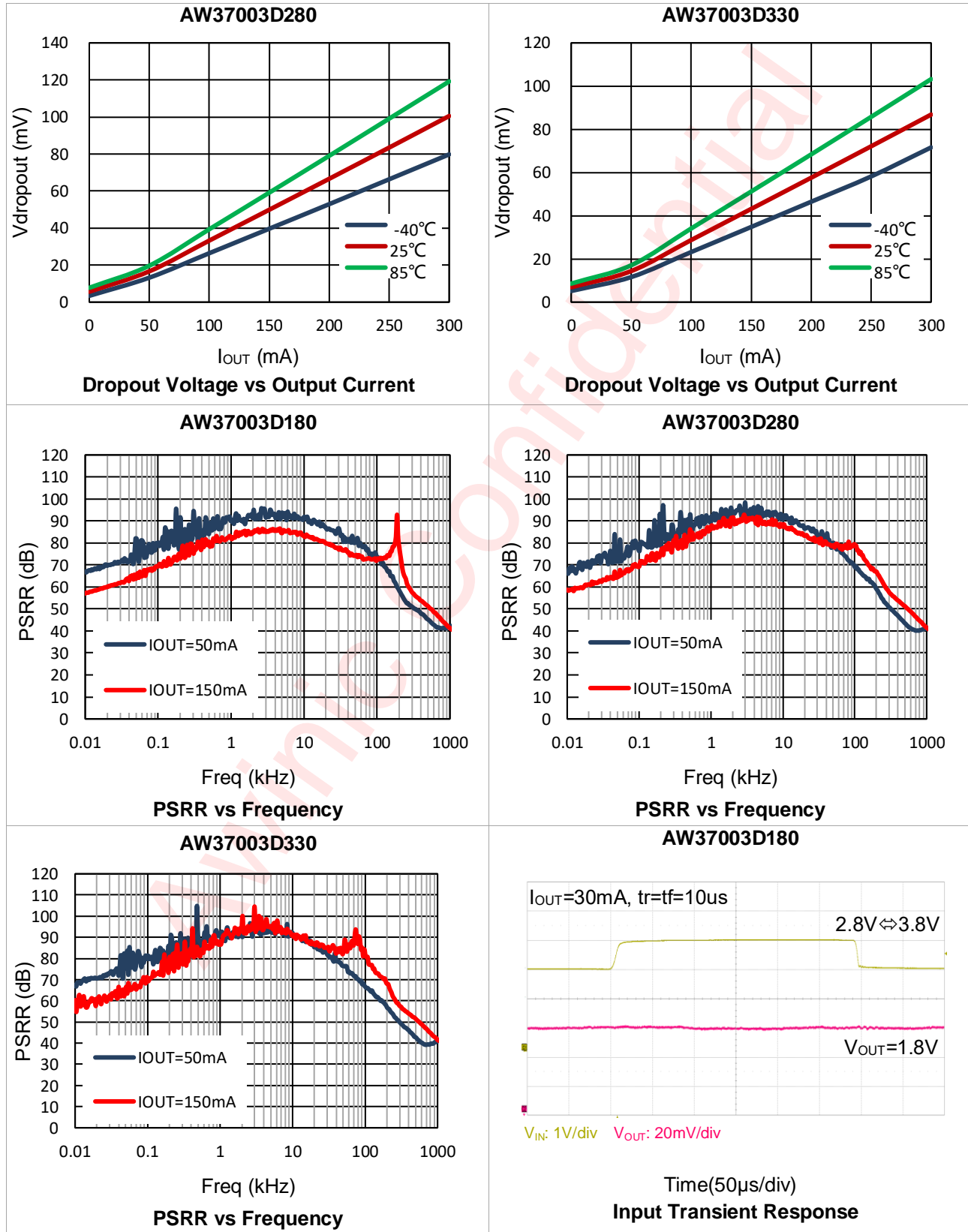
Typical Characteristics (Continued)

$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25^\circ C$, In Typical Application Circuit, unless otherwise noted.



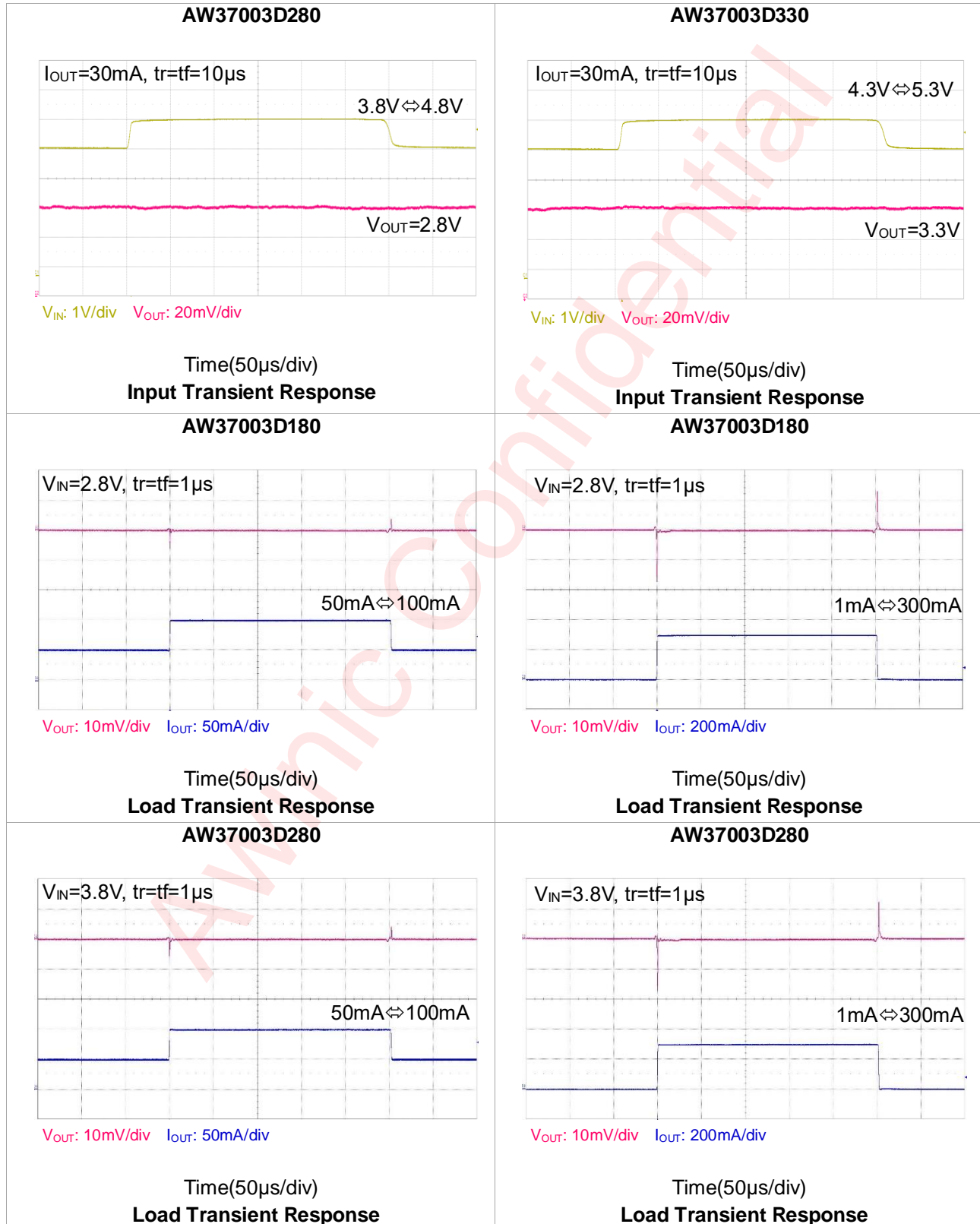
Typical Characteristics (Continued)

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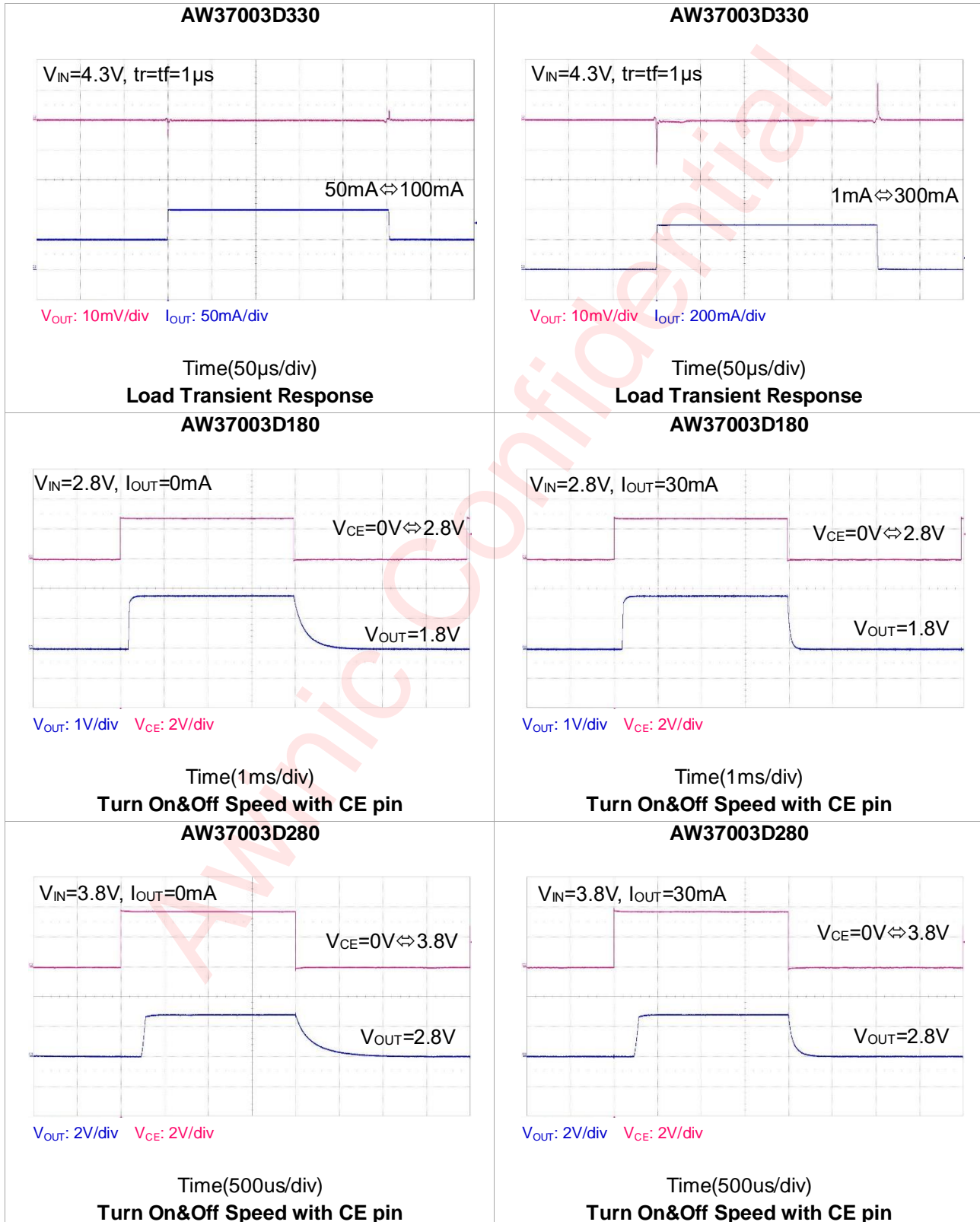
Typical Characteristics (Continued)

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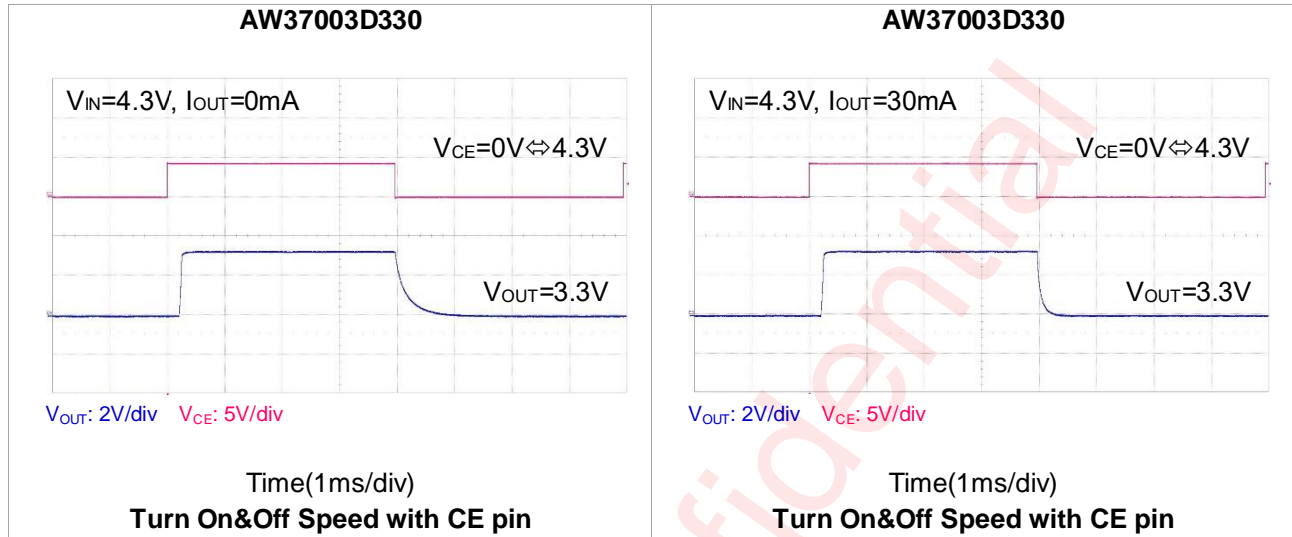
Typical Characteristics (Continued)

$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25^\circ C$, In Typical Application Circuit, unless otherwise noted.



Typical Characteristics (Continued)

$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25^\circ C$, In Typical Application Circuit, unless otherwise noted.



Detailed Functional Description

AW37003YXXX is a low dropout voltage regulator. After powered on, with CE pin assertion, feedback voltage signal from the integrated resistor network and a voltage related to the voltage reference are transmit to positive input terminal and negative input terminal of an error amplifier (EA) respectively. The output signal of EA is used to control the open-state of power MOSFET. After soft-start, feedback voltage signal compares with the established reference voltage, making output voltage stable and accurate. AW37003YXXX integrates function of load transient accelerating, making LDO obtain excellent dynamic load transient response performance.

Enable Operation

AW37003YXXX uses CE pin to realize enable operation. Applying proper value of voltage to CE pin can make IC enable/disable.

If the voltage of CE pin is less than 0.36V, AW37003YXXX is guaranteed to be disabled. In this state, function modules of IC and power MOSFET are turned off. And the auto discharge function is enabled making output discharge through a on-state NMOSFET to Ground. In disable state, AW37003YXXX only consumes a typical 100nA current.

If the voltage of CE pin is more than 0.84V, AW37003YXXX is guaranteed to be enabled. In this state, the auto discharge function is disabled, and AW37003YXXX regulates output voltage to the designed value of voltage. A 420nA pull down current to Ground is built-in at CE pin, making sure that the IC is disabled when CE pin floats. If Enable function is not required, CE pin should be connected directly to IN pin.

Output Current Limit

AW37003YXXX integrates output current limit function, protecting IC from excessive current.

When the load is excessively heavy, AW37003YXXX limits the current flowing through the IC to a typical 480mA current. This value is specially designed, so that IC is protected properly and the output capability of 300mA is not influenced either.

Meanwhile, AW37003YXXX integrates a 130mA fold-back current limit function, lowering the system dissipation when output overload or short to Ground.

Thermal Shutdown

AW37003YXXX integrates thermal shutdown function, protect IC from excessively high temperature.

When the chip temperature exceeds 160°C, AW37003YXXX detects it as an over-temperature event, triggering thermal shutdown, which will turn off the main function module, including power MOSFET. This inhibits increase of chip's temperature. IC would keep the protection-state on until the chip's temperature falls below to 135°C. At this moment, the over-temperature protection-state is released, IC resumes to work again. The hysteresis avoids IC's turning off and on frequently around the the Thermal Shutdown threshold.

Auto Discharge

AW37003YXXX makes output voltage discharge quickly when in CE disable state or thermal shutdown state, benefit from integrating auto discharge function. Auto discharge function is implemented by integrated a NMOSFET of typical 200Ω R_{dson} route from Output to Ground, and the route is get through in CE disable state or thermal shutdown state. This feature prevents residual charge voltage on the output capacitor, which may impact proper power up of the system connected to the converter. It should be noted that auto discharge function is optional according to different specs.

Application Information

Power Dissipation and Device Operation

The permissible power dissipation is dependent on the ambient temperature T_A and the junction-to-ambient thermal resistance $R_{\theta JA}$.

The absolute maximum allowable power dissipation for the device in a given package can be calculated using Equation below, where $T_{J_MAX} = 150^\circ\text{C}$:

$$PD_{MAX_ABS} = (T_{J_MAX} - T_A) / R_{\theta JA}$$

The recommended maximum allowable power dissipation for the device in a given package can be calculated using Equation below, where $T_{J_REC} = 125^\circ\text{C}$:

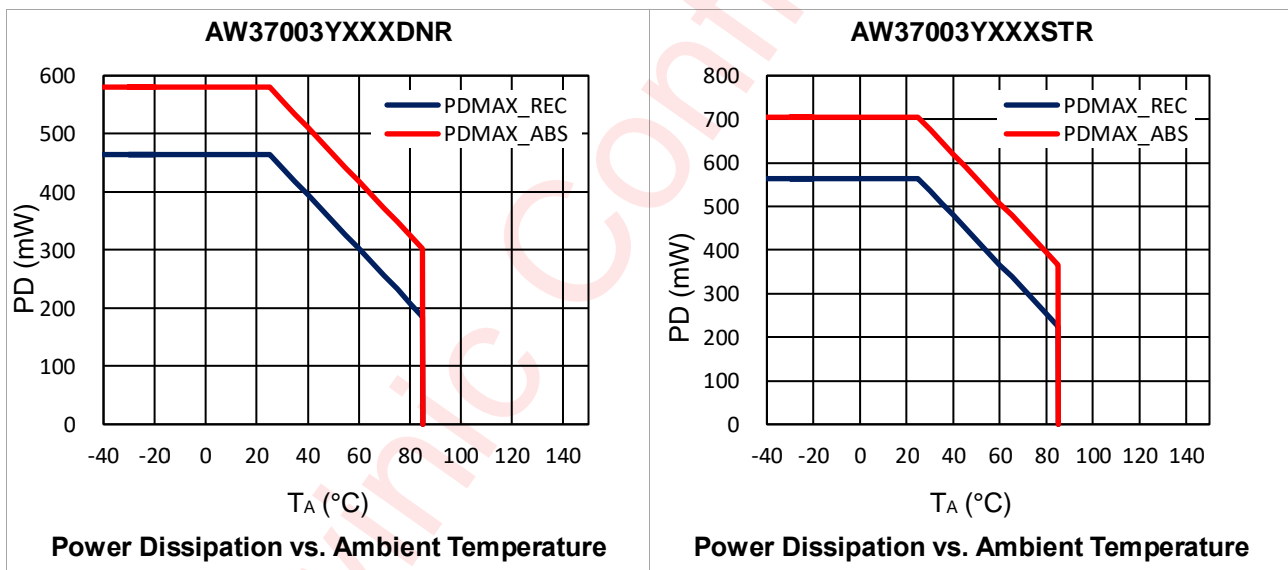
$$PD_{MAX_REC} = (T_{J_REC} - T_A) / R_{\theta JA}$$

The actual power being dissipated in the device can be represented by Equation below:

$$PD_{ACT} = (V_{IN} - V_{OUT}) \times I_{OUT}$$

These equations above establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device.

The graphs of Power Dissipation vs. Ambient Temperature are showed below :



The above graphs show the maximum power dissipation of the respective package at $T_{J_REC} = 125^\circ\text{C}$ and $T_{J_MAX} = 150^\circ\text{C}$. Operating the device in the region between PD_{MAX_REC} and PD_{MAX_ABS} might have a negative influence on its lifetime.

Capacitors Selection

IN pin: Input Capacitor C_{IN}

AW37003YXXX advises to use a $1\mu\text{F}$ or more X5R or X7R ceramic capacitor at IN pin as shown in Typical Application Circuit.

OUT pin: Output Capacitor C_{OUT}

AW37003YXXX advises to use a $1\mu\text{F}$ or more X5R or X7R ceramic capacitor at OUT pin as shown in Typical Application Circuit.

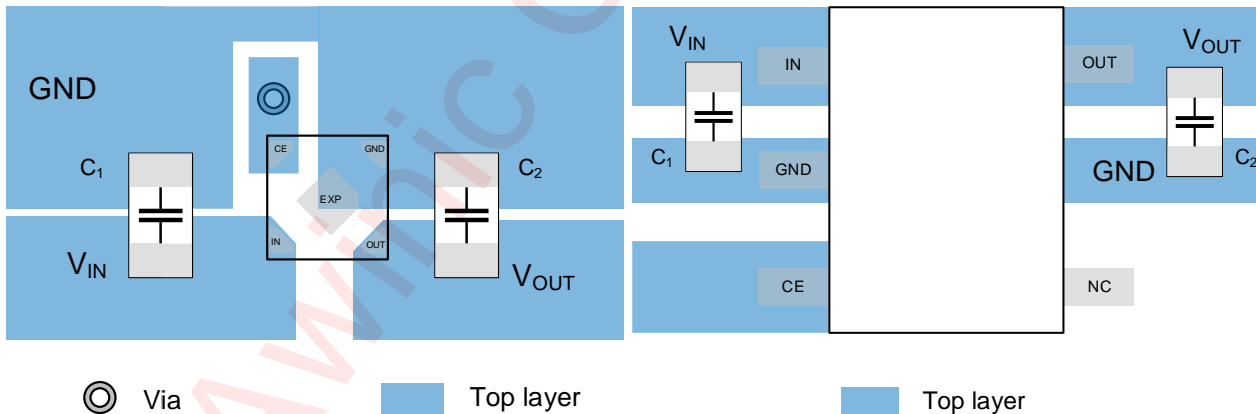
Recommended Components List

Component	PART No.	DESCRIPTION	MFR	TYP.	UNIT
C _{IN}	GRM155R61A105KE15	10V, X5R, 0402	MURATA	1	μF
C _{OUT}	GRM155R61A105KE15	10V, X5R, 0402	MURATA	1	μF

PCB Layout Consideration

The performance of a power source circuit using this device is highly dependent on a peripheral circuit. To obtain the optimal performance, a peripheral component or the device mounted on PCB should not exceed its rated voltage, rated current or rated power. When designing a peripheral circuit, guidelines below for PCB layout of AW37003YXXX should be obeyed:

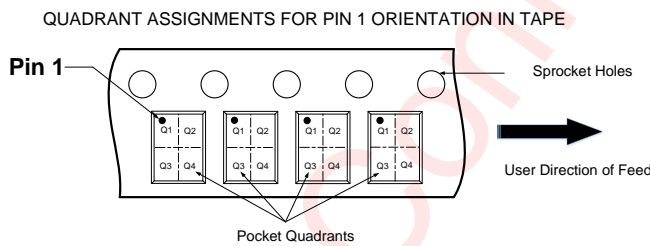
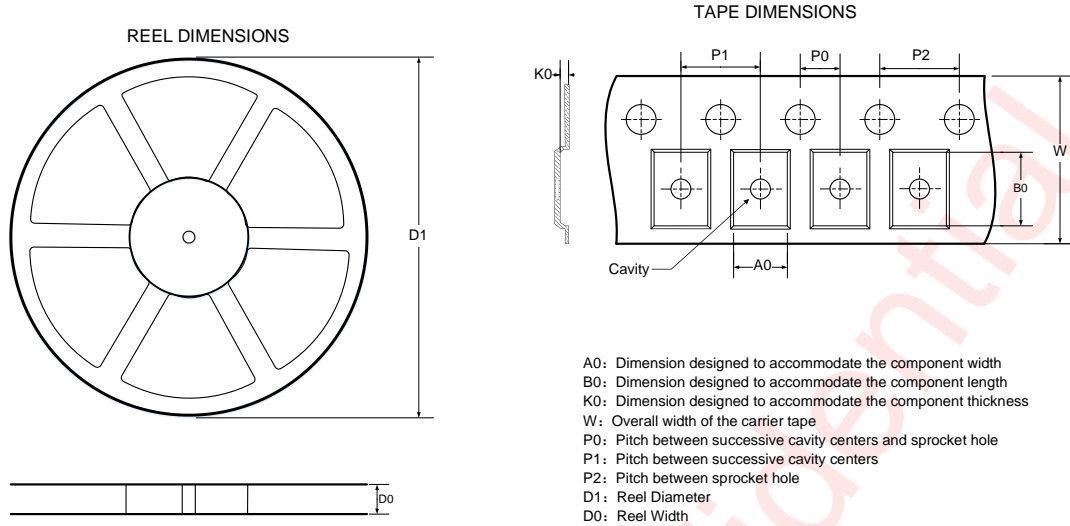
1. All peripheral components should be placed as close to the chip as possible. C_{IN} and C_{OUT} should be close to IN and OUT pins respectively. Avoid connecting device and chip pins with two different layers of copper, use the same layer of copper instead.
2. IN and OUT pin are the large current input and output of the chip, make IN, OUT, and meanwhile GND lines sufficient.
3. The connection lines between the planes of C_{IN} or C_{OUT} and respective chip pin should be as short and wide as possible, to reduce noise and EMI interference, or it may cause noise pickup or unstable operation.
4. The exposed plane of chip and GND pins must be connected to the large-area ground layer of PCB directly, meanwhile place sufficient vias below the exposed plane. Thus we can decrease the thermal resistor on the board to optimize heat-diffusion performance.



AW37003YXXX PCB LAYOUT

Tape And Reel Information

DFN 1mmX1mm-4L



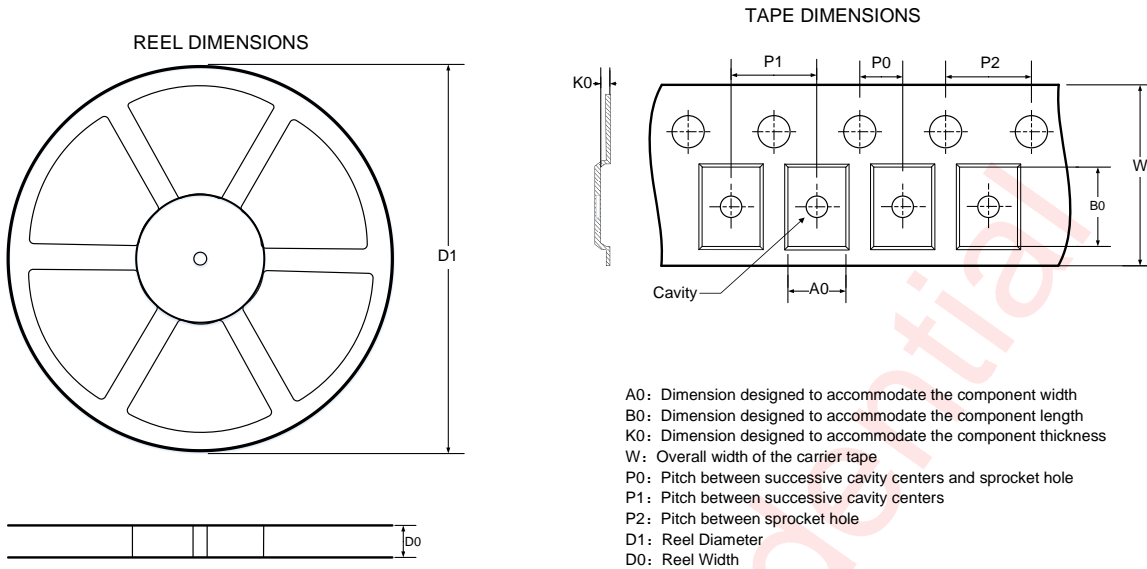
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

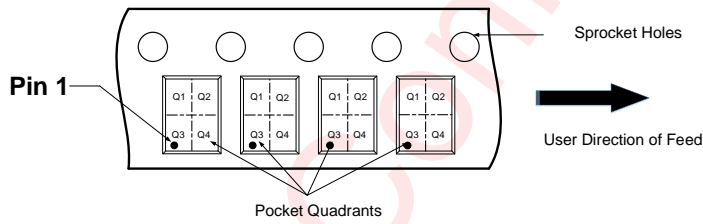
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178.00	8.40	1.16	1.16	0.50	2.00	2.00	4.00	8.00	Q1

All dimensions are nominal

SOT 23-5L



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

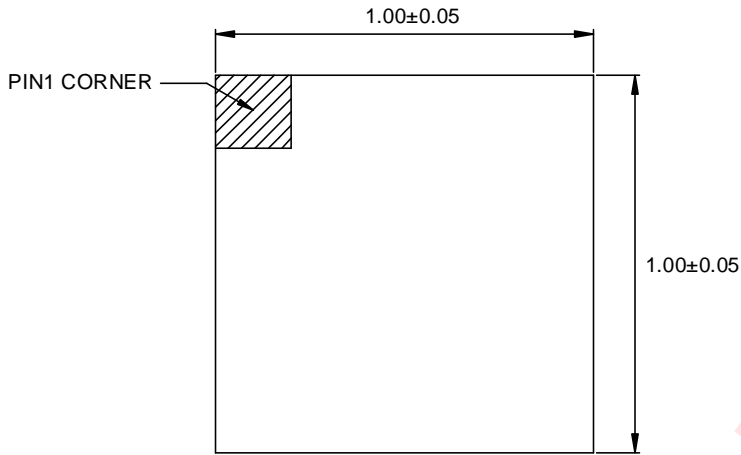
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178.00	8.40	3.30	3.20	1.40	2.00	4.00	4.00	8.00	Q3

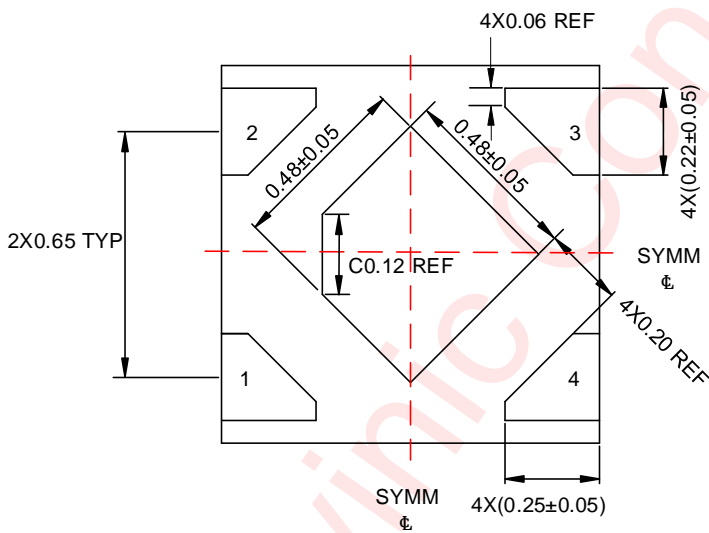
All dimensions are nominal

Package Description

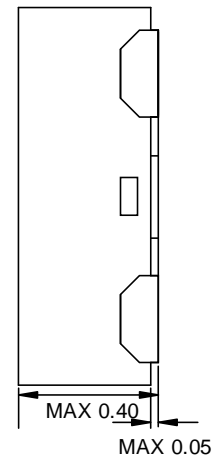
DFN 1mmX1mm-4L



Top View



Bottom View

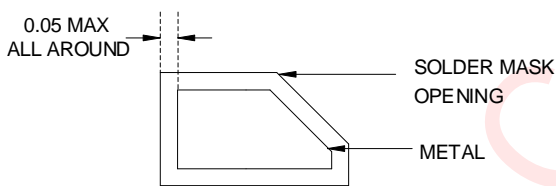
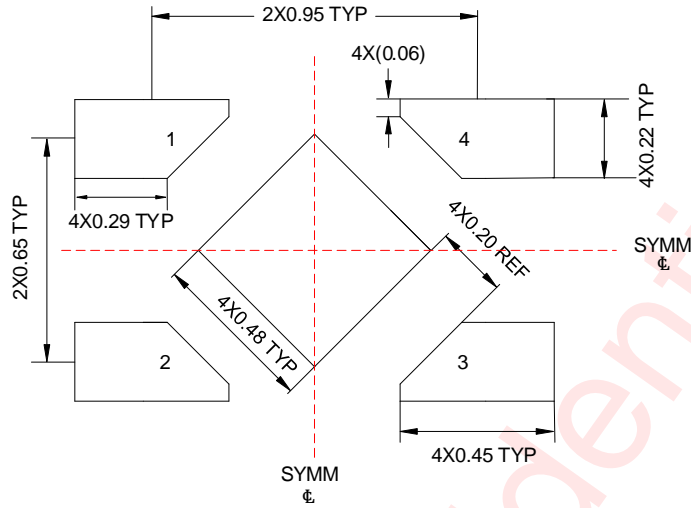


Side View

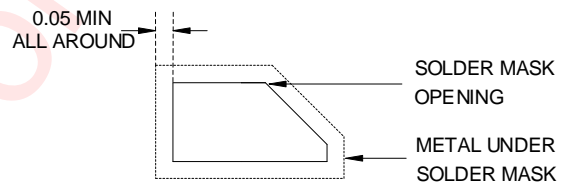
Unit:mm

Land Pattern Data

DFN 1mmX1mm-4L



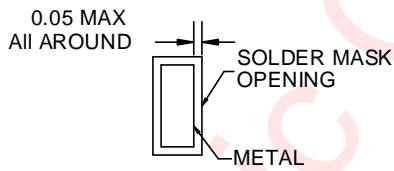
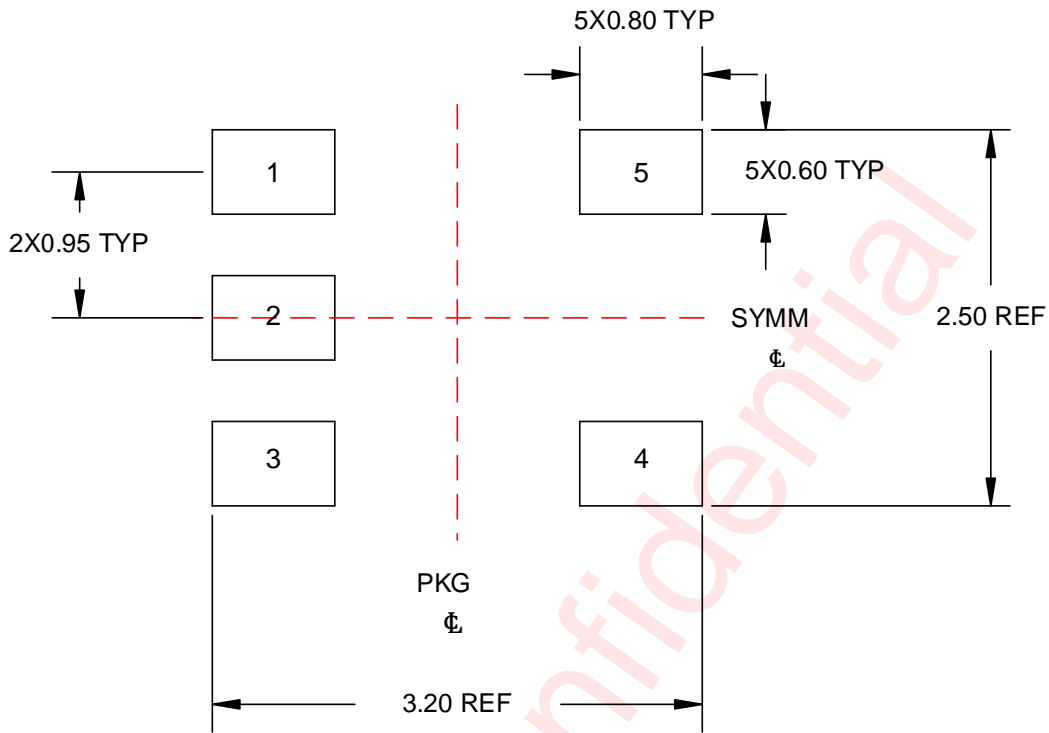
NON SOLDER MASK DEFINED



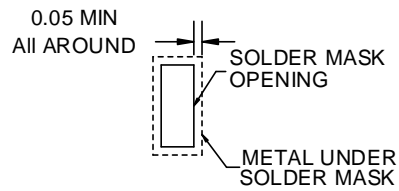
SOLDER MASK DEFINED

UNIT : mm

SOT 23-5L



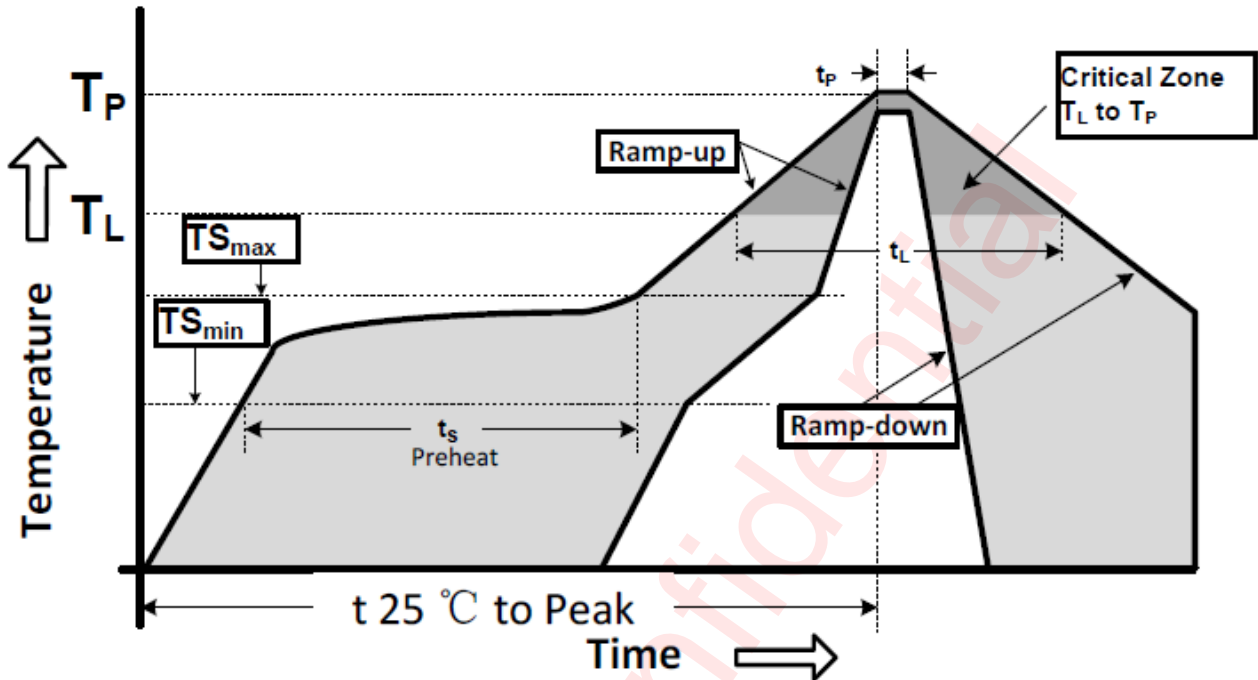
NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Reflow



Reflow Note	Spec
Ramp-up rate ($T_{S_{max}}$ to T_P)	3°C/second max.
Preheat temperature ($T_{S_{min}}$ to $T_{S_{max}}$)	150°C to 200°C
Preheat time (t_s)	60 - 180 seconds
Time above T_L , 217°C (t_L)	60 - 150 seconds
Peak temperature (T_P)	260°C
Time within 5°C of peak temperature(t_p)	20 - 40 seconds
Ramp-down rate	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

Revision History

Version	Date	Change Record
V1.0	Mar. 2023	Officially released
V1.1	Apr.2023	Add V _{OUT} of 2.2V and 2.85V(P1 P5)
V1.2	Jun. 2023	Update PSRR parameters(P1 P7 P10)
V1.3	Feb.2024	Update Output Voltage Accuracy(P7)
V1.4	May 2024	Add V _{OUT} of 2.25V and 2.9V(P1 P5), Update Dropout Voltage(P7)
V1.5	Mar.2025	Add Note1 to the Electrical Characteristics(P8);Update Typical Characteristics(P12 P13); Update the format of the Package Description(P20)

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