钍地半导体
Tudi Semiconductor

Product Specification

TUDI-DS2431

1024-Bit, 1-Wire EEPROM

网址 www.sztdbdt.com

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semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Benefits and Features

● Easily Add Traceability and Relevant Information to Any Individual System
●1024 Bits of EEPROM Memory Partitioned Into Four Pages of 256 Bits
● Individual Memory Pages Can Be Permanently Write Protected or Put in EPROM-Emulation Mode (Write to 0)
● Switchpoint Hysteresis and Filtering to Optimize Performance in the Presence of Noise
● Minimalist 1-Wire Interface Lowers Cost and Interface Complexity
● IEC 1000-4-2 Level 4 ESD Protection (±8kV Contact, ±15kV Air, typ)
● Reads and Writes Over a Wide Voltage Range from 2.8V to 5.25V from -40 ° C to +85 ° C
●Communicates to Host with a Single Digital Signal at 15.4kbps or 125kbps

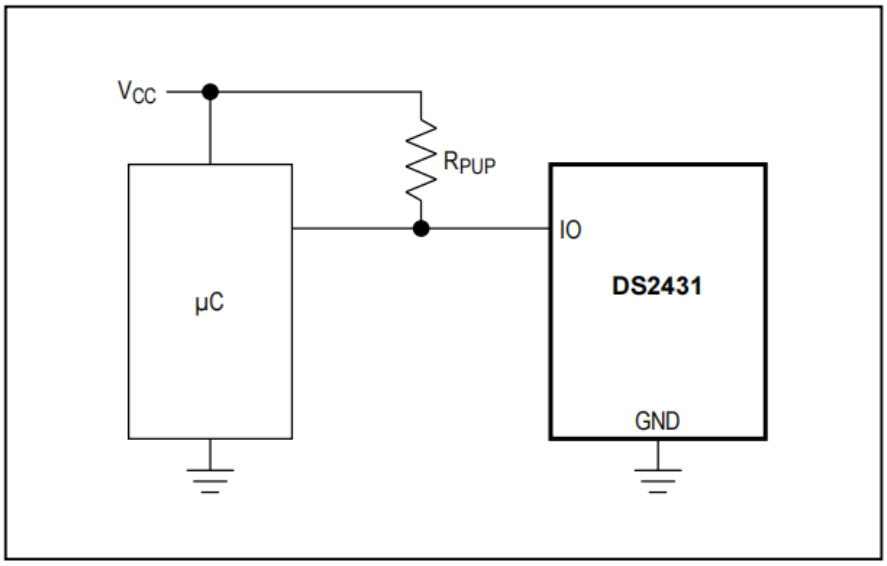
Applications

● Accessory/PCB Identification
● Medical Sensor Calibration Data Storage
● Analog Sensor Calibration Including IEEE P1451.4 Smart Sensors
● Ink and Toner Print Cartridge Identification
● After-Market Management of Consumables

General Description

The DS2431 is a 1024-bit, 1-Wire®EEPROM chip orga-nized as four memory pages of 256 bits each. Data is written to an 8-byte scratchpad, verified, and then copied to the EEPROM memory. As a special feature, the four memory pages can individually be write protected or put in EPROM-emulation mode, where bits can only be changed from a 1 to a 0 state. The DS2431 communi-cates over the single-conductor 1-Wire bus. The com-munication follows the standard 1-Wire protocol. Each device has its own unalterable and unique 64-bit ROM registration number that is factory lasered into the chip. The registration number is used to address the device in a multidrop, 1-Wire net environment.

Typical Operating Circuit



Pin Configurations appear at end of data sheet.

Absolute Maximum Ratings

IO Voltage Range to GND.....-0.5V to +6V
IO Sink Current.....20mA
Operating Temperature Range.....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range.....-55°C to +125°C

Lead Temperature (excluding UCSP, soldering, 10s).....+300°C
Soldering Temperature (reflow)
TO-92.....+250°C
All other packages, excluding SFN.....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN: GENERAL DATA						
1-Wire Pullup Voltage	V_{PUP}	(Note 2)	2.8		5.25	V
1-Wire Pullup Resistance	R_{PUP}	(Notes 2, 3)	0.3		2.2	kΩ
Input Capacitance	C_{IO}	(Notes 4, 5)			1000	pF
Input Load Current	I_L	IO pin at V_{PUP}	0.05		6.7	µA
High-to-Low Switching Threshold	V_{TL}	(Notes 5, 6, 7)	0.5		V_{PUP} - 1.8	V
Input Low Voltage	V_{IL}	(Notes 2, 8)			0.5	V
Low-to-High Switching Threshold	V_{TH}	(Notes 5, 6, 9)	1.0		V_{PUP} - 1.0	V
Switching Hysteresis	V_{HY}	(Notes 5, 6, 10)	0.21		1.70	V
Output Low Voltage	V_{OL}	At 4mA (Note 11)			0.4	V
Recovery Time (Notes 2,12)	t_{REC}	Standard speed, R_{PUP} = 2.2kΩ	5			µs
		Overdrive speed, R_{PUP} = 2.2kΩ	2			
		Overdrive speed, directly prior to reset pulse; R_{PUP} = 2.2kΩ	5			
Rising-Edge Hold-Off Time (Notes 5, 13)	t_{REH}	Standard speed	0.5		5.0	µs
		Overdrive speed	Not applicable (0)			
Time Slot Duration (Notes 2, 14)	t_{SLOT}	Standard speed	65			µs
		Overdrive speed	8			
IO PIN: 1-Wire RESET, PRESENCE-DETECT CYCLE						
Reset Low Time (Note 2)	t_{RSTL}	Standard speed	480		640	µs
		Overdrive speed	48		80	
Presence-Detect High Time	t_{PDH}	Standard speed	15		60	µs
		Overdrive speed	2		6	
Presence-Detect Low Time	t_{PDL}	Standard speed	60		240	µs
		Overdrive speed	8		24	
Presence-Detect Sample Time (Notes 2, 15)	t_{MSP}	Standard speed	60		75	µs
		Overdrive speed	6		10	

Electrical Characteristics (continued)

(T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN: 1-Wire WRITE						
Write-Zero Low Time (Notes 2, 16, 17)	t_{W0L}	Standard speed	52.1		120	µs
		Overdrive speed, V_{PUP} > 4.5V	5		15.5	
		Overdrive speed	6		15.5	
Write-One Low Time (Notes 2, 17)	t_{W1L}	Standard speed	1		15	µs
		Overdrive speed	1		2	
IO PIN: 1-Wire READ						
Read Low Time (Notes 2, 18)	t_{RL}	Standard speed	5		15 - δ	µs
		Overdrive speed	1		2 - δ	
Read Sample Time (Notes 2, 18)	t_{MSR}	Standard speed	t_{RL} + δ		15	µs
		Overdrive speed	t_{RL} + δ		2	
EEPROM						
Programming Current	I_{PROG}	(Notes 5, 19)			0.8	mA
Programming Time	t_{PROG}	(Notes 20, 21)			10	ms
Write/Erase Cycles (Endurance) (Notes 22, 23)	N_{CY}	At +25°C	200k			—
		At +85°C (worst case)	50k			
Data Retention (Notes 24, 25, 26)	t_{DR}	At +85°C (worst case)	40			Years

Note 1: Limits are 100% production tested at T_A = +25°C and/or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.

Note 2: System requirement.

Note 3: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times. For more heavily loaded systems, an active pullup such as that found in the DS2482-x00, DS2480B, or DS2490 may be required.

Note 4: Maximum value represents the internal parasite capacitance when V_{PUP} is first applied. Once the parasite capacitance is charged, it does not affect normal communication.

Note 5: Guaranteed by design, characterization, and/or simulation only. Not production tested.

Note 6: V_{TL}, V_{TH}, and V_{HY} are a function of the internal supply voltage, which is a function of V_{PUP}, R_{PUP}, 1-Wire timing, and capacitive loading on IO. Lower V_{PUP}, higher R_{PUP}, shorter t_{REC}, and heavier capacitive loading all lead to lower values of V_{TL}, V_{TH}, and V_{HY}.

Note 7: Voltage below which, during a falling edge on IO, a logic 0 is detected.

Note 8: The voltage on IO must be less than or equal to V_{ILMAX} at all times the master is driving IO to a logic 0 level.

Note 9: Voltage above which, during a rising edge on IO, a logic 1 is detected.

Note 10: After V_{TH} is crossed during a rising edge on IO, the voltage on IO must drop by at least V_{HY} to be detected as logic 0.

Note 11: The I-V characteristic is linear for voltages less than 1V.

Note 12: Applies to a single device attached to a 1-Wire line.

Note 13: The earliest recognition of a negative edge is possible at t_{REH} after V_{TH} has been reached on the preceding rising edge.

Note 14: Defines maximum possible bit rate. Equal to t_{W0LMIN} + t_{RECMIN}.

Note 15: Interval after t_{RSTL} during which a bus master can read a logic 0 on IO if there is a DS2431 present. The power-up presence detect pulse could be outside this interval, but will be complete within 2ms after power-up.

Note 16: Numbers in **bold** are **not** in compliance with legacy 1-Wire product standards. See the *Comparison Table*.

Note 17: ε in Figure 11 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to V_{TH}. The actual maximum duration for the master to pull the line low is t_{W1LMAX} + $t_{F\,-\,\varepsilon}$ and t_{W0LMAX} + $t_{F\,-\,\varepsilon}$, respectively.

Note 18: δ in Figure 11 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to the input-high threshold of the bus master. The actual maximum duration for the master to pull the line low is t_{RLMAX} + t_F.

Note 19: Current drawn from IO during the EEPROM programming interval. The pullup circuit on IO during the programming interval should be such that the voltage at IO is greater than or equal to V_{PUPMIN}. If V_{PUP} in the system is close to V_{PUPMIN}, a low-impedance bypass of R_{PUP}, which can be activated during programming, may need to be added.

Note 20: Interval begins t_{REHMAX} after the trailing rising edge on IO for the last time slot of the E/S byte for a valid Copy Scratchpad sequence. Interval ends once the device's self-timed EEPROM programming cycle is complete and the current drawn by the device has returned from I_{PROG} to I_L.

Note 21: t_{PROG} for units branded version "A1" is 12.5ms. t_{PROG} for units branded version "A2" and later is 10ms.

Note 22: Write-cycle endurance is degraded as T_A increases.

Note 23: Not 100% production tested; guaranteed by reliability monitor sampling.

Note 24: Data retention is degraded as T_A increases.

Note 25: Guaranteed by 100% production test at elevated temperature for a shorter time; equivalence of this production test to the data sheet limit at operating temperature range is established by reliability testing.

Note 26: EEPROM writes can become nonfunctional after the data-retention time is exceeded. Long-term storage at elevated temperatures is not recommended; the device can lose its write capability after 10 years at +125°C or 40 years at +85°C.

Comparison Table

PARAMETER	LEGACY VALUES				DS2431 VALUES			
	STANDARD SPEED (µs)		OVERDRIVE SPEED (µs)		STANDARD SPEED (µs)		OVERDRIVE SPEED (µs)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
t_{SLOT} (including t_{REC})	61	(undefined)	7	(undefined)	65*	(undefined)	8*	(undefined)
t_{RSTL}	480	(undefined)	48	80	480	640	48	80
t_{PDH}	15	60	2	6	15	60	2	6
t_{PDL}	60	240	8	24	60	240	8	24
t_{W0L}	60	120	6	16	52.1	120	6	**15.5**

**Intentional change; longer recovery time requirement due to modified 1-Wire front-end.*

***Note:** Numbers in **bold** are **not** in compliance with legacy 1-Wire product standards.*

Pin Description

PIN					NAME	FUNCTION
TSOC	TO-92	TDFN-EP	SFN	UCSPR		
3, 4, 5, 6	3	1, 4, 5, 6	—	A2, A3, C2, C3	N.C.	Not Connected
2	2	2	1	C1	IO	1-Wire Bus Interface. Open-drain signal that requires an external pullup resistor.
1	1	3	2	A1	GND	Ground Reference
—	—	—	—	—	EP	Exposed Pad (TDFN only). Solder evenly to the board's ground plane for proper operation. Refer to Application Note 3273: *Exposed Pads: A Brief Introduction* for additional information.

Detailed Description

The DS2431 combines 1024 bits of EEPROM, an 8-byte register/control page with up to 7 user read/write bytes, and a fully featured 1-Wire interface in a single chip. Each DS2431 has its own 64-bit ROM registration number that is factory lasered into the chip to provide a guaranteed unique identity for absolute traceability. Data is transferred serially through the 1-Wire protocol, which requires only a single data lead and a ground return. The DS2431 has an additional memory area called the scratchpad that acts as a buffer when writing to the main memory or the register page. Data is first written to the scratchpad from which it can be read back. After the data has been verified, a Copy Scratchpad command transfers the data to its final memory location. The DS2431 applications include accessory/PCB identification, medical sensor calibration data storage, analog sensor calibration including IEEE P1451.4 smart sensors, ink and toner print cartridge identification, and after-market management of consumables.

Overview

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS2431. The DS2431 has four main data components: 64-bit lasered ROM, 64-bit scratchpad, four 32-byte pages of EEPROM, and a 64-bit register page.

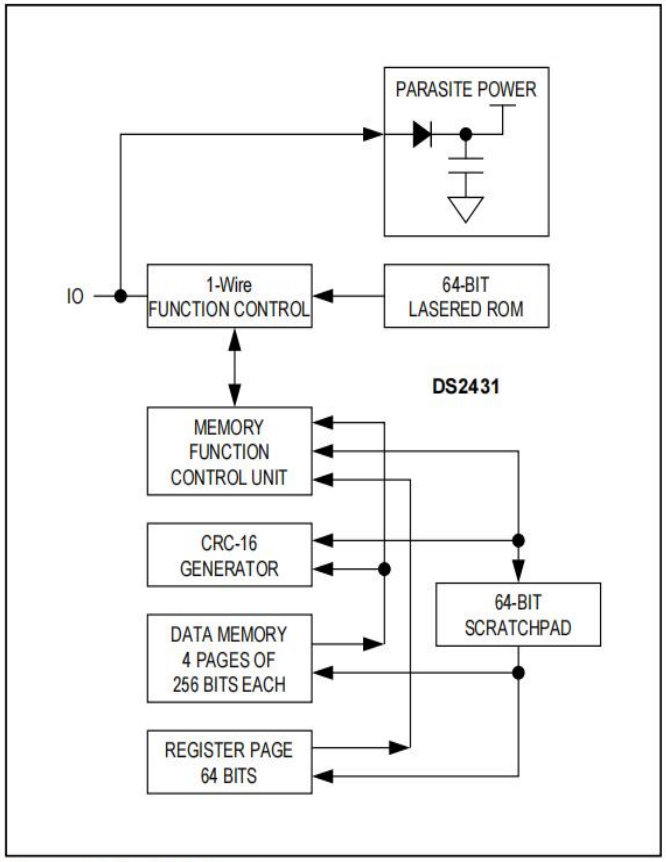


Figure 1. Block Diagram

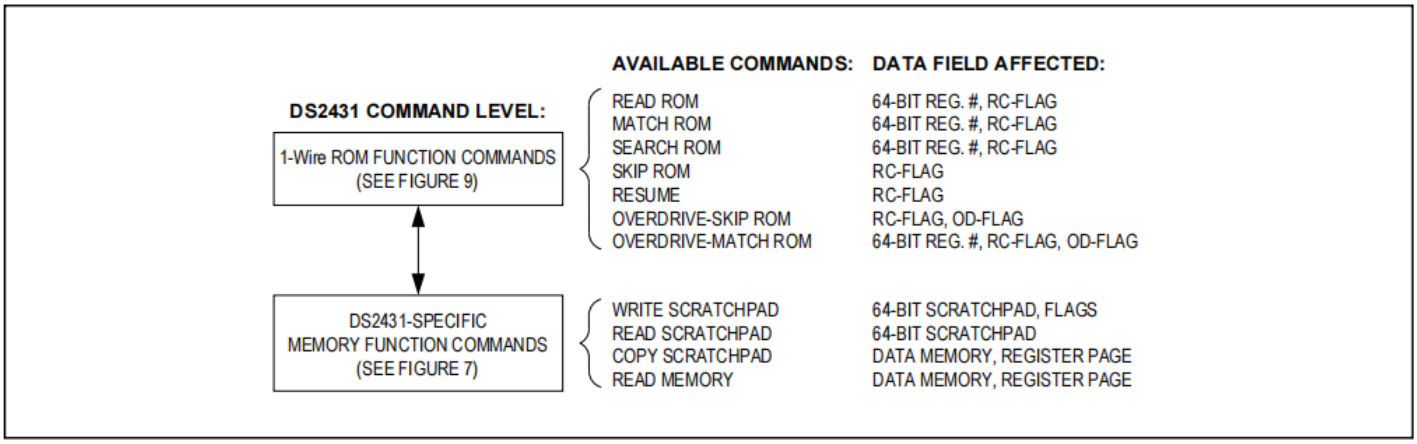


Figure 2. Hierarchical Structure for 1-Wire Protocol

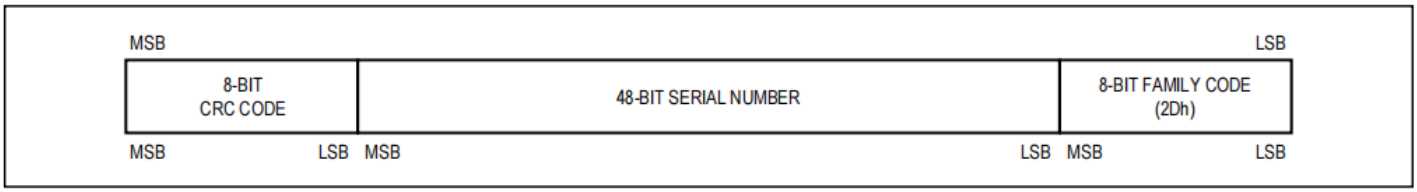


Figure 3. 64-Bit Lasered ROM

The hierarchical structure of the 1-Wire protocol is shown in Figure 2. The bus master must first provide one of the seven ROM function commands: Read ROM, Match ROM, Search ROM, Skip ROM, Resume, Overdrive-Skip ROM, or Overdrive-Match ROM. Upon completion of an Overdrive-Skip ROM or Overdrive-Match ROM command byte executed at standard speed, the device enters overdrive mode where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 9. After a ROM function command is successfully executed, the memory functions become accessible and the master can provide any one of the four memory function commands. The protocol for these memory function commands is described in Figure 7. **All data is read and written least significant bit first**.

64-Bit Lasered ROM

Each DS2431 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a cyclic redundancy check (CRC) of the first 56 bits. See Figure 3 for details. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the 1-Wire CRC is available in Application Note 27: *Understanding and Using Cyclic Redundancy Checks with Maxim iButton® Products*.

The shift register bits are initialized to 0. Then, starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, the serial number is entered. After the last bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of the CRC returns the shift register to all 0s.

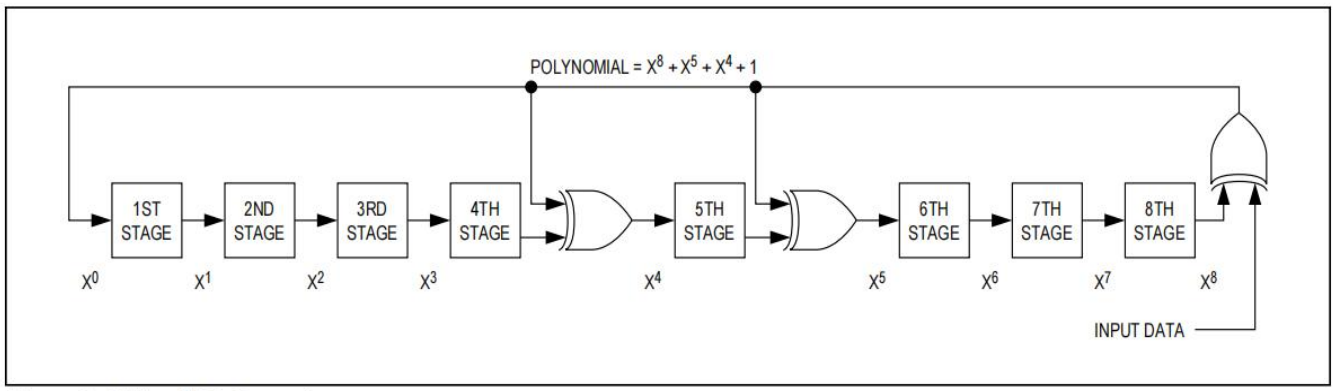


Figure 4. 1-Wire CRC Generator

Memory Access

Data memory and registers are located in a linear address space, as shown in Figure 5. The data memory and the registers have unrestricted read access. The DS2431 EEPROM array consists of 18 rows of 8 bytes each. The first 16 rows are divided equally into four memory pages (32 bytes each). These four pages are the primary data memory. Each page can be individually set to open (unprotected), write protected, or EPROM mode by setting the associated protection byte in the register row. As a factory default, the entire data memory is unprotected and its contents are undefined. The last two rows contain protection registers and reserved bytes. The register row consists of 4 protection control bytes, a copy-protection byte, the factory byte, and 2 user byte/manufacture ID bytes. The manufacturer ID can be a customer-supplied identification code that assists the application software in identifying the product the DS2431 is associated with.

ADDRESS RANGE	TYPE	DESCRIPTION	PROTECTION CODES
0000h to 001Fh	R/(W)	Data Memory Page 0	—
0020h to 003Fh	R/(W)	Data Memory Page 1	—
0040h to 005Fh	R/(W)	Data Memory Page 2	—
0060h to 007Fh	R/(W)	Data Memory Page 3	—
0080h*	R/(W)	Protection Control Byte Page 0	55h: Write Protect P0; AAh: EPROM Mode P0; 55h or AAh: Write Protect 80h
0081h*	R/(W)	Protection Control Byte Page 1	55h: Write Protect P1; AAh: EPROM Mode P1; 55h or AAh: Write Protect 81h
0082h*	R/(W)	Protection Control Byte Page 2	55h: Write Protect P2; AAh: EPROM Mode P2; 55h or AAh: Write Protect 82h
0083h*	R/(W)	Protection Control Byte Page 3	55h: Write Protect P3; AAh: EPROM Mode P3; 55h or AAh: Write Protect 83h
0084h*	R/(W)	Copy Protection Byte	55h or AAh: Copy Protect 0080h:008Fh, and Any Write-Protected Pages
0085h	R	Factory Byte. Set at Factory.	AAh: Write Protect 85h, 86h, 87h; 55h: Write Protect 85h; Unprotect 86h, 87h
0086h	R/(W)	User Byte/Manufacturer ID	—
0087h	R/(W)	User Byte/Manufacturer ID	—
0088h to 008Fh	—	Reserved	—

**Once programmed to AAh or 55h this address becomes read only. All other codes can be stored, but neither write protect the address nor activate any function.*

Figure 5. Memory Map

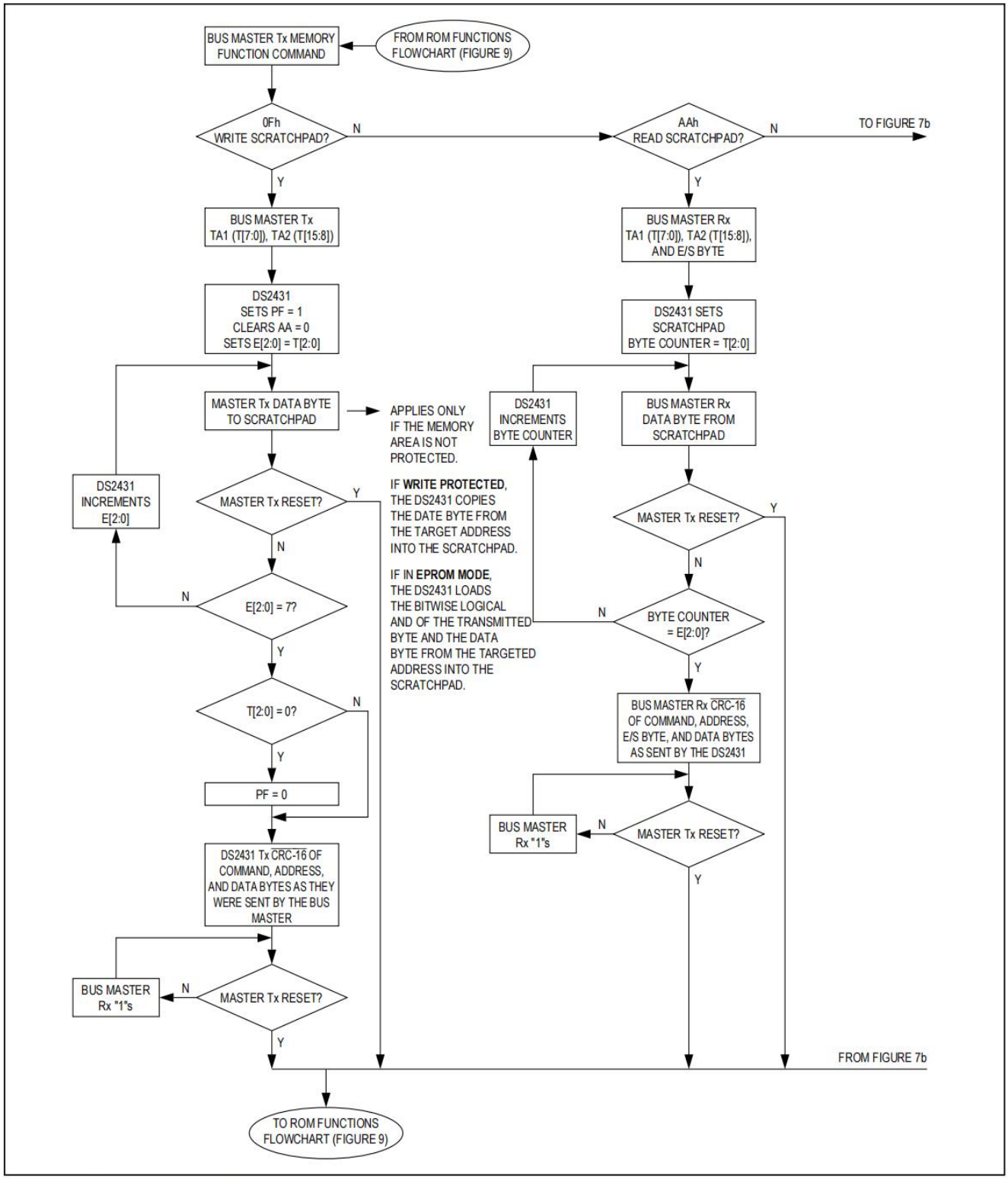


Figure 7a. Memory Function Flowchart

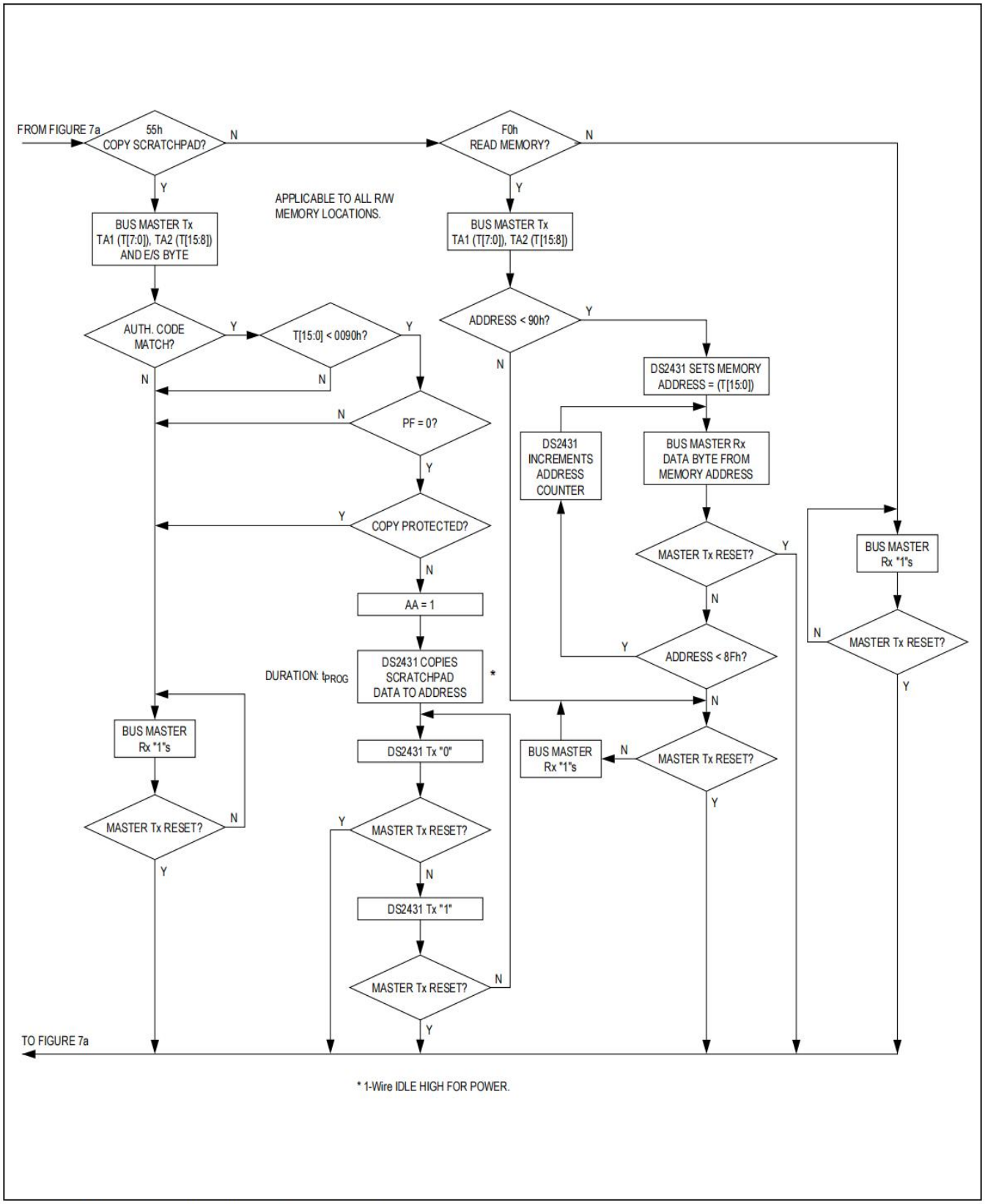


Figure 7b. Memory Function Flowchart (continued)

BIT #	7	6	5	4	3	2	1	0
TARGET ADDRESS (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY)	AA	0	PF	0	0	E2	E1	E0

Figure 6. Address Registers

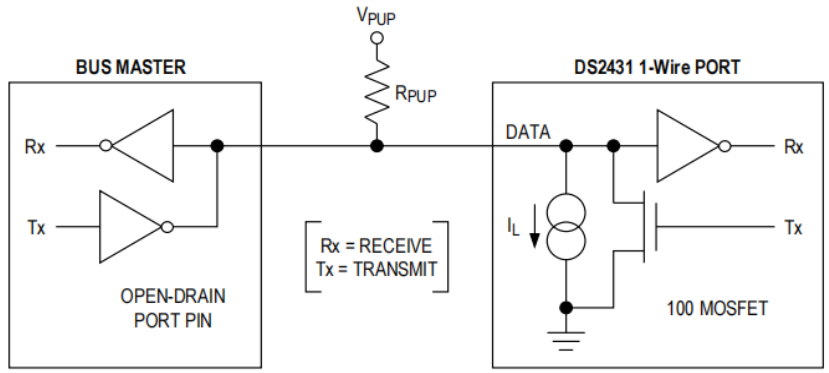


Figure 8. Hardware Configuration

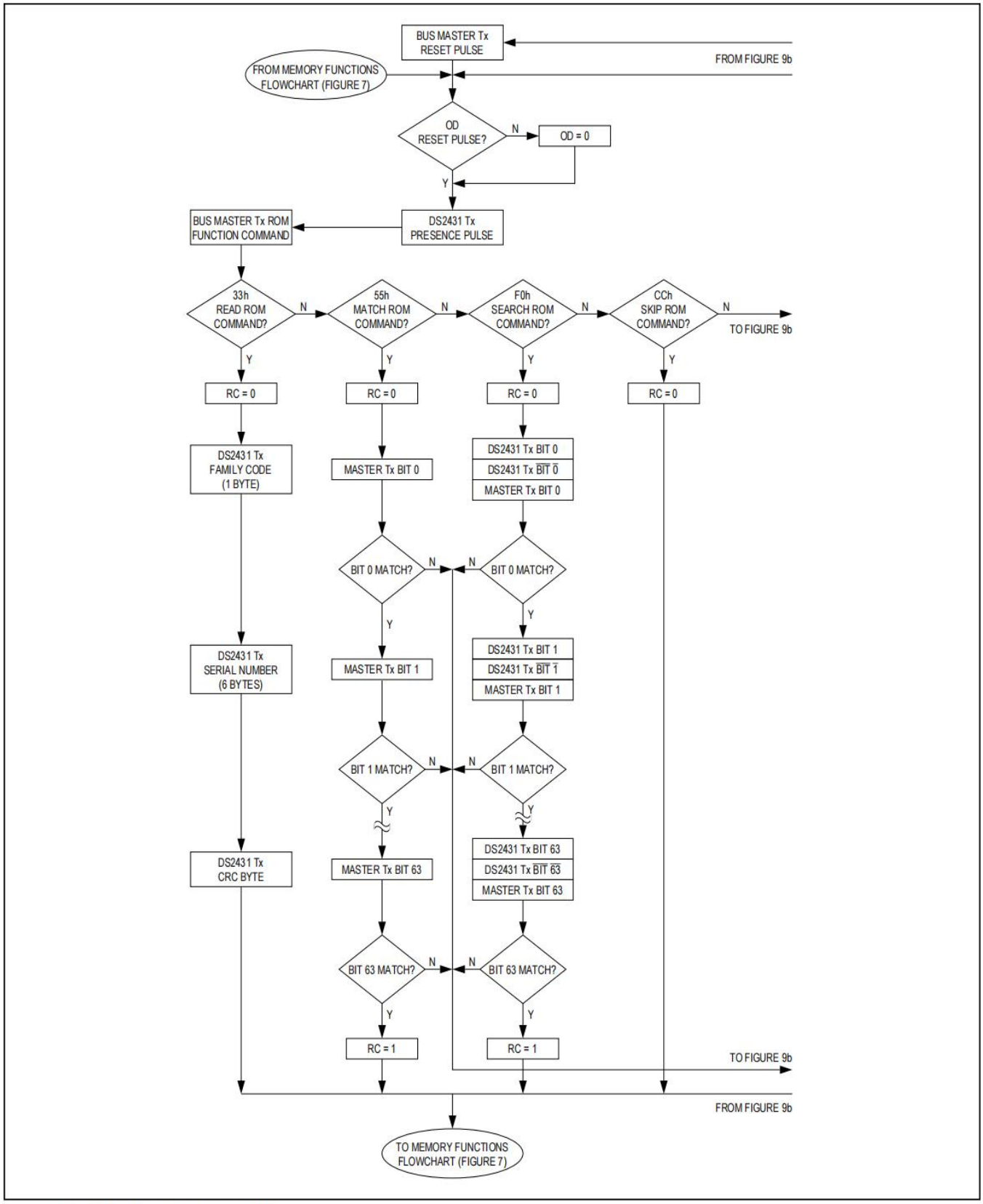


Figure 9a. ROM Functions Flowchart

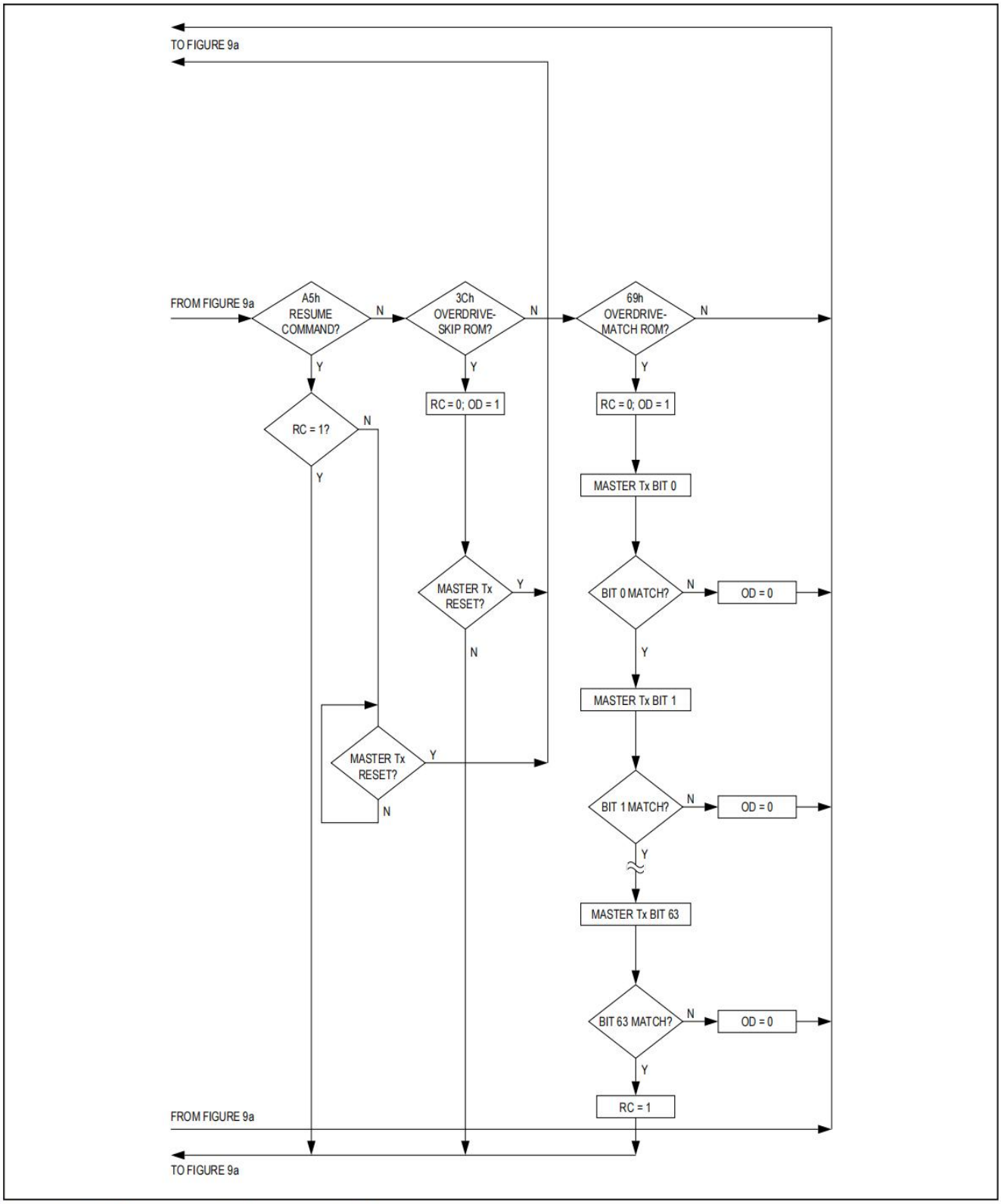


Figure 9b. ROM Functions Flowchart (continued)

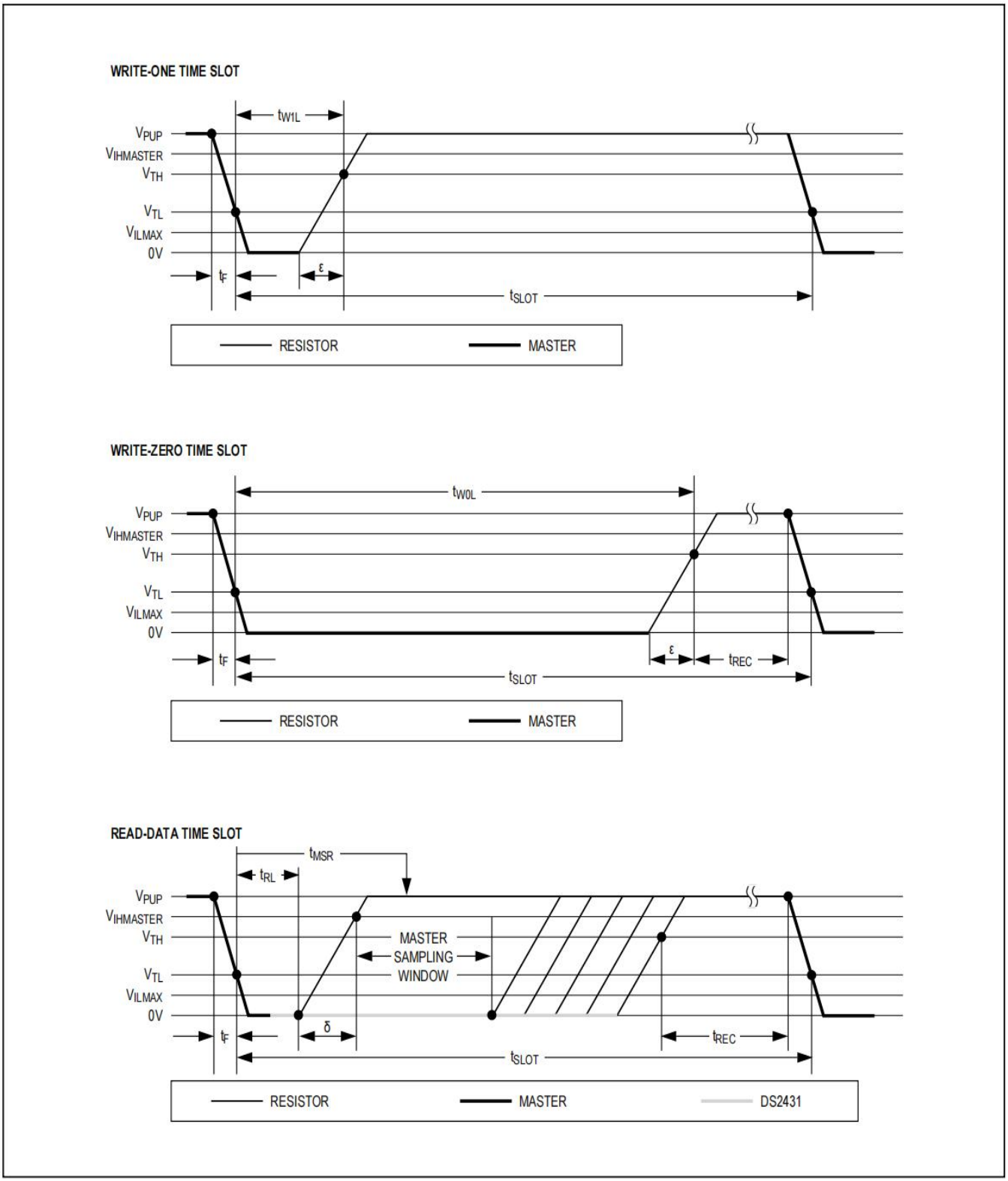


Figure 11. Read/Write Timing Diagrams

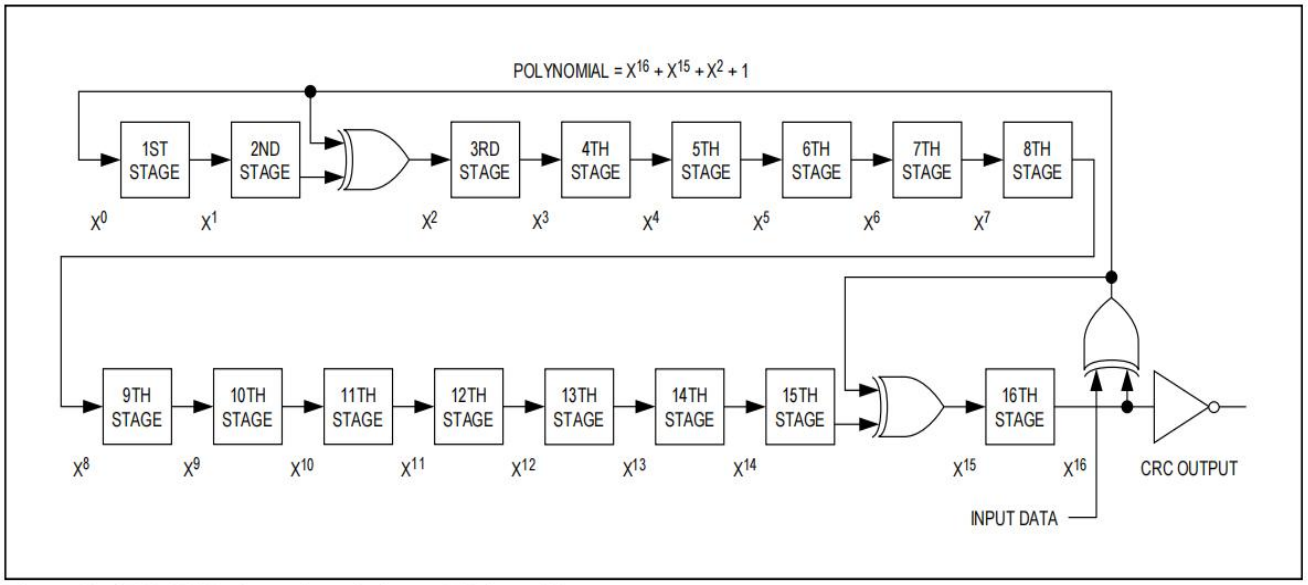


Figure 13. CRC-16 Hardware Description and Polynomial

and all the data bytes as they were sent by the bus master. The DS2431 transmits this CRC only if E[2:0] = 111b.

With the Read Scratchpad command, the CRC is generated by first clearing the CRC generator and then shifting in the command code, the target addresses TA1 and TA2, the E/S byte, and the scratchpad data as they were sent by the DS2431. The DS2431 transmits this CRC only if the reading continues through the end of the scratchpad. For more information on generating CRC values, refer to Application Note 27.

Command-Specific 1-Wire Communication Protocol—Legend

SYMBOL	DESCRIPTION
RST	1-Wire reset pulse generated by master.
PD	1-Wire presence pulse generated by slave.
Select	Command and data to satisfy the ROM function protocol.
WS	Command “Write Scratchpad.”
RS	Command “Read Scratchpad.”
CPS	Command “Copy Scratchpad.”
RM	Command “Read Memory.”
TA	Target address TA1, TA2.
TA-E/S	Target address TA1, TA2 with E/S byte.
<8–T[2:0] bytes>	Transfer of as many bytes as needed to reach the end of the scratchpad for a given target address.
<Data to EOM>	Transfer of as many data bytes as are needed to reach the end of the memory.
$\overline{\text{CRC-16}}$	Transfer of an inverted $\overline{\text{CRC-16}}$.
FF Loop	Indefinite loop where the master reads FF bytes.
AA Loop	Indefinite loop where the master reads AA bytes.
Programming	Data transfer to EEPROM; no activity on the 1-Wire bus permitted during this time.

Memory Function Example

Write to the first 8 bytes of memory page 1. Read the entire memory.

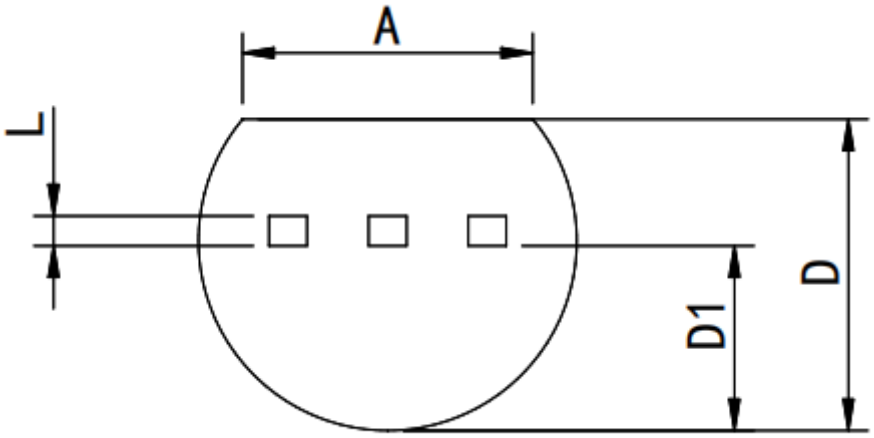
With only a single DS2431 connected to the bus master, the communication looks like this:

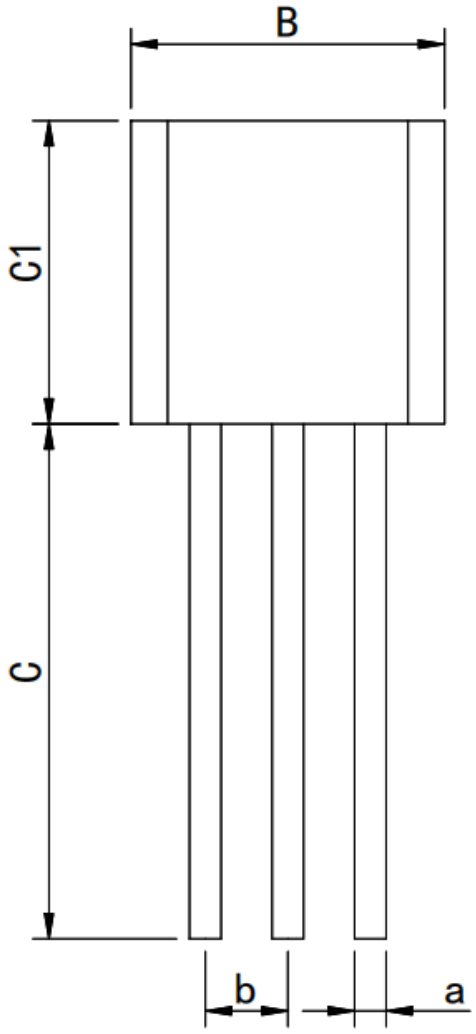
MASTER MODE	DATA (LSB FIRST)	COMMENTS	
Tx	(Reset)	Reset pulse	
Rx	(Presence)	Presence pulse	
Tx	CCh	Issue “Skip ROM” command	
Tx	0Fh	Issue “Write Scratchpad” command	
Tx	20h	TA1, beginning offset = 20h	
Tx	00h	TA2, address = 0020h	
Tx	<8 Data Bytes>	Write 8 bytes of data to scratchpad	
Rx	<2 Bytes CRC-16>	Read CRC to check for data integrity	
Tx	(Reset)	Reset pulse	
Rx	(Presence)	Presence pulse	
Tx	CCh	Issue “Skip ROM” command	
Tx	AAh	Issue “Read Scratchpad” command	
Rx	20h	Read TA1, beginning offset = 20h	
Rx	00h	Read TA2, address = 0020h	
Rx	07h	Read E/S, ending offset = 111b, AA, PF = 0	
Rx	<8 Data Bytes>	Read scratchpad data and verify	
Rx	<2 Bytes CRC-16>	Read CRC to check for data integrity	
Tx	(Reset)	Reset pulse	
Rx	(Presence)	Presence pulse	
Tx	CCh	Issue “Skip ROM” command	
Tx	55h	Issue “Copy Scratchpad” command	
Tx	20h	TA1	(AUTHORIZATION CODE)
Tx	00h	TA2	
Tx	07h	E/S	
—	<1-Wire Idle High>	Wait $t_{PROGMAX}$ for the copy function to complete	
Rx	AAh	Read copy status, AAh = success	
Tx	(Reset)	Reset pulse	
Rx	(Presence)	Presence pulse	
Tx	CCh	Issue “Skip ROM” command	
Tx	F0h	Issue “Read Memory” command	
Tx	00h	TA1, beginning offset = 00h	
Tx	00h	TA2, address = 0000h	
Rx	<144 Data Bytes>	Read the entire memory	
Tx	(Reset)	Reset pulse	
Rx	(Presence)	Presence pulse	

Order information

Order Number	Package	Package Quantity	Marking On The park
DS2431+T&R-TUDI	TO92	1000 pieces per package	DS2431+T&R

Package TO92





Symbol	Min	Max
A	3.43	4.13
B	4.44	5.21
C	13.5	15.3
C1	4.32	5.34
D	3.17	4.19
D1	2.03	2.67
L	0.33	0.42
a	0.40	0.52
b	1.27BSC	

Important statement:

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