High-performance Neural Network Intelligent Voice Chip with A-NPU

Features

- Neural network processor for the audio(A-NPU)
  - A-NPU supports neural networks such as DNN, TDNN, RNN, and CNN, as well as parallel vector operations. It can realize functions including speech recognition, speaker identification, edge-side NLP, command word self-learning, voice detection, and deep learning noise reduction
- CPU and memory
  - The CPU clock speed can reach 240 MHz
  - Built-in 4MBytes Flash memory
  - Built-in 640KBytes SRAM
  - Built-in 512-bit eFuse, can be used for application encryption
- Audio Codec
  - High-performance, low-power audio ADC, SNR ≥ 95dB
  - Low-power audio DAC, SNR ≥ 95dB
- Audio Interface
  - 1-way IIS interface, supports configurable master-slave
  - 1-channel dual-path PDM interface
- ADC and PWM
  - Built-in 4-channel 12-bit SAR ADC
  - Supports 6 PWM interfaces
- GPIO
  - 26 high-speed GPIOs with a response rate of up to 20MHz
  - Among them, 18 GPIOs support 5V input
- Reset and power management
  - Built-in Power Management Unit (PMU)
  - PMU input voltage range: 3.6V to 5.5V
  - Built-in Power-On Reset (POR)
  - Built-in Voltage Detection (PVD)
- Clock
  - Built-in RC oscillator, also supports external crystal oscillator; developers can choose to use either the built-in RC or an external crystal as the chip clock source depending on different application scenarios
- Communication interface
  - 1-channel IIC interface
  - 3 UART interfaces, supporting 5V communication and up to 3Mbps speed
- Timers and Watchdogs
  - Built-in 4 sets of 32-bit timers and 2 sets of watchdogs

General Description

AWA89601QNR is Awinic's high-performance intelligent voice chip, integrating the self-developed A-NPU and CPU core, with a main frequency of 240MHz. It features 640KB of built-in SRAM and rich peripherals such as PMU and audio codecs, requiring only minimal external components to build a high-cost-performance intelligent voice solution.

The chip meets industrial-grade standards, with an operating temperature range of -40°C to 85°C, and complies with multiple reliability certifications such as MSL3, 4KV contact discharge, FCC EMC, ROHS, and REACH.

Its A-NPU technology supports mainstream neural networks such as DNN, RNN, and CNN, features voice/voiceprint recognition, edge-side NLP, command word self-learning, and deep learning noise reduction functions, and supports multiple languages.

Applications

AIoT, AI-Powered Toys, Conference Systems, Intelligent Security Systems

Pin Configuration And Top Mark

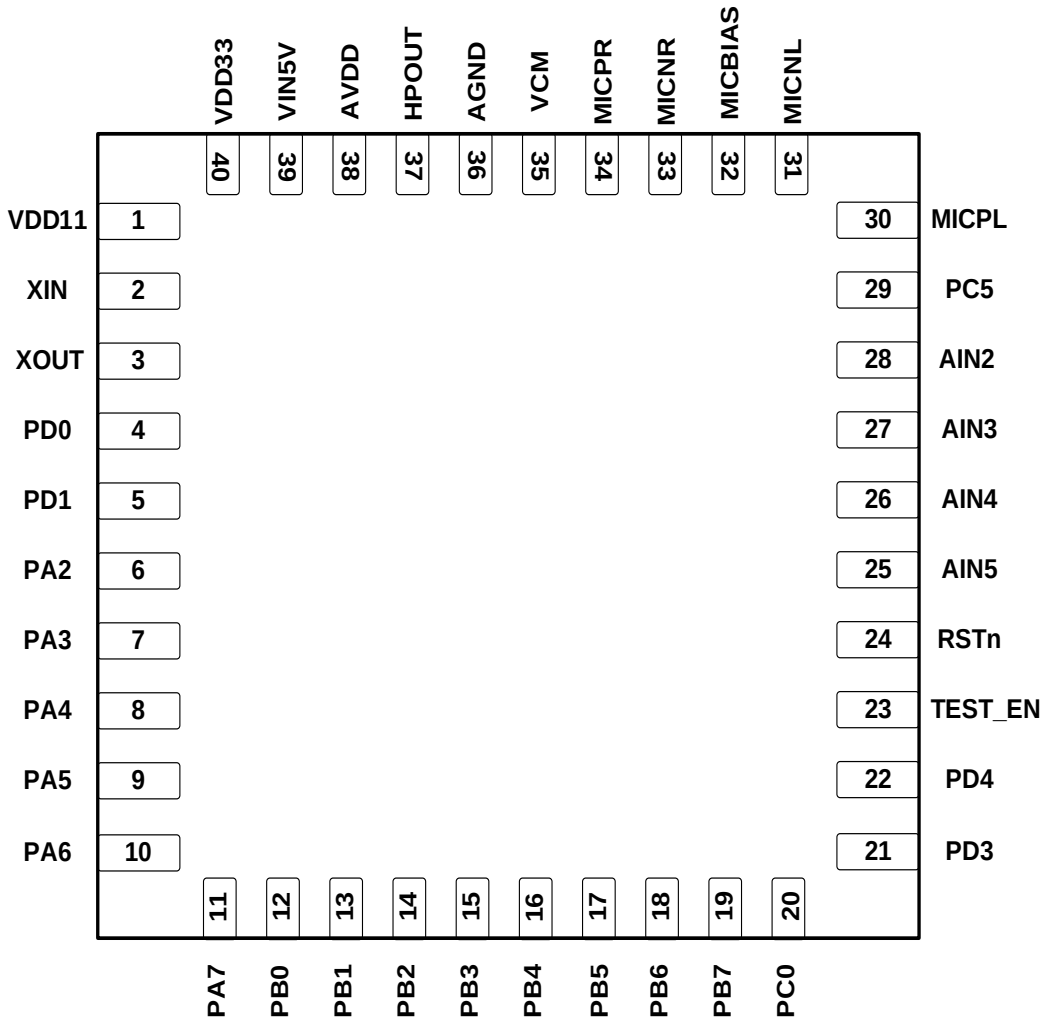


Figure 1 QFN40 Pin Diagram

Pin Definition

Pin No	Pin Name	Description
1	VDD11	1.1V LDO output pin, which is also the core power input pin, connected to an external 4.7uF capacitor
2	XIN	1. External crystal oscillator pin XIN (default state on power-up, no external crystal needed for normal applications) 2.GPIO PA0 3.PWM5
3	XOUT	1. External crystal oscillator pin XOUT (default state on power-up, no external crystal needed for normal use) 2.GPIO PA1
4	PD0	GPIO PD0
5	PD1	GPIO PD1
6	PA2	1.GPIO PA2 (default state at power-on)IIS_SDI 2.IIC_SDA 3.UART1_TX 4.PWM0
7	PA3	1.GPIO PA3 (default state when powered on) 2.IIS_LRCLK 3.IIC_SCL 4.UART1_RX1 5.PWM1
8	PA4	1.GPIO PA4 (default state on power-up) / PG_EN(Determines whether programming is initiated based on the voltage level at power-up; programming function is activated when high level) 2.IIS_SDO 3.PWM2
9	PA5	1.GPIO PA5 (default state when powered on) 2.IIS_SCLK 3.PDM_DAT 4.UART2_TX 5. PWM3
10	PA6	1.GPIO PA6 (default state when powered on) 2.IIS_MCLK 3.PDM_CLK 4.UART2_RX 5.PWM4
11	PA7	1.GPIO PA7 (default state when powered on) 2.PWM0 3.UART1_TX 4.EXT_INT[0]
12	PB0	1.GPIO PB0 (default state when powered on) 2.PWM1 3.UART1_RX 4.EXT_INT[1]
13	PB1	1.GPIO PB1 (default state when 2.powered on) 3.PWM2 4.UART2_TX

Pin No	Pin Name	Description
14	PB2	1.GPIO PB2 (default state when 2.powered on) 3.PWM3 4.UART2_RX
15	PB3	1.GPIO PB3 (default state when powered on) 2.PWM4 3.IIC_SDA
16	PB4	1.GPIO PB4 (default state when powered on) 2.PWM5 3.IIC_SCL
17	PB5	1.GPIO PB5 (default state when powered on) 2.UART0_TX 3.IIC_SDA 4.PWM1
18	PB6	1.GPIO PB6 (default state when powered on) 2.UART0_RX 3.IIC_SCL 4.PWM2
19	PB7	1.GPIO PB7 (default state when powered on) 2.UART1_TX 3.IIC_SDA 4.PWM3
20	PC0	1.GPIO PC0 (default state when powered on) 2.UART1_RX 3.IIC_SCL 4.PWM4
21	PD3	GPIO PD3
22	PD4	GPIO PD4
23	TEST_EN	Test Pin NOTE1
24	RSTn	Reset Pin NOTE2
25	AIN5	1.Hold (default state when powered on) 2.GPIO PC1 3.UART2_TX 4.PWM3 5.PDM_DAT 6.SAR ADC input channel 5
26	AIN4	1.Hold (default state when powered on) 2.GPIO PC2 3.UART2_RX 4.PWM2 5.PDM_CLK 6.SAR ADC input channel 4
27	AIN3	1.Hold (default state when powered on) 2.GPIO PC3 3.IIC_SDA 4.PWM1 5.PDM_DAT 6.SAR ADC input channel 3

Pin No	Pin Name	Description
28	AIN2	1.Hold (default state when powered on) 2.GPIO PC4 3.IIC_SCL 4.PWM0 5.PDM_CLK 6.SAR ADC input channel 2
29	PC5	GPIO PC5/BOOT_SEL (Determines the system's boot device based on the voltage level at power-up; boots from Flash when low, and from SRAM when high)
30	MICPL	Left Microphone P input
31	MICNL	Left Microphone N input
32	MICBIAS	Microphone bias output
33	MICNR	Right Microphone N input
34	MICPR	Right Microphone P input
35	VCM	VCM Output
36	AGND	Analog ground
37	HPOUT	DAC output
38	AVDD	3.3V analog LDO output pin, which is also the analog power input pin, with an external 4.7uF capacitor connected.
39	VIN5V	VIN5V is the PMU power input pin. The normal operating input voltage range is 3.6V to 5.5V. Connect an external 4.7μF input capacitor. The maximum input voltage for this pin is 6.5V. Note that overvoltage and surge protection devices, such as a TVS diode and a 4.7-ohm resistor, should be added to this pin to prevent surge damage.
40	VDD33	3.3V LDO output pin, connect an external 4.7uF capacitor
41	GND	The chip's bottom pad is grounded NOTE3

NOTE1: TEST_EN is the pin that enables the test function. It has an internal pull-down resistor. When powered on, the input level of this pin is detected. If it is low, the chip starts normally; if it is high, it enters test mode.

NOTE2: RSTn is an external reset input pin. Pulling it low for more than 100 μs enables the chip reset.

NOTE3: The bottom of the QFN40 package has a thermal pad, which needs to be connected to ground during us

Block Diagram

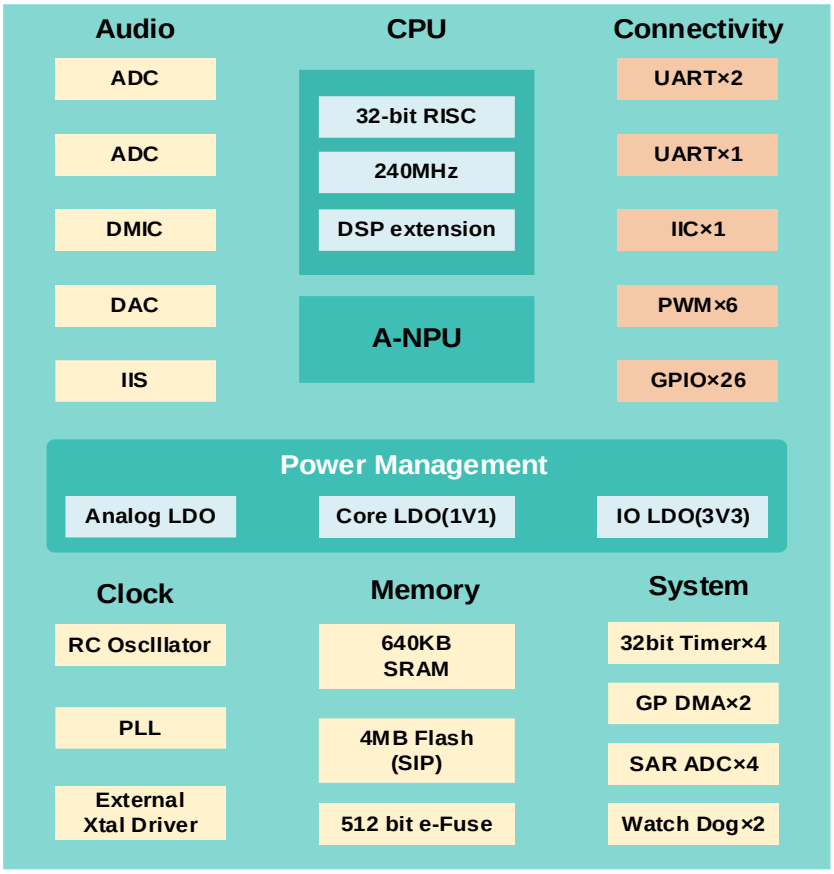


Figure 2 Chip Functional Block Diagram

- **Neural Network Processor For Audio(A-NPU)**
  - Adopting hardware technology, it supports neural networks such as DNN, TDNN, RNN, CNN, as well as parallel vector operations, enabling functions such as speech recognition, voiceprint recognition, edge-side NLP, command word self-learning, voice detection, and deep learning noise reduction
- **CPU**
  - 32-bit high-performance CPU, with a maximum operating frequency of up to 240MHz
  - 32-bit single-cycle multiplier, supports DSP extension acceleration
- **Memory**
  - Built-in 640KB SRAM
  - Built-in 512-bit eFuse
  - Built-in 4MB Flash
- **Audio Interface**
  - Built-in high-performance, low-power Audio Codec module, supporting dual ADC sampling and single DAC playback
  - Supports Automatic Level Control (ALC) function
  - Supports 8kHz/16kHz/24kHz/32kHz/44.1kHz/48kHz sampling rates
  - Supports a single IIS audio extension path
  - Supports a single PDM interface, which can connect to one or two digital MEMS microphones
- **Power Management Unit (PMU)**

- Built-in 3 high-performance LDOs, no external power chip required, only a small number of resistors and capacitors needed externally
- Supports direct 5V power input, with a power supply range supporting a minimum input of 3.6V and a maximum input of 5.5V

■ **Clock**

- It has a built-in RC oscillator and also supports an external crystal oscillator; developers can choose to use the built-in RC or an external crystal as the chip's clock source according to different application scenarios

■ **SAR ADC**

- 4-channel 12-bit SAR ADC input, with a sampling frequency of up to 1 MHz
- ADC IO can be multiplexed with digital GPIO functions

■ **Peripherals and timers**

- 3 UART interfaces, supporting up to 3M baud rate
- 1 IIC interface, which can be used to connect external IIC devices for expansion
- 6-channel PWM interface, suitable for direct driving of lighting and motor applications
- Built-in 4 sets of 32-bit timers
- Built-in 1 independent watchdog (IWDG)
- Built-in 1 window watchdog (WWDG)

■ **GPIO**

- Supports 26 GPIO pins and can be used as the main control IC
- Except for the 4 GPIO pins corresponding to PD, other GPIO pins can be configured with interrupt functions, and all GPIO pins support configurable pull-up and pull-down
- Some GPIOs support wide-voltage 5V level signal communication directly, without the need for external level conversion

■ **Software development support**

- Provides a complete software development kit, application solution examples, and an online platform for creating firmware for voice development, etc.

■ **Firmware burning and protection**

- Supports UART upgrade and firmware protection

■ **EMC and ESD**

- Good EMC design, compliant with FCC standards
- Internal ESD enhanced design, capable of withstanding 4KV contact discharge test

■ **ROHS and REACH**

- Made with eco-friendly materials, compliant with ROHS and REACH testing

■ **Packaging and operating temperature range**

- Package type: QFN40, dimensions are 5mm length, 5mm width, 0.85mm height
- Operating temperature: -40℃ to 85℃

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWA89601QNR	-40℃～85℃	QFN 5mmX5mm-40L	BDCK	MSL3	ROHS+HF	5000 units/ Tape and Reel

Electrical Characteristics

Test condition: VIN5V=5V, TA=25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Digital Logical Interface						
V_{IH}	Logic input high level	3.0V ≤ VD33 ≤ 3.6V	0.7 x VDD33			V
V_{IL}	Logic input low level				0.3 x VDD33	V
V_{OH}	Logic output high level	I_{OH} = 20mA			0.4	V
V_{OL}	Logic output low level	I_{OL} = 12mA	2.4			V
I_{5VIO}	Driving current of IO when outputting 3.3V	5V withstand voltage	5		23	mA
I_{33VIO}	Driving current of IO when outputting 3.3V	3.3V withstand voltage	12		26	mA
$\sum IVDD$	The total current of all IOs of the chip				180	mA
Power						
VIN5V	The PMU input pin voltage		3.6	5	5.5	V
AVDD	Analog and Codec power supply voltage		2.97	3.3	3.63	V
VDD33	Chip IO supply voltage		2.97	3.3	3.63	V
VDD11	Chip core supply voltage		0.99	1.1	1.22	V
Codec Performance For ADC						
SNR	Signal-to-noise ratio	With A-Weighted Filter		95		dB
THD+N	Total harmonic distortion	-3dBFS input		-80		dB
Codec Performance For DAC						

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio, A-weighted	With A-Weighted Filter		95		dB
THD+N	Total harmonic distortion	30mW 32 ohm loading		-75		dB
Power Consumption Of Work						
Pde	Using 5V power supply, the chip 1.1V is powered by an external DC-DC chip, and the total power consumption with 5V input during normal operation	ambient temperature TA = 25 °C	75		175	mW
Pdi	Using 5V power supply, using an internal PMU, and the total power consumption at 5V input under normal operation	ambient temperature TA = 25 °C	165		265	mW
Performance Of RC Oscillator						
RC oscillator accuracy	Frequency accuracy of RC oscillator at different temperatures	TA = -40 to 85℃	-4		+3	%
		TA = -20 to 85℃	-3		+3	%
		TA = -10 to 70℃	-2.5		+2.5	%

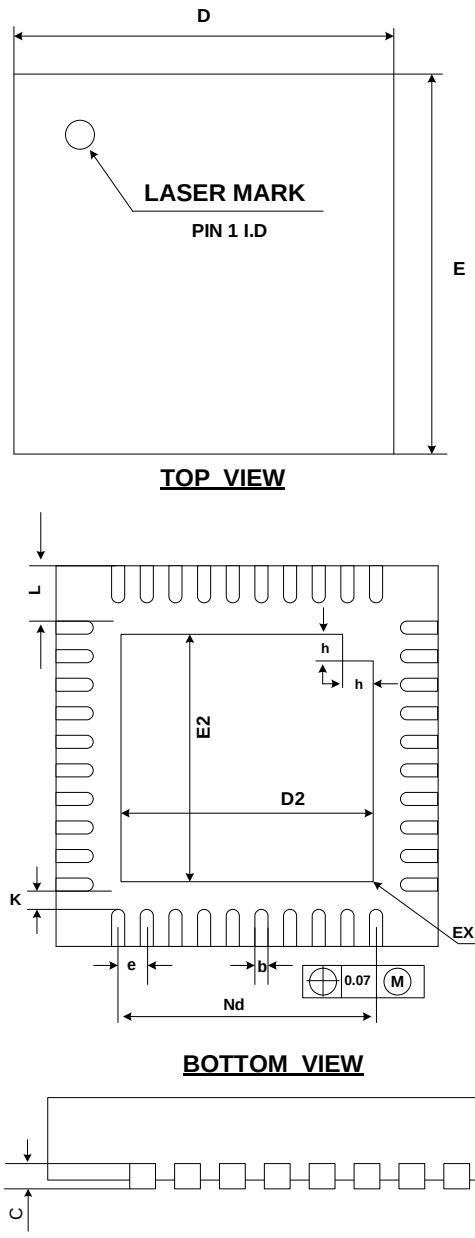
Pin Diagram And Function Description

REUSE FUNCTIONALITY

Pin Name	Function1	Function2	Function3	Function4	Function5	Analog Function	Specific Function
XIN	PA0	PWM5	-	-	-	XIN	-
XOUT	PA1	-	-	-	-	XOUT	-
PA2	PA2	IIS_SDI	IIC_SDA	UART1_TX	PWM0	-	-
PA3	PA3	IIS_LRCLK	IIC_SCL	UART1_RX	PWM1	-	-
PA4	PA4	IIS_SDO	-	-	PWM2	-	PG_EN NOTE1
PA5	PA5	IIS_SCLK	PDM_DAT	UART2_TX	PWM3	-	-
PA6	PA6	IIS_MCLK	PDM_CLK	UART2_RX	PWM4	-	-
PA7	PA7	PWM0	UART1_TX	EXT_INT[0]	-	-	-
PB0	PB0	PWM1	UART1_RX	EXT_INT[1]	-	-	-
PB1	PB1	PWM2	UART2_TX	-	-	-	-
PB2	PB2	PWM3	UART2_RX	-	-	-	-
PB3	PB3	PWM4	IIC_SDA	-	-	-	-
PB4	PB4	PWM5	IIC_SCL	-	-	-	-
PB5	PB5	UART0_TX	IIC_SDA	PWM1	-	-	-
PB6	PB6	UART0_RX	IIC_SCL	PWM2	-	-	-
PB7	PB7	UART1_TX	IIC_SDA	PWM3	PDM_DAT	-	-
PC0	PC0	UART1_RX	IIC_SCL	PWM4	PDM_CLK	-	-
AIN5	-	PC1	UART2_TX	PWM3	PDM_DAT	AIN5	-
AIN4	-	PC2	UART2_RX	PWM2	PDM_CLK	AIN4	-
AIN3	-	PC3	IIC_SDA	PWM1	PDM_DAT	AIN3	-
AIN2	-	PC4	IIC_SCL	PWM0	PDM_CLK	AIN2	-
PC5	PC5	-	-	-	-	-	BOOT_SEL

Note1: Pin 8 of the chip, PA4 (PG_EN), is internally pulled up by default. When powered on, if it is detected as high, the chip will automatically enter upgrade mode if an upgrade signal is detected on UART0 during power-up. At this time, the accompanying upgrade tool can be used to program the internal Nor Flash of the chip. If no upgrade signal is detected on UART0, it will enter normal operating mode.

Encapsulated Information



COMMON DIMENSIONS

SYMBOL	UNIT：MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	_	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
e	0.40BSC		
Nd	3.60BSC		
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.35	0.40	0.45
K	0.20	_	_
h	0.30	0.35	0.40

Figure 3 Package size

Revision History

Version	Date	Change Record
V1.0	Oct. 2025	Briefly released

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