2-channel Force Touch AFE

Features

- 2 analog input differential channel
- Selectable Gains of 1,8,16, 32, 64, 128, 256,512,1024
- 150 KSPS 14-bit SAR ADC
- 11-bit offset calibration DAC
- Support 400KHz/1MHz I²C
- 1 smart watch dog timer(SWDT)
- Support Temperature Sense
- 1 INTN pin
- Power-on reset, Low voltage detection
- Low voltage reset
- Low power consumption mode
- Built-in pressing algorithm
- WLCSP 1.41mmX1.41mmX0.34mm-16B package
- FCQFN 1.6mmX1.6mmX0.55mm-12L package

Applications

TWS IOT

Mobile phones

Smart Home

General Description

AW86862 is a chip of force touch AFE, which has the functions of pressure sensing signal acquisition, amplification and processing. It integrated 1 I²C module, 1 system control module, 1 power management module and 1 AFE module (Include 2 analog input differential channel and MUX, level 2 PGA, 11-bit offset calibration DAC, 14bit ADC and pressing algorithm).

AW86862 can enter low power consumption mode automatically without the master participation and trigger AFE work through SWDT wake-up to sample and process the signal. In low power consumption mode, the operating frequency of the chip is 10Hz and the power consumption is 8~13μA. Interrupt signals such as sampling completion, threshold comparison and press event trigger can be configured to output through interrupt pin.

The AW86862 is available in a WLCSP 1.41mmX1.41mmX0.34mm-16B and FCQFN 1.6mmX1.6mmX0.55mm-12L package.

Typical Application Circuit

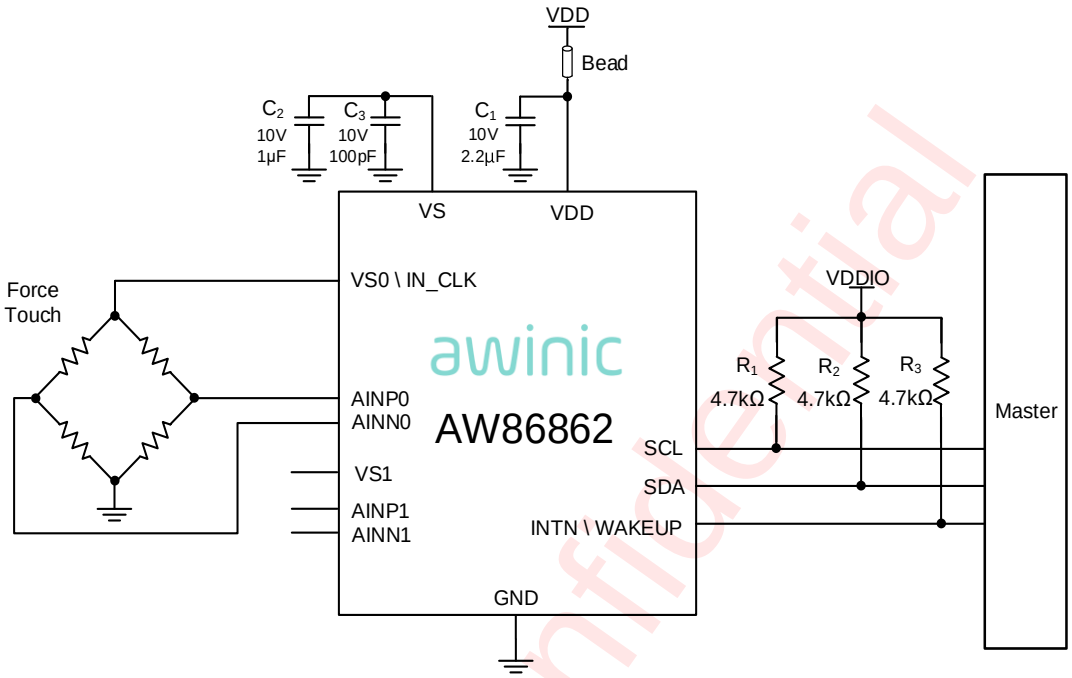
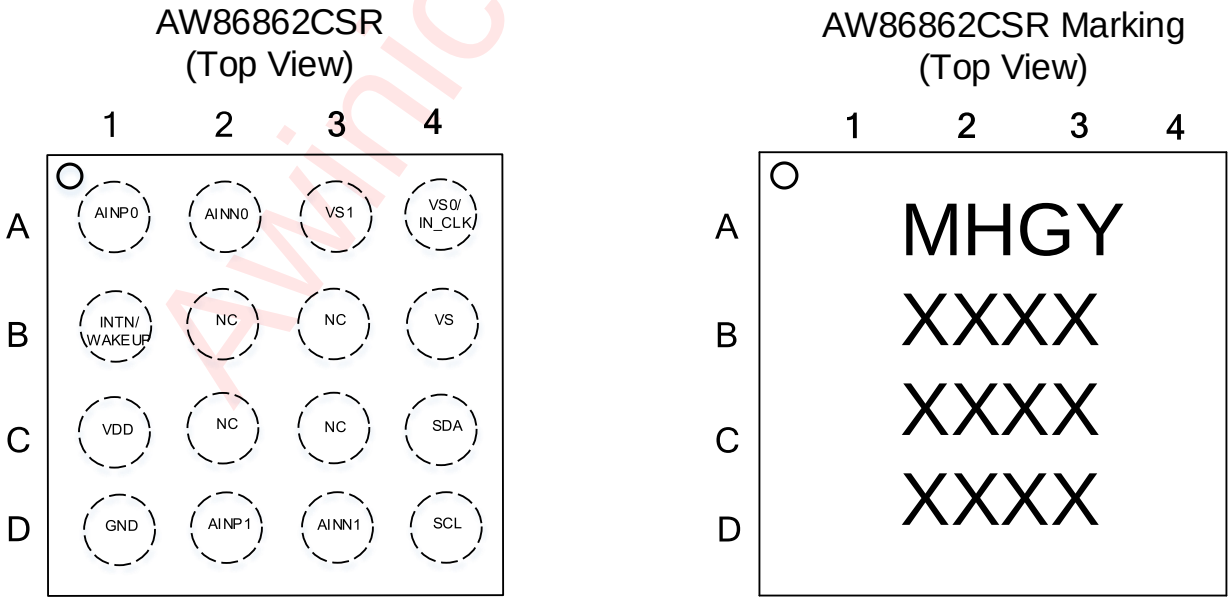


Figure 1 AW86862 Typical Application Circuit

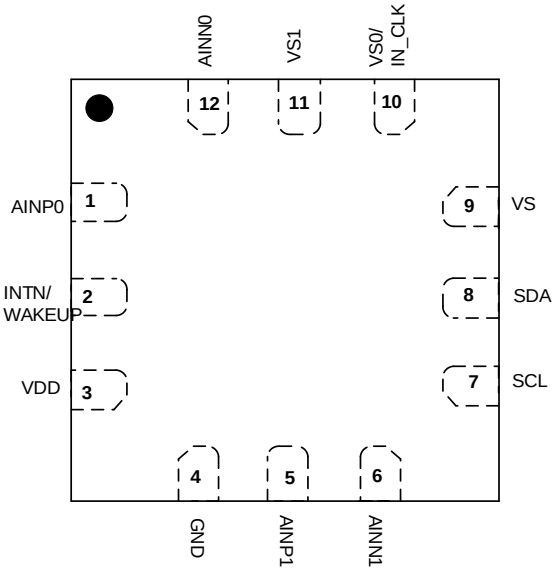
Pin Configuration And Top Mark



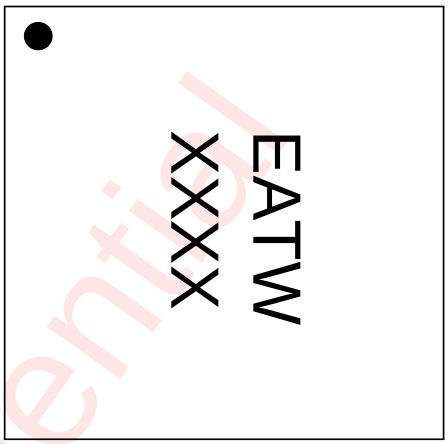
MHGY - AW86862CSR
XXXX XXXX XXXX - Production Tracing Code

Figure 2 AW86862CSR Pin Configuration And Top Mark

AW86862FCR
(Top View)



AW86862FCR Marking
(Top View)



EATW - AW86862FCR
XXXX - Production Tracing Code

Figure 3 AW86862FCR Pin Configuration And Top Mark

Pin Definition

AW86862CSR Pin Definition

NO.	NAME	DESCRIPTION
A1	AINP0	Sensor Channel 0 Positive Input
A2	AINN0	Sensor Channel 0 Negative Input
A3	VS1	VS1 Regulated output
A4	VS0/IN_CLK	VS0 Regulated output/External Clock Input
B1	INTN/WAKEUP	Interrupt/Wakeup
B2	NC	NOT Connect
B3	NC	NOT Connect
B4	VS	VS output, need to be connected to 1μF capacitor
C1	VDD	Power
C2	NC	NOT Connect
C3	NC	NOT Connect
C4	SDA	I²C DATA
D1	GND	Ground
D2	AINP1	Sensor Channel 1 Positive Input
D3	AINN1	Sensor Channel 1 Negative Input
D4	SCL	I²C CLOCK

AW86862FCR Pin Definition

No.	NAME	DESCRIPTION
1	AINP0	Sensor Channel 0 Positive Input
2	INTN/WAKEUP	Interrupt/Wakeup
3	VDD	Power
4	GND	Ground
5	AINP1	Sensor Channel 1 Positive Input
6	AINN1	Sensor Channel 1 Negative Input
7	SCL	I²C CLOCK
8	SDA	I²C DATA
9	VS	VS output, need to be connected to 1μF capacitor
10	VS0/IN_CLK	VS0 Regulated output/External Clock Input
11	VS1	VS1 Regulated output
12	AINN0	Sensor Channel 0 Negative Input

Functional Block Diagram

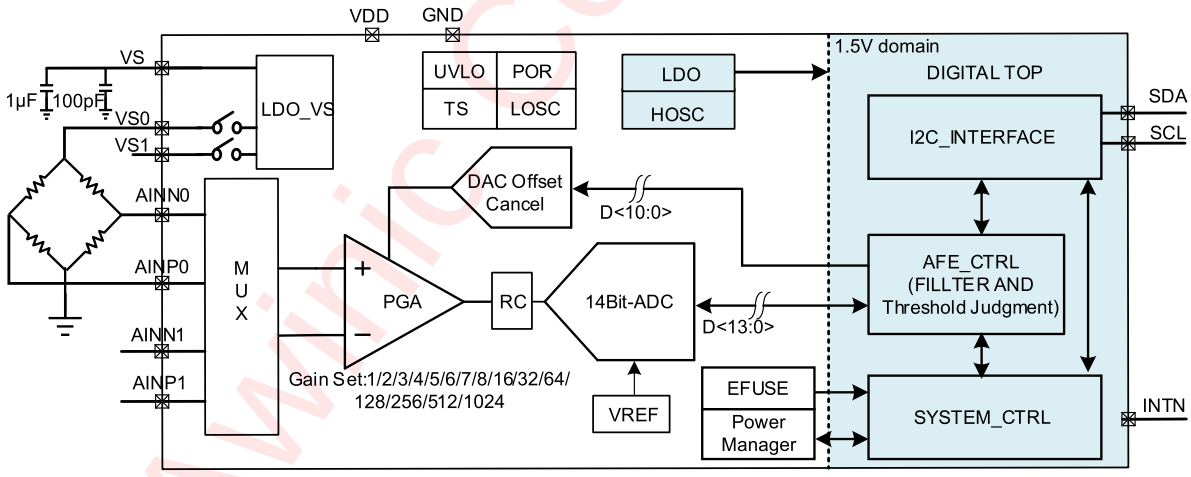


Figure 4 AW86862 Function Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW86862CSR	-40°C～85°C	WLCSP 1.41mm×1.41mm×0.34mm -16B	MHGY	MSL1	ROHS+HF	4500 units/Tape and Reel
AW86862FCR	-40°C～85°C	FCQFN 1.6mm×1.6mm×0.55mm -12L	EATW	MSL1	ROHS+HF	4500 units/Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS	RANGE
Supply voltage range V_{DD}	-0.3V to 5.5V
AINP, AINN,INTN	-0.3V to VDD+0.3V
Ambient Temperature Range	-40°C to 85°C
Junction-to-ambient thermal resistance θ_{JA}	60°C /W
Maximum operating junction temperature T_{JMAX}	165°C
Storage Temperature Range T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD Rating (NOTE 2 3)	
HBM（Human Body Model）	±2kV
CDM(Charge Device Model)	±1.5kV
Latch-up	
Test Condition: JESD78E	+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE 3：Charge Device Model test method: ESDA/JEDEC JS-002-2018.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Analog supply voltage	2.6	3.3	5.5	V
C_{VDD}	Input capacitance		2.2		μF
C_{VS}	VS Decoupling capacitor	1			μF
T_A	Operating free-air temperature range	-40	25	85	°C

Electrical Characteristics

VDD=3.3V, T_A=25°C for typical values (unless otherwise noted)

Parameter		Test Conditions	Min	Typical	Max	Unit
VDD	Analog supply voltage		2.6		5.5	V
VIH	Logic input high level		1.35			V
VIL	Logic input low level				0.4	V
VOL	Logic output low level				0.4	V
VOH	Logic output high level		VDD-0.4			V
ILP	Standby current			4		μA
IACT	Active current			1.4		mA
6MHz HOSC						
FHOSC	HOSC working frequency			6		MHz
RHOSC	HOSC Accuracy		-2		2	%
32kHz LOSC						
FLOSC	LOSC working frequency			32		kHz
RLOSC	LOSC Accuracy		-10		10	%
Temperature Sense						
TR	Range		-40		85	°C
TA	Accuracy		-3		3	°C
14bit ADC						
VADIN	Input voltage		0		VREF	V
VREF	ADC Reference voltage			2.8		V
FADC	Conversion rate			150	150	ksps
PGA(Signal input path)						
VCMI	Common mode input voltage		0.1		VDD-1	V
VDMI	Differential input voltage				VDD/ GPGA	V
GPGA	PGA gain		1		1024	
GE	Gain error			10		%
RIN	Differential input impedance			17		MΩ
ISOch-ch	Channel isolation			80		dB
CMRR	Common mode rejection ratio	1.5 mV_{PP} on SIN, 200Hz		105		dB
PSRR	Power supply rejection ratio	200Hz		50		dB
VOS	Input offset voltage			±1		mV
DAC						
RDAC	Resolution			11		bit

Parameter		Test Conditions	Min	Typical	Max	Unit
MDAC	Monotonic			10		bit
VEOSI	Equivalent offset calibration range		- 614×K(1)		+614×K(1)	mV
VS						
VS	VS output voltage		2.4		3.1	V
C_{VS}	VS Decoupling capacitor		1			μF
UVLO						
VUV	Undervoltage detection voltage			2.3		V
VUVH	Under-voltage protection hysteresis voltage			100		mV
POR						
VPOR	Power-on reset voltage			1.6		V

(1) K=（VS/3）×Kpga，（Kpga =1（Gpga1≤64），Kpga =1/2（Gpga1=128））

I²C Interface

- Only slave mode is supported
- Data bidirectional transmission between master and slaver
- The address is 8 bit, the data bit width is 8 bit
- Support general call, the enable can be configured
- Whether the function of general call responds to ACK can be configured
- Support fast mode and standard mode
- Up to 1MHz communication speed
- The chip device address is 0x6A by default, and the bit is 7bit

Parameter			Fast mode			Super-fast mode			UNIT
No.	Symbol	Name	MIN	TYP	MAX	MIN	TYP	MAX	
1	f_{SCL}	SCL Clock frequency			400			1000	kHz
2	t_{LOW}	SCL Low level Duration	1.3			0.5			μs
3	t_{HIGH}	SCL High level Duration	0.6			0.26			μs
4	t_{RISE}	SCL, SDA rise time			0.3			0.12	μs
5	t_{FALL}	SCL, SDA fall time			0.3			0.12	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			0.3			μs
7	$t_{HD:STA}$	(repeat-start) start condition hold time	0.6			0.3			μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			0.26			μs
9	t_{BUF}	Time between start and stop condition	1.3			0.5			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			0.1			μs
11	$t_{HD:DAT}$	SDA hold time	0			0			ns

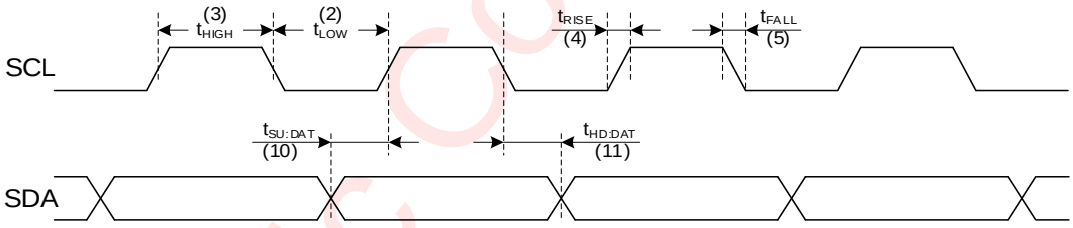


Figure 5 SCL and SDA timing relationships in the data transmission process

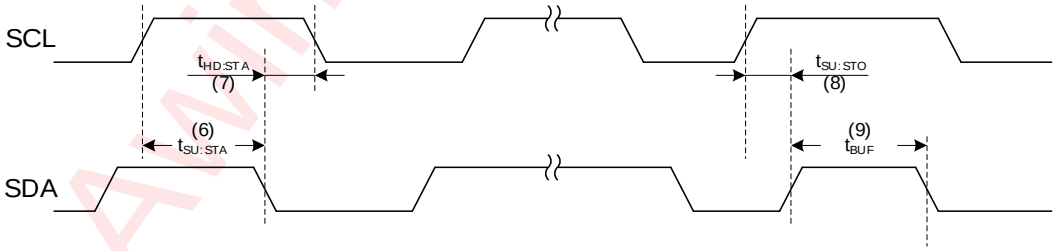


Figure 6 The timing relationship between START and STOP state

WRITE PROCESS

Writing process refers to the master device write data into the slave device. In this process, the transfer direction of the data is always unchanged from the master device to the slave device. All acknowledge bits are transferred by the slave device, in particular, the device as the slave device, the transmission process in accordance with the following steps, as shown in Figure 7.

Master device generates START state. The START state is produced by pulling the data line SDA to a low

level when the clock SCL signal is a high level.

Master device transmits the 7-bits device address of the slave device, followed by the "read / write" flag (flag $R/\overline{W}$ = 0);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device transmits the 8-bit register address to which the first data byte will written;

The slave device asserts an acknowledgment (ACK) bit to confirm the register address is correct;

Master sends 8 bits of data to register which needs to be written;

The slave device asserts an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

If the master device needs to continue transmitting data by sending another pair of data bytes, just need to repeat the sequence from step 6. In the latter case, the targeted register address will have been auto-incremented by the device.

The master device generates the STOP state to end the data transmission.

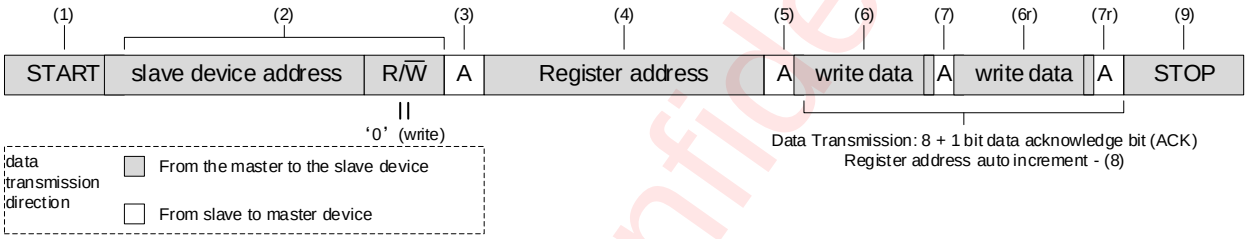


Figure 7 Writing process

READ PROCESS

Reading process refers to the slave device reading data back to the master device. In this process, the direction of data transmission will change. Before and after the change, the master device sends START state and slave address twice, and sends the opposite "read/write" flag. In particular, AW86862 as the slave device, the transmission process carried out by following steps listed in Figure 8.

Master device asserts a start condition;

Master device transmits the 7 bits address of the device, and followed by a "read / write" flag ($R/\overline{W}$ = 0);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device transmits the register address to make sure where the first data byte will read;

The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;

The master device restarts the data transfer process by continuously generating STOP state and START state or a separate Repeated START;

Master sends 7-bits address of the slave device and followed by a read / write flag (flag $R/\overline{W}$ = 1) again;

The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;

Master transmits 8 bits of data to register which needs to be read;

The slave device sends an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

The device automatically increment register address once after sent each acknowledge bit (ACK);

The master device generates the STOP state to end the data transmission.

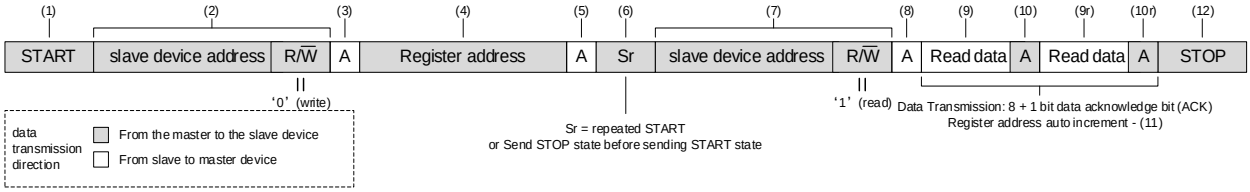


Figure 8 Reading process

Detailed Functional Description

Power On Sequence

The power on sequence of this device is illustrated in the following figure:

Parameter		Value			Unit
Symbol	Name	Min	Typical	Max	
t_{WAIT}	Waiting time for communication with I²C after power on	3			ms
PUR	Instant Power-up rate	1.6			mV/μs
t_{FALL}	Falling time of power supply	0			ms
t_{LOW}	Time between power off and power on	50*			ms

**The t_{LOW} is to make sure the power supply below 100mV after power off.*

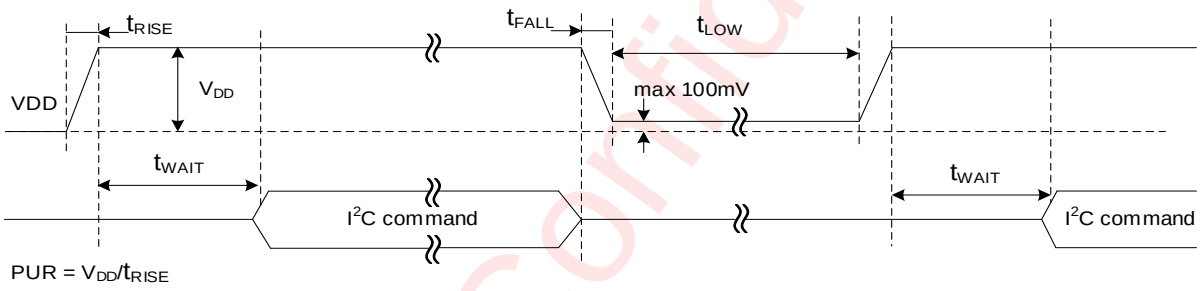


Figure 9 Power On Sequence

Clock

Source of system clock: internal high-speed clock (HOSC) and external pin clock (EOSC, multiplexing VS0 pin). LOSC is the clock of low power consumption module, which is used for SWDT timing wake-up. The osc_clk_sel signal is used to select HOSC or EOSC. The system clock is obtained by frequency division of the selected clock.

Before configuring the clock selection signal, the clock enable should be configured first. The system will give priority to the enabled clock. ADC clock uses the system clock.

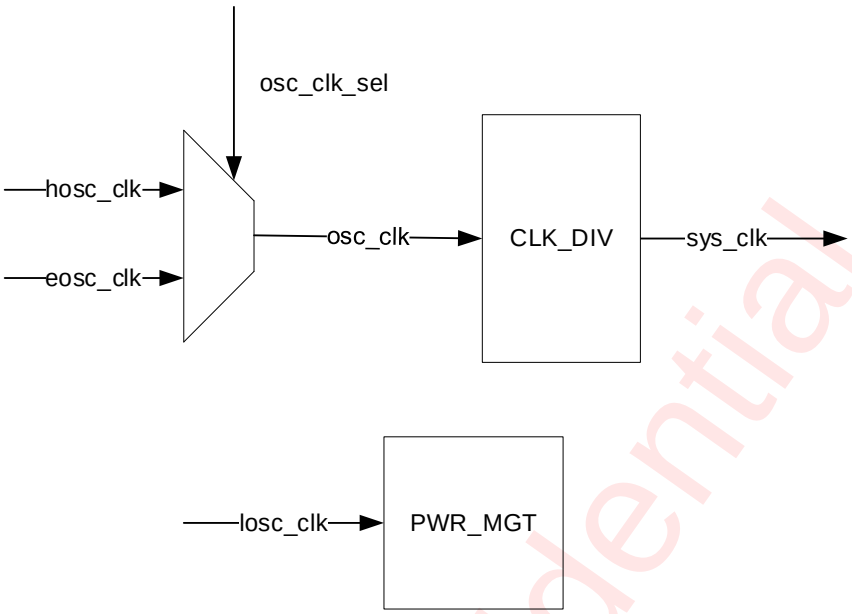


Figure 10 Clock Tree

Reset

AW86862 has three kinds of reset signal: power on reset (POR), whole chip reset (Chip Reset) and soft reset of digital circuit (Soft Reset). Soft Reset resets the system control module and AFE module.

The POR is effective after the chip is powered on, and the reset signal of the system is generated by the control circuit of the power on sequence.

System Control and PAD

Master can configure the way of chip entering low power consumption mode and clearing wake-up request through I²C. After chip is awakened, the wake-up request signal needs to be cleared if the system wants to enter low power consumption mode again. System control module can configure the delay time of automatic trigger AFE in the operation state, and the AFE will be triggered immediately after entering operation state.

The interrupts produced in the operation state, including ADC interrupt, comparator interrupt, algorithm interrupt and so on, can be output through interrupt pin PAD_INTN. The output enable of each interrupt can be configured and the effective level of interrupt output can be configured. PAD_INTN is used as wake-up pin in low power consumption mode and its wake-up effective level can be configured. It should be noted that since the wake-up function multiplexes PAD_INTN, the effective level of the interrupt output should be consistent with the wake-up active level, and the recommended configuration is low level active (default configuration).

PAD_SCL, PAD_SDA, PAD_INTN and PAD_VS0 are multiplexed as IO pins, and its analog characteristics can be configured through registers.

- PAD_SCL is open drain output. There is no pull-up resister or pull-down resister in the chip. The input can be configured with the enable of Schmidt trigger and fast mode. It is the SCL pin of I²C interface.
- PAD_SDA is open drain output. There is no pull-up resister or pull-down resister in the chip. The input can be configured with the enable of Schmidt trigger and fast mode. It is the SDA pin of I²C interface.
- PAD_INTN is open drain output. There is no pull-up resister or pull-down resister in the chip. The input can be configured with the enable of Schmidt trigger and fast mode. It is the interrupt output pin and wake-up pin.
- PAD_VS0 can be configured as open drain or push-pull output. The input can be configured with the enable of Schmidt trigger and fast mode. In normal operation, it is the power supply pin of the sensor, which can be multiplexed as input pin of external clock.

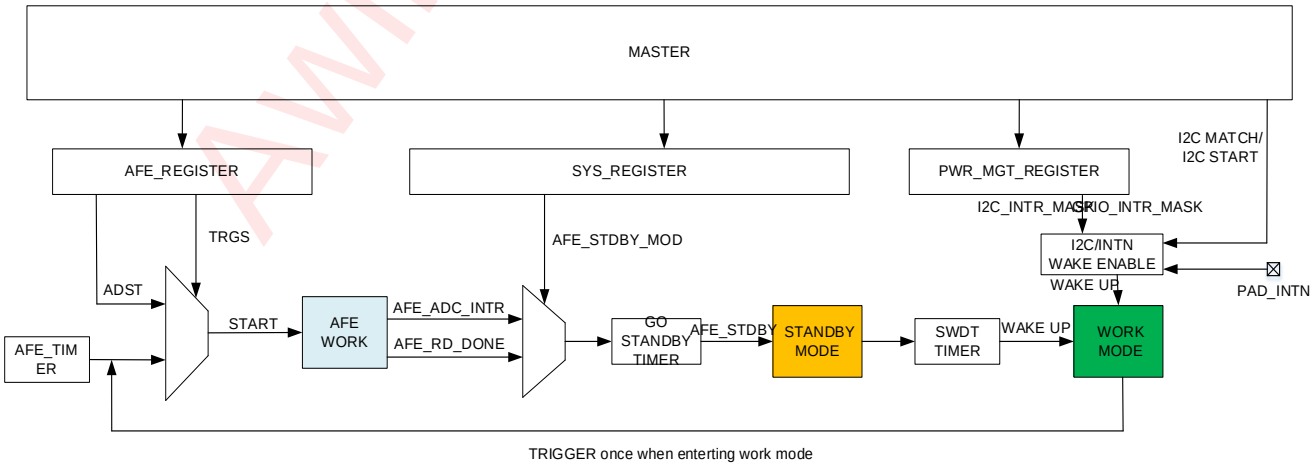


Figure 11 System Workflow

Low Power Consumption and SWDT

When the chip enters low power consumption mode, it can be awakened by SWDT in the 5V domain, or can be configured to wake up through I²C and PAD_INTN. HOSC and VS are automatically turned off, LOSC and digital power supply LDO can choose to turn off.

- Four low-power mode
- Send I²C command to enter low-power mode immediately
- Two ways to enter low-power mode after the delay T1
  - ADC interrupt trigger
  - Trigger after reading AFE data register
- SWDT
  - Working under 5V domain power
  - SWDT still work when turn off LDO
  - The clock source is LOSC, 32kHz
  - 16 bit counter, wake up time T2 configurable

* T1 = GO_STDBY_DLY [23:0]/F_{sys} T2 = LD_SWDT_CNT[15:0]/F_{lclk} = LD_SWDT_CNT[15:0]*31.25 ms
F_{sys} indicates the frequency of system clock(can be configured by HOSC_SEL and CLK_DIV register)
F_{lclk} indicates the frequency of LOSC(32kHz)

Low power consumption mode	**Deep Sleep1 LDO open LOSC open**	**Deep Sleep2 LDO open LOSC close**	**Deep Sleep3 LDO close LOSC open**	**Deep Sleep4 LDO close LOSC close**
HOSC	close	close	close	close
LOSC	open	close	open	close
LDO	open	open	close	close
SWDT	open	close	open	close
AFE module （PGA+ADC+DAC）	Switch is configurable	Switch is configurable	close	close
AFE+SYS configuration	Retain configuration	Retain configuration	Lose configuration	Lose configuration
Awakening conditions	I²C(configurable) PAD_INTN(configurable) SWDT(If LOSC is turned off, SWDT will not work) In Deep Sleep2 and Deep Sleep4 mode, if both I²C wake-up and PAD_INTN wake-up are turned off, LOSC and SWDT wake-up will be forced to open.			

AFE

The AFE module include two PGAs, one 11 bit DAC and one 14-bit ADC

- Provide different configurations for 6 logical channels, including 2 external sensor inputs and 4 internal inputs(VS/GND channels for external impedance self-checking, the single-ended and differential channels are used to measure temperature)
- Provide 6 working modes

- Single conversion mode : Complete a conversion on the designated channel
- Single cycle scan mode : Complete a conversion on all designated channels
- Finite cycle scan mode1 : Each channel switches to the next channel after a specified number of conversions
- Finite cycle scan mode2 : Each channel converts once and then enters the next channel in turn, converting a specified number of times in total
- Infinite scan mode : Continuously execute single-cycle scan mode until software stops A/D conversion
- Burst Mode : Continue on a single designated channel and store the results in FIFO in sequence

➢ Conditions for starting A/D conversion
- Software writes 1 to ADST bit
- Timer trigger (can be configured to turn off enable)

➢ The conversion result can be compared with the specified value, the user can set whether to generate an interruption when matching

➢ Built-in two press detection modules, which can detect the press events of two channels at the same time and generate interruptions.

➢ Built-in Level 2 PGA, The first stage PGA gain coefficient can be configured as 1/16/32/64/128, The second stage PGA gain coefficient can be configured as 1/2/3/4/5/6/7/8

➢ Built-in 11-bit DAC for offset voltage calibration

➢ Built-in 14 bit SAR ADC, up to 150kHz SPS

➢ ADC reference voltage VREF is configurable: 2.4V/2.8V/3.0V/3.1V/AVDD

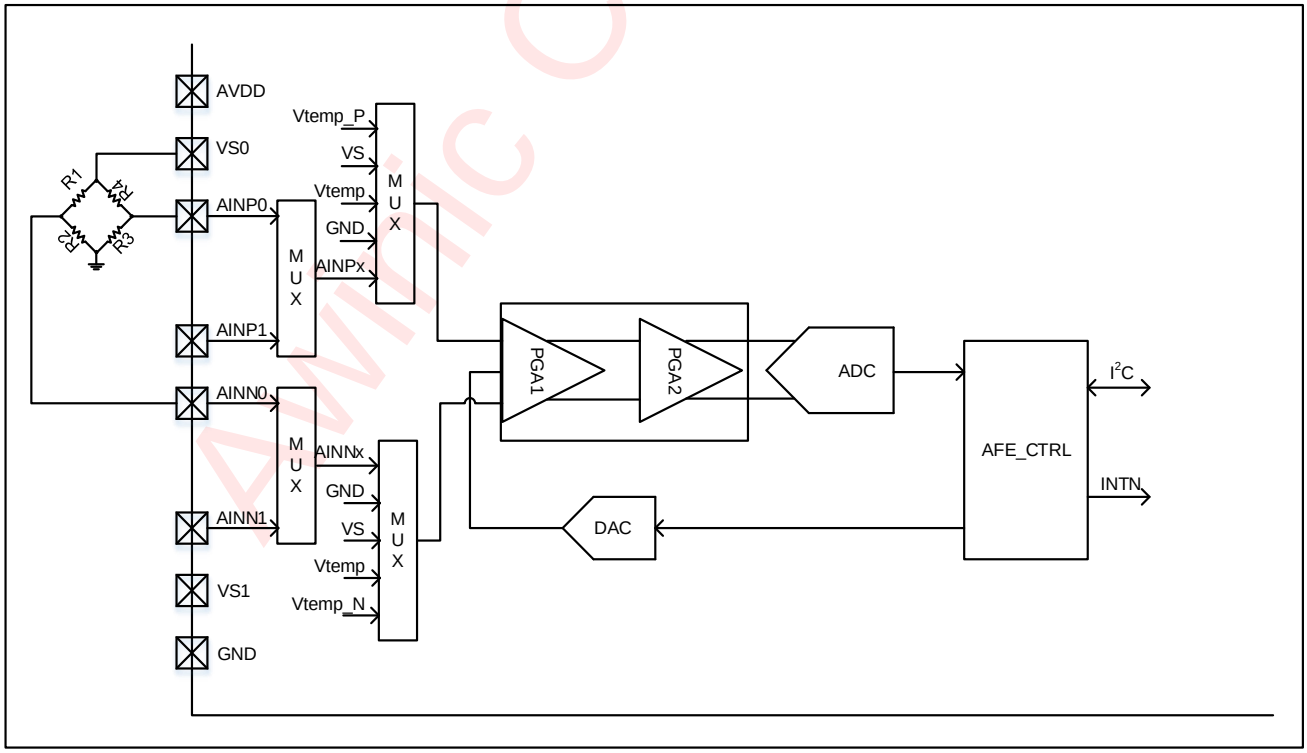


Figure 12 AFE Function Block Diagram

Register Configuration

Register List

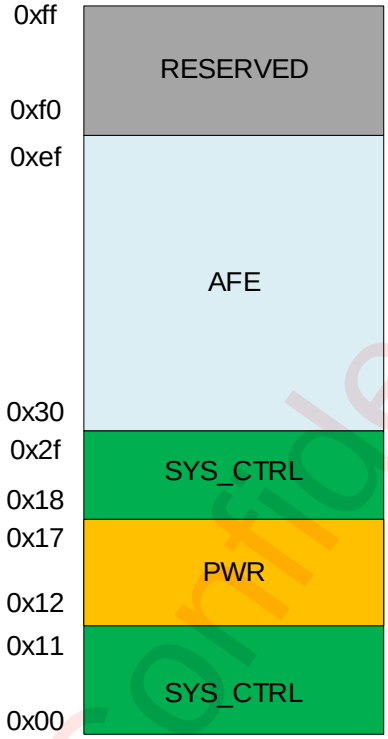


Figure 13 AW86862 Register Address Distribution

SYS

ADDR	NAME	R/W	Description	Default
0x00	**CHIPID**	**RO**	Chip id register	0x62
0x01	**YEAR**	**RO**	Chip year register	0x20
0x02	**MONTH**	**RO**	Chip month register	0x0a
0x03	**DATE**	**RO**	Chip date register	0x25
0x04	**SYS_BLANK**	**R/W**	System blank register	0x55
0x05	**WR_UNLOCK**	**R/W**	System register write unlock register	0x00
0x06	**RESERVED**	**R/W**	Reserved	0x00
0x07	**SYS_ST**	**RO**	System state register	0x01
0x08	**RESERVED**	**RO**	Reserved	0x00
0x09	**RESERVED**	**RO**	Reserved	0x00
0x0a	**RESERVED**	**RO**	Reserved	0x00
0x0b	**RESERVED**	**RO**	Reserved	0x00
0x0c	**RESERVED**	**RO**	Reserved	0x00
0x0d	**RESERVED**	**RO**	Reserved	0x00
0x0e	**RESERVED**	**RO**	Reserved	0x00
0x0f	**DAC_EN_CFG**	**R/W**	DAC enable configuration register	0x00

0x10	**CLK_DIV0**	**R/W**	Clk division data register	0x01
0x11	**CLK_CFG**	**R/W**	Clk configuration register	0x0c
0x18	**GO_STDBU_DLY2**	**R/W**	Go standby delay time register[23:16]	0x03
0x19	**GO_STDBU_DLY1**	**R/W**	Go standby delay time register[15:8]	0xff
0x1a	**GO_STDBU_DLY0**	**R/W**	Go standby delay time register[7:0]	0xff
0x1b	**GO_STDBY_CFG**	**R/W**	Go standby configuration register	0x00
0x1c	**AFE_TIMER2**	**R/W**	Trigger AFE timer register[23:16]	0x03
0x1d	**AFE_TIMER1**	**R/W**	Trigger AFE timer register[15:8]	0xff
0x1e	**AFE_TIMER0**	**R/W**	Trigger AFE timer register[7:0]	0xff
0x1f	**INTR_MASK**	**R/W**	Interrupt mask register	0x01
0x20	**INTR_STAT**	**R/W**	Interrupt state register	0x00
0x21	**ANA_ADJ_CFG**	**R/W**	Analog adjustment configuration register	0x22
0x22	**TEMP_VS_SEL**	**R/W**	Analog temperature and VS mode configuration register	0x01
0x25	**PAD_EN_OD**	**R/W**	Pad open drain enable register	0x03
0x26	**PD_PU_RES**	**R/W**	Pad pull up or pull down resistance	0x00
0x27	**PAD_ADJ**	**R/W**	Pad adjustment configuration register	0x30
0x28	**SR_CTRL**	**R/W**	Pad output delay control register	0x22
0x29	**FAST_CTRL**	**R/W**	Pad input fast enable register	0x00
0x2a	**EN_SCHMITT**	**R/W**	Pad input Schmitt enable register	0x0f
0x2b	**ANA_EN_CFG**	**R/W**	Analog module enable configuration register	0x0b
0x2c	**UVLO_CFG**	**RO**	UVLO module configuration register	0x00
0x2f	**RST_CFG**	**R/W**	Reset configuration register	0x00
PWR				
ADDR	**NAME**	**R/W**	**Description**	**Default**
0x12	**SWDT_CNT1**	**RO**	SWDT counter current number register[15:8]	0x0b
0x13	**SWDT_CNT0**	**RO**	SWDT counter current number register[7:0]	0xff
0x14	**LD_SWDT_CNT1**	**R/W**	SWDT delay counter load data register[15:8]	0x0b
0x15	**LD_SWDT_CNT0**	**R/W**	SWDT delay counter load data register[7:0]	0xff
0x16	**LD_SWDT_CFG**	**R/W**	Load SWDT configuration register	0x00
0x17	**STDBY_CFG**	**R/W**	Standby state configuration register	0x03
AFE				
ADDR	**NAME**	**R/W**	**Description**	**Default**
0x30	**ADCH0CR0_0**	**R/W**	channel 0 ADC configuration register0[7:0]	0x00
0x31	**ADCH0CR0_1**	**R/W**	channel 0 ADC configuration register0[15:8]	0x37
0x32	**ADCH0CR0_2**	**R/W**	channel 0 ADC configuration register0[23:16]	0x10
0x33	**ADCH0CR0_3**	**R/W**	channel 0 ADC configuration register0[31:24]	0x10
0x34	**ADCH0CR1_0**	**R/W**	channel 0 ADC configuration register1[7:0]	0x23
0x35	**ADCH0CR1_1**	**R/W**	channel 0 ADC configuration register1[15:8]	0x00
0x36	**ADCH0CR1_2**	**R/W**	channel 0 ADC configuration register1[23:16]	0x64

0x37	**ADCH0CR1_3**	**R/W**	channel 0 ADC configuration register1[31:24]	0x43
0x38	**DACH0CR_0**	**R/W**	channel 0 DAC configuration register[7:0]	0x00
0x39	**DACH0CR_1**	**R/W**	channel 0 DAC configuration register[15:8]	0x09
0x3A	**DACH0CR_2**	**RO**	channel 0 DAC configuration register[23:16]	0x00
0x3B	**DACH0CR_3**	**RO**	channel 0 DAC configuration register[31:24]	0x00
0x3C	**DACH0DR_0**	**R/W**	channel 0 DAC data register[7:0]	0x00
0x3D	**DACH0DR_1**	**R/W**	channel 0 DAC data register[15:8]	0x00
0x3E	**DACH0DR_2**	**R/W**	channel 0 DAC data register[23:16]	0x00
0x3F	**DACH0DR_3**	**R/W**	channel 0 DAC data register[31:24]	0x00
0x40	**ADCH1CR0_0**	**R/W**	channel 1 ADC configuration register0[7:0]	0x00
0x41	**ADCH1CR0_1**	**R/W**	channel 1 ADC configuration register0[15:8]	0x37
0x42	**ADCH1CR0_2**	**R/W**	channel 1 ADC configuration register0[23:16]	0x10
0x43	**ADCH1CR0_3**	**R/W**	channel 1 ADC configuration register0[31:24]	0x10
0x44	**ADCH1CR1_0**	**R/W**	channel 1 ADC configuration register1[7:0]	0x23
0x45	**ADCH1CR1_1**	**R/W**	channel 1 ADC configuration register1[15:8]	0x00
0x46	**ADCH1CR1_2**	**R/W**	channel 1 ADC configuration register1[23:16]	0x64
0x47	**ADCH1CR1_3**	**R/W**	channel 1 ADC configuration register1[31:24]	0x43
0x48	**DACH1CR_0**	**R/W**	channel 1 DAC configuration register[7:0]	0x00
0x49	**DACH1CR_1**	**R/W**	channel 1 DAC configuration register[15:8]	0x09
0x4A	**DACH1CR_2**	**RO**	channel 1 DAC configuration register[23:16]	0x00
0x4B	**DACH1CR_3**	**RO**	channel 1 DAC configuration register[31:24]	0x00
0x4C	**DACH1DR_0**	**R/W**	channel 1 DAC data register[7:0]	0x00
0x4D	**DACH1DR_1**	**R/W**	channel 1 DAC data register[15:8]	0x00
0x4E	**DACH1DR_2**	**R/W**	channel 1 DAC data register[23:16]	0x00
0x4F	**DACH1DR_3**	**R/W**	channel 1 DAC data register[31:24]	0x00
0x50	**ADCH2CR0_0**	**R/W**	channel 2 ADC configuration register0[7:0]	0x00
0x51	**ADCH2CR0_1**	**R/W**	channel 2 ADC configuration register0[15:8]	0x37
0x52	**ADCH2CR0_2**	**R/W**	channel 2 ADC configuration register0[23:16]	0x10
0x53	**ADCH2CR0_3**	**R/W**	channel 2 ADC configuration register0[31:24]	0x10
0x54	**ADCH2CR1_0**	**R/W**	channel 2 ADC configuration register1[7:0]	0x23
0x55	**ADCH2CR1_1**	**R/W**	channel 2 ADC configuration register1[15:8]	0x00
0x56	**ADCH2CR1_2**	**R/W**	channel 2 ADC configuration register1[23:16]	0x64
0x57	**ADCH2CR1_3**	**R/W**	channel 2 ADC configuration register1[31:24]	0x43
0x58	**DACH2CR_0**	**R/W**	channel 2 DAC configuration register[7:0]	0x00
0x59	**DACH2CR_1**	**R/W**	channel 2 DAC configuration register[15:8]	0x09

0x5A	**DACH2CR_2**	**RO**	channel 2 DAC configuration register[23:16]	0x00
0x5B	**DACH2CR_3**	**RO**	channel 2 DAC configuration register[31:24]	0x00
0x5C	**DACH2DR_0**	**R/W**	channel 2 DAC data register[7:0]	0x00
0x5D	**DACH2DR_1**	**R/W**	channel 2 DAC data register[15:8]	0x00
0x5E	**DACH2DR_2**	**R/W**	channel 2 DAC data register[23:16]	0x00
0x5F	**DACH2DR_3**	**R/W**	channel 2 DAC data register[31:24]	0x00
0x60	**ADCH3CR0_0**	**R/W**	channel 3 ADC configuration register0[7:0]	0x00
0x61	**ADCH3CR0_1**	**R/W**	channel 3 ADC configuration register0[15:8]	0x37
0x62	**ADCH3CR0_2**	**R/W**	channel 3 ADC configuration register0[23:16]	0x10
0x63	**ADCH3CR0_3**	**R/W**	channel 3 ADC configuration register0[31:24]	0x10
0x64	**ADCH3CR1_0**	**R/W**	channel 3 ADC configuration register1[7:0]	0x23
0x65	**ADCH3CR1_1**	**R/W**	channel 3 ADC configuration register1[15:8]	0x00
0x66	**ADCH3CR1_2**	**R/W**	channel 3 ADC configuration register1[23:16]	0x64
0x67	**ADCH3CR1_3**	**R/W**	channel 3 ADC configuration register1[31:24]	0x43
0x68	**DACH3CR_0**	**R/W**	channel 3 DAC configuration register[7:0]	0x00
0x69	**DACH3CR_1**	**R/W**	channel 3 DAC configuration register[15:8]	0x09
0x6A	**DACH3CR_2**	**RO**	channel 3 DAC configuration register[23:16]	0x00
0x6B	**DACH3CR_3**	**RO**	channel 3 DAC configuration register[31:24]	0x00
0x6C	**DACH3DR_0**	**R/W**	channel 3 DAC data register[7:0]	0x00
0x6D	**DACH3DR_1**	**R/W**	channel 3 DAC data register[15:8]	0x00
0x6E	**DACH3DR_2**	**R/W**	channel 3 DAC data register[23:16]	0x00
0x6F	**DACH3DR_3**	**R/W**	channel 3 DAC data register[31:24]	0x00
0x70	**ADCH4CR0_0**	**R/W**	channel 4 ADC configuration register0[7:0]	0x00
0x71	**ADCH4CR0_1**	**R/W**	channel 4 ADC configuration register0[15:8]	0x37
0x72	**ADCH4CR0_2**	**R/W**	channel 4 ADC configuration register0[23:16]	0x10
0x73	**ADCH4CR0_3**	**R/W**	channel 4 ADC configuration register0[31:24]	0x10
0x74	**ADCH4CR1_0**	**R/W**	channel 4 ADC configuration register1[7:0]	0x23
0x75	**ADCH4CR1_1**	**R/W**	channel 4 ADC configuration register1[15:8]	0x00
0x76	**ADCH4CR1_2**	**R/W**	channel 4 ADC configuration register1[23:16]	0x64
0x77	**ADCH4CR1_3**	**R/W**	channel 4 ADC configuration register1[31:24]	0x43
0x78	**DACH4CR_0**	**R/W**	channel 4 DAC configuration register[7:0]	0x00
0x79	**DACH4CR_1**	**R/W**	channel 4 DAC configuration register[15:8]	0x09
0x7A	**DACH4CR_2**	**RO**	channel 4 DAC configuration register[23:16]	0x00
0x7B	**DACH4CR_3**	**RO**	channel 4 DAC configuration register[31:24]	0x00
0x7C	**DACH4DR_0**	**R/W**	channel 4 DAC data register[7:0]	0x00

0x7D	**DACH4DR_1**	**R/W**	channel 4 DAC data register[15:8]	0x00
0x7E	**DACH4DR_2**	**R/W**	channel 4 DAC data register[23:16]	0x00
0x7F	**DACH4DR_3**	**R/W**	channel 4 DAC data register[31:24]	0x00
0x80	**ADCH5CR0_0**	**R/W**	channel 5 ADC configuration register0[7:0]	0x00
0x81	**ADCH5CR0_1**	**R/W**	channel 5 ADC configuration register0[15:8]	0x37
0x82	**ADCH5CR0_2**	**R/W**	channel 5 ADC configuration register0[23:16]	0x10
0x83	**ADCH5CR0_3**	**R/W**	channel 5 ADC configuration register0[31:24]	0x10
0x84	**ADCH5CR1_0**	**R/W**	channel 5 ADC configuration register1[7:0]	0x23
0x85	**ADCH5CR1_1**	**R/W**	channel 5 ADC configuration register1[15:8]	0x00
0x86	**ADCH5CR1_2**	**R/W**	channel 5 ADC configuration register1[23:16]	0x64
0x87	**ADCH5CR1_3**	**R/W**	channel 5 ADC configuration register1[31:24]	0x43
0x88	**DACH5CR_0**	**R/W**	channel 5 DAC configuration register[7:0]	0x00
0x89	**DACH5CR_1**	**R/W**	channel 5 DAC configuration register[15:8]	0x09
0x8A	**DACH5CR_2**	**RO**	channel 5 DAC configuration register[23:16]	0x00
0x8B	**DACH5CR_3**	**RO**	channel 5 DAC configuration register[31:24]	0x00
0x8C	**DACH5DR_0**	**R/W**	channel 5 DAC data register[7:0]	0x00
0x8D	**DACH5DR_1**	**R/W**	channel 5 DAC data register[15:8]	0x00
0x8E	**DACH5DR_2**	**R/W**	channel 5 DAC data register[23:16]	0x00
0x8F	**DACH5DR_3**	**R/W**	channel 5 DAC data register[31:24]	0x00
0xb0	**ADCH0DR_0**	**RO**	channel 0 ADC data register[7:0]	0x00
0xb1	**ADCH0DR_1**	**RO**	channel 0 ADC data register[15:8]	0x00
0xb2	**ADCH1DR_0**	**RO**	channel 1 ADC data register[7:0]	0x00
0xb3	**ADCH1DR_1**	**RO**	channel 1 ADC data register[15:8]	0x00
0xb4	**ADCH2DR_0**	**RO**	channel 2 ADC data register[7:0]	0x00
0xb5	**ADCH2DR_1**	**RO**	channel 2 ADC data register[15:8]	0x00
0xb6	**ADCH3DR_0**	**RO**	channel 3 ADC data register[7:0]	0x00
0xb7	**ADCH3DR_1**	**RO**	channel 3 ADC data register[15:8]	0x00
0xb8	**ADCH4DR_0**	**RO**	channel 4 ADC data register[7:0]	0x00
0xb9	**ADCH4DR_1**	**RO**	channel 4 ADC data register[15:8]	0x00
0xba	**ADCH5DR_0**	**RO**	channel 5 ADC data register[7:0]	0x00
0xbb	**ADCH5DR_1**	**RO**	channel 5 ADC data register[15:8]	0x00
0xc0	**ADMCR_0**	**R/W**	ADC mode control register[7:0]	0x4b
0xc1	**ADMCR_1**	**R/W**	ADC mode control register[15:8]	0x00
0xc2	**ADMCR_2**	**R/W**	ADC mode control register[23:16]	0x0a
0xc3	**ADMCR_3**	**RO**	ADC mode control register[31:24]	0x00

0xc4	**ADTDR_0**	**R/W**	ADC trigger delay control register[7:0]	0xff
0xc5	**ADTDR_1**	**R/W**	ADC trigger delay control register[15:8]	0x01
0xc6	**ADTDR_2**	**RO**	ADC trigger delay control register[23:16]	0x00
0xc7	**ADTDR_3**	**RO**	ADC trigger delay control register[31:24]	0x00
0xc8	**ADSR_0**	**R/W**	ADC status register[7:0]	0x00
0xc9	**ADSR_1**	**RO**	ADC status register[15:8]	0x00
0xca	**ADSR_2**	**RO**	ADC status register[23:16]	0x00
0xcb	**ADSR_3**	**RO**	ADC status register[31:24]	0x00
0xcc	**ADCMPCR0_0**	**R/W**	ADC compare register0[7:0]	0x00
0xcd	**ADCMPCR0_1**	**R/W**	ADC compare register0[15:8]	0x00
0xce	**ADCMPCR0_2**	**R/W**	ADC compare register0[23:16]	0x00
0xcf	**ADCMPCR0_3**	**R/W**	ADC compare register0[31:24]	0x00
0xd0	**ADCMPCR1_0**	**R/W**	ADC compare register1[7:0]	0x00
0xd1	**ADCMPCR1_1**	**R/W**	ADC compare register1[15:8]	0x00
0xd2	**ADCMPCR1_2**	**R/W**	ADC compare register1[23:16]	0x00
0xd3	**ADCMPCR1_3**	**R/W**	ADC compare register1[31:24]	0x00
0xd4	**ADCHEN_0**	**R/W**	channel enable register[7:0]	0x03
0xd5	**ADCHEN_1**	**RO**	channel enable register[15:8]	0x00
0xd6	**ADCHEN_2**	**RO**	channel enable register[23:16]	0x00
0xd7	**ADCHEN_3**	**RO**	channel enable register[31:24]	0x00
0xd8	**DAOSDR_0**	**RO**	DAC offset calibration register[7:0]	0x00
0xd9	**DAOSDR_1**	**RO**	DAC offset calibration register[15:8]	0x00
0xda	**DAOSDR_2**	**R/W**	DAC offset calibration register[23:16]	0x00
0xdb	**DAOSDR_3**	**R/W**	DAC offset calibration register[31:24]	0x00
0xdc	**FACH0CR0**	**R/W**	force algorithm channel 0 compare register0	0x00
0xdd	**FACH0CR1**	**R/W**	force algorithm channel 0 compare register1	0x00
0xde	**FACH0CR2**	**R/W**	force algorithm channel 0 compare register2	0x00
0xdf	**FACH1CR0**	**R/W**	force algorithm channel 1 compare register0	0x00
0xe0	**FACH1CR1**	**R/W**	force algorithm channel 1 compare register1	0x00
0xe1	**FACH1CR2**	**R/W**	force algorithm channel 1 compare register2	0x00
0xe2	**FACH2CR0**	**R/W**	force algorithm channel 2 compare register0	0x00
0xe3	**FACH2CR1**	**R/W**	force algorithm channel 2 compare register1	0x00
0xe4	**FACH2CR2**	**R/W**	force algorithm channel 2 compare register2	0x00
0xe5	**FACH3CR0**	**R/W**	force algorithm channel 3 compare register0	0x00
0xe6	**FACH3CR1**	**R/W**	force algorithm channel 3 compare register1	0x00

0xe7	**FACH3CR2**	**R/W**	force algorithm channel 3 compare register2	0x00
0xe8	**FACHTR0**	**R/W**	force algorithm compare event time register0	0x00
0xe9	**FACHTR1**	**R/W**	force algorithm compare event time register1	0x00
0xea	**FACFTR**	**R/W**	force algorithm compare filter time register	0x00
0xeb	**FACR0**	**R/W**	force algorithm control register0	0x00
0xec	**FACR1**	**R/W**	force algorithm control register1	0x00
0xed	**FAMR**	**R/W**	force algorithm mode register	0x00
0xee	**FASR0**	**RO**	force algorithm status register0	0x00
0xef	**FASR1**	**RO**	force algorithm status register1	0x00

Register Detailed Description

CHIPID: Address(0x00)

Bit	Symbol	R/W	Description	Default
7:0	CHIP_ID_0	RO	chip identification register	0x62

YEAR: Address(0x01)

Bit	Symbol	R/W	Description	Default
7:0	YEAR_0	RO	chip year register	0x20

MONTH: Address(0x02)

Bit	Symbol	R/W	Description	Default
7:0	MONTH_0	RO	chip month register	0x0a

DATE: Address(0x03)

Bit	Symbol	R/W	Description	Default
7:0	DATE_0	RO	chip date register	0x25

SYS_BLANK: Address(0x04)

Bit	Symbol	R/W	Description	Default
7:0	SYS_BLANK_0	RW	system blank register	0x55

WR_UNLOCK: Address(0x05)

Bit	Symbol	R/W	Description	Default
7:1	WR_UNLOCK_0	RW	system register write unlock register, write 0xa5 to unlock the system register(control address range:0x00-0x2F)	0x0
0	UNLOCK_STAT	RW	system write unlocked state 1: unlocked 0:locked	0x0

RESERVED: Address(0x06)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RO	Not used	0x00

SYS_ST: Address(0x07)

Bit	Symbol	R/W	Description	Default
7	EF_LOCK	RO	efuse write lock state 1: locked 0:unlocked	0x0
6	EF_TRIM_FLAG	RO	efuse trim ready flag state 1: ready 0:not ready	0x0
5	EOSC_CLK_OK	RO	EOSC start work flag state 1: ready 0:not ready	0x0
4	HOSC_CLK_OK	RO	HOSC start work flag state 1: working 0:not working	0x0
3	VBG_OK	RO	Vbg ready flag state 1: ready 0:not ready	0x0
2:1	SYS_CTR_STATE	RO	system control current state 00:standby state 01:work state 10:power up state	0x0
0	INIT_STATE	RO	power up initial state 1:work state after power up 0:standby state after power up	0x1

RESERVED: Address(0x08)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RO	Not used	0x00

RESERVED: Address(0x09)

Bit	Symbol	R/W	Description	Default
7	HOSC_SEL	RW	HOSC frequency configuration register 1: 8MHz 0: 6MHz	0x0
6:0	Reserved	RO	Not used	0x00

RESERVED: Address(0x0A)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RO	Not used	0x00

RESERVED: Address(0x0B)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RO	Not used	0x00

RESERVED: Address(0x0C)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RO	Not used	0x00

RESERVED: Address(0x0D)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RO	Not used	0x00

RESERVED: Address(0x0E)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	Reserved	RO	Not used	0x00

DAC_EN_CFG: Address(0x0F)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	Reserved	RO	Not used	0x0
3	SYS_EN_ADC	RW	adc start enable 1: enable 0 :disable	0x0
2	EN_PGA	RW	pga start enable 1: enable 0 :disable	0x0
1	EN_DAC	RW	dac start enable 1: enable 0 :disable	0x0
0	EN_DAC_CODE	RW	dac code standby mode enable 0: 11'd0 when standby mode 1: unchange when standby mode	0x0

CLK_DIV0: Address(0x10)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	CLK_DIV	RW	system clock frequence division counter, no frequence dividion when 0 or 1, $F_{sys}=F_{hosc}$/ CLK_DIV	0x01

CLK_CFG: Address(0x11)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RO	Not used	0
6	OSC_CLK_SEL	RO	current system clock selection, read only 1: external clock 0: hosc clock	0x0
5	OSC_CLK_OK	RO	selection clock ready flag register, read only 1: ready 0: not ready	0x0
4	OSC_SEL	RW	system clock selection configuration 1: external clock 0: hosc clock	0x0
3	EN_EOSC	RW	external clock enable, 1: enable 0: disable	0x1
2	EN_HOSC	RW	hosc clock enable, 1: enable 0: disable	0x1
1:0	Reserved	RO	Not used	0

SWDT_CNT1: Address(0x12)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	SWDT_CNT1_0	R0	The [15:8] bit of swdt counter current value, read only	0x0b

SWDT_CNT0: Address(0x13)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	SWDT_CNT0_0	RO	The [7:0] bit of swdt counter current value, read only	0xff

LD_SWDT_CNT1: Address(0x14)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	LD_SWDT_CNT1_0	RW	The [15:8] bit of swdt counter configuration register LD_SWDT_CNT; swdt wake up time = LD_SWDT_CNT[15:0]/ F_{lclk}	0x0b

LD_SWDT_CNT0: Address(0x15)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	LD_SWDT_CNT0_0	RW	The [7:0] bit of swdt counter configuration register LD_SWDT_CNT; swdt wake up time = LD_SWDT_CNT[15:0]/ F_{lclk}	0xff

LD_SWDT_CFG: Address(0x16)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	LDO_OK	RO	LDO state register, 1 when active	0x0
6	I2C_INTR_MASK	RW	I^2C interrupt mask, 1 enable I^2C wake up	0x0
5	GPIO_INTR_MASK	RW	gpio interrupt mask, 1 enable gpio wake up	0x0
4	EN_VLDOH	RW	LDO high voltage enable, 1:LDO voltage increase 100Mv	0x0
3	CTRL_ACTI	RW	LDO active state output current configuration 1: decrease 35Ma 0: nomal	0x0
2	EN_LOAD	RW	work state load swdt counter enable 0: disable 1: enable	0x0
1	EN_SWDT	RW	work state swdt enable 0: disable 1: enable	0x0
0	EN_SWDT_INTR	RW	swdt interrupt enable 0: disable 1: enable	0x0

STDBY_CFG: Address(0x17)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	PWR_ST_WORK	RO	power manage module state, 1:work state 0:standby state	0x0
6	SWDT_WAKEUP_REQ	RO	swdt wake up request	0x0
5	GPIO_WAKEUP_REQ	RO	gpio wake up request	0x0
4	I2C_WAKEUP_REQ	RO	i^2c wake up request	0x0
3	GPIO_INTR_MOD	RW	gpio interrupt/wake up mode 1: high enable 0:low enable	0x0

2	I2C_INTR_MOD	RW	i²c interrupt/wake up mode 1: i²c start enable 0: not used	0x0
1	STDBY_EN_LOSC	RW	standby state losc enable 0: disable 1: enable	0x1
0	STDBY_EN_LDO	RW	standby state ldo enable, 0: disable 1: enable	0x1

GO_STDBY_DLY2: Address(0x18)

Bit	Symbol	R/W	Description	Default
7:0	GO_STDBY_DLY2_0	RW	The [23:16] bit of afe trigger to go standby delay time counter threshold configuration register GO_STDBY_DLY; go standby delay time = GO_STDBY_DLY [23:0]/F_{sys} ;	0x03

GO_STDBY_DLY1: Address(0x19)

Bit	Symbol	R/W	Description	Default
7:0	GO_STDBY_DLY1_0	RW	The [15:8] bit of afe trigger to go standby delay time counter threshold configuration register GO_STDBY_DLY; go standby delay time = GO_STDBY_DLY [23:0]/F_{sys} ;	0xff

GO_STDBY_DLY0: Address(0x1A)

Bit	Symbol	R/W	Description	Default
7:0	GO_STDBY_DLY0_0	RW	The [7:0] bit of afe trigger to go standby delay time counter threshold configuration register GO_STDBY_DLY; go standby delay time = GO_STDBY_DLY [23:0]/F_{sys} ;	0xff

GO_STDBY_CFG: Address(0x1B)

Bit	Symbol	R/W	Description	Default
7	CMD_STDBY_REQ	RW	Command to go standby. This bit writes 1 to make the system enter standby, and then the hardware automatically clears	0
6:4	Reserved	RO	Not used	0
3	WRCLR_WAKEUP_REQ	RW	i²c write to clear wake up request configuration register, auto clear when go standby 0: disable 1: enable	0x0
2	CLR_WAKEUP_MOD	RW	clear wake up request mode configuration 0: i²c write clear 1: auto clear	0x0
1:0	AFE_STDBY_MOD	RW	afe trigger to go standby mode configuration 01: afe_rd_done trigger(I²C matches the address of the last channel data register enabled) 10: afe_ad_intr trigger(The ADF bit is 1 and ADIE is enabled) 11: afe_rd_done or afe_ad_intr trigger 00: no trigger	0x0

AFE_TIMER2: Address(0x1C)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	AFE_TIMER2_0	RW	The [23:16] bit of afe trigger time counter threshold register configuration AFE_TIMER; It is used to trigger AFE operation under system working state; afe trigger time = AFE_TIMER/F_{sys}	0x03

AFE_TIMER1: Address(0x1D)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	AFE_TIMER1_0	RW	The [15:8] bit of afe trigger time counter threshold configuration register AFE_TIMER; It is used to trigger AFE operation under system working state;afe trigger time = AFE_TIMER/F_{sys}	0xff

AFE_TIMER0: Address(0x1E)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	AFE_TIMER0_0	RW	The [7:0] bit of afe trigger time counter threshold configuration register AFE_TIMER; It is used to trigger AFE operation under system working state; afe trigger time = AFE_TIMER/F_{sys}	0xff

INTR_MASK: Address(0x1F)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	BASE_INTR_MASK	RW	base interrupt mask, enable interrupt output to INTN pin 1: enable output 0: disable output	0x0
6	FORCE_POS_INTR_MASK	RW	force posedge interrupt mask, enable interrupt output to INTN pin 1: enable output 0: disable output	0x0
5	FORCE_NEG_INTR_MASK	RW	force negedge interrupt mask, enable interrupt output to INTN pin 1: enable output 0: disable output	0x0
4	WAKEUP_REQ_MASK	RW	wake up request interrupt mask, enable interrupt output to INTN pin 1: enable output 0: disable output	0x0
3	SWDT_INTR_MASK	RW	swdt interrupt mask, enable interrupt output to INTN pin 1: enable output 0: disable output	0x0
2	AFE_CMP1_INTR_MASK	RW	afe compare 1 interrupt mask, enable interrupt output to INTN pin 1: enable output 0: disable output	0x0
1	AFE_CMP0_INTR_MASK	RW	afe compare 0 interrupt mask, enable interrupt output to INTN pin 1: enable output 0: disable output	0x0

0	AFE_AD_INTR_MASK	RW	afe adc interrupt mask, enable interrupt output to INTN pin 1: enable output 0: disable output	0x1

INTR_STAT: Address(0x20)

Bit	Symbol	R/W	Description	Default
7	BASE_INTR	RO	base line interrupt, write an arbitrary value to the FASR0 or FASR1 registers to clear this bit 1: valid 0: unvalid	0x0
6	FORCE_POS_INTR	RO	force posedge interrupt, write an arbitrary value to the FASR0 or FASR1 registers to clear this bit 1: valid 0: unvalid	0x0
5	FORCE_NEG_INTR	RO	foece negedge interrupt, write an arbitrary value to the FASR0 or FASR1 registers to clear this bit 1: valid 0: unvalid	0x0
4	WAKEUP_REQ	RO	wake up request interrupt, when the bit of CLR_WAKEUP_MOD is 1 , auto clear after waking up , when the bit of CLR_WAKEUP_MOD is 0 , write 1 to WRCLR_WAKEUP_REQ to clear this bit 1: valid 0: unvalid	0x0
3	SWDT_INTR	RO	swdt interrupt, when the bit of CLR_WAKEUP_MOD is 1 , auto clear after waking up , when the bit of CLR_WAKEUP_MOD is 0 , write 1 to WRCLR_WAKEUP_REQ to clear this bit 1: valid 0: unvalid	0x0
2	AFE_CMP1_INTR	RO	afe compare 1 interrupt, write 1 to CMPF1 to clear this bit 1: valid 0: unvalid	0x0
1	AFE_CMP0_INTR	RO	afe compare 0 interrupt, write 1 to CMPF0 to clear this bit 1: valid 0: unvalid	0x0
0	AFE_AD_INTR	RO	afe adc interrupt, write 1 to ADF to clear this bit 1: valid 0: unvalid	0x0

ANA_ADJ_CFG: Address(0x21)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0
6	INTR_LEVEL	RW	interrupt output level selection 1: high level 0: low level	0x0

5:4	VS_ADJ	RW	vs voltage adjustment 00: 2.4V 01: 2.8V 10: 3.0V 11: 3.1V	0x2
3	UVLO_HV_EN	RW	UVLO high voltage control 0: 3.93/4.04 1: 6.40/6.50	0x0
2:0	UVLO_ADJ	RW	uvlo adjustment 000: 1.78/1.87 001: 1.93/2.03 010: 2.30/2.43 011: 2.61/2.70 100: 3.01/3.13 101: 3.57/3.67 110: 3.93/4.04 111: 6.40/6.50 or 3.93/4.04	0x2

ANA_LDO_CUR: Address(0x22)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RO	Not used	0
4	SEL_TEMP	RW	temperature sensor mode selection 0: double port VTEMP_P/VTEMP_N output 1: single port VTEMP output	0x0
3:1	Reserved	RO	Not used	0
0	PJ_VS	RW	vs mode selection 0: CVS discharge 1: CVS don't discharge	0x1

PAD_EN_OD: Address(0x25)

Bit	Symbol	R/W	Description	Default
7:2	Reserved	RO	Not used	0
1	INTN_EN_OD	RW	PAD_INTN open drain enable, 0: disable 1: enable	0x1
0	VS0_EN_OD	RW	PAD_VS0 open drain enable 0: disable 1: enable	0x1

PD_PU_RES: Address(0x26)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0
6:4	PD_RES	RW	PAD_VS0 pull down resistance enable xx0: disable xx1: enable	0x0
3	Reserved	RO	Not used	0
2:0	PU_RES	RW	PAD_VS0 pull up resistance enable xx0: disable xx1: enable	0x0

PAD_ADJ: Address(0x27)

Bit	Symbol	R/W	Description	Default

7	Reserved	RO	Not used	0
6	not use	RW	Not used	0x0
5	PA_SW_PD_0	RW	VS1 analog switch configuration 1: off 0: on	0x1
4	PA_SW_PD_1	RW	VS0 analog switch configuration 1: off 0: on	0x1
3	ADJ_OD_0	RW	SDA, open drain output delay control 0: 20ns 1: 2ns	0x0
2	ADJ_OD_1	RW	SCL open drain output delay control 0: 20ns 1: 2ns	0x0
1	ADJ_OD_2	RW	INTN open drain output delay control 0: 20ns 1: 2ns	0x0
0	Not use	RW	Not used	0x0

SR_CTRL: Address(0x28)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5:4	not use	RW	Not used	0x2
3:2	Reserved	RO	Not used	0
1:0	SR_CTRL_VS0	RW	PAD_VS0 output delay control 00: 110ns 01：21ns 10：9ns 11：3ns	0x2

FAST_CTRL: Address(0x29)

Bit	Symbol	R/W	Description	Default
7	EN_GNR	RW	general call function enable, 0: disable 1: enable	0x0
6	EN_GNR_ACK	RW	general call Acknowledge enable, 0: disable 1: enable	0x0
5:4	GNR_ADDR	RW	general call address low 2 bits selection	0x0
3	FAST_0	RW	SDA input FAST mode enable 0: disable 1: enable,	0x0
2	FAST_1	RW	SCL input FAST mode enable 0: disable 1: enable,	0x0
1	FAST_2	RW	INTN input FAST mode enable 0: disable 1: enable,	0x0
0	FAST_3	RW	VS0 input FAST mode enable 0: disable 1: enable,	0x0

EN_SCHMITT: Address(0x2A)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	Reserved	RO	Not used	0
3	EN_SCHMITT_0	RW	SDA input schmitt mode enable 0: disable 1: enable	0x1
2	EN_SCHMITT_1	RW	SCL input schmitt mode enable 0: disable 1: enable	0x1
1	EN_SCHMITT_2	RW	INTN input schmitt mode enable 0: disable 1: enable	0x1
0	EN_SCHMITT_3	RW	VS0 input schmitt mode enable 0: disable 1: enable	0x1

ANA_EN_CFG: Address(0x2B)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	Reserved	RO	Not used	0
3	EN_BIAS	RW	analog bias module enable, 1: enable 0: disable	0x1
2	EN_VS	RW	vs voltage output enable, 1: enable 0: disable	0x0
1	EN_UVLO	RW	analog uvlo module enable, 1: enable 0: disable	0x1
0	EN_PDR	RW	analog PDR module enable, 1: enable 0: disable	0x1

UVLO_CFG: Address(0x2C)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	Reserved	RO	Not used	0
3	Reserved	RO	Not used	0
2	UVLO_CLR	RW	UVLO clear flag state, write any data to clear UVLO history	0x0
1	UVLO_HIS	RO	UVLO history flag state,1 indicate that low supply voltage is detected in the past，read only	0x0
0	UVLO	RO	UVLO current flag state, 1 indicate that low supply voltage is detected now， read only	0x0

RST_CFG: Address(0x2F)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:5	Reserved	RO	Not used	0
4	CHIP_RST	RW	chip rst configuration register, 1: enable 0: disable	0x0
3:1	Reserved	RO	Not used	0

0	SOFT_RST	RW	soft rst configuration resgister, 1: enable 0: disable	0x0

ADCH0CR0_0: Address(0x30)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RO	Not used	0
6:4	PD_AINP_0	RW	CHx sensor positive input selection (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0b000: sensor0 positive 0b001: sensor1 positive	0x0
3	Reserved	RO	Not used	0
2:0	PD_AINN_0	RW	CHx sensor negative input selection (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0b000: sensor1 negative 0b001: sensor0 negative	0x0

ADCH0CR0_1: Address(0x31)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	RED_OS_0	RW	offset Residual cancellation enable signal (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0: no elimination of residuals 1: elimination of residuals	0x0
6	Reserved	RO	Not used	0
5	PD_DOUBLE_VIN_0	RW	in ADC single-ended mode, turn off the double-ended input (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0: double-ended input 1: single-ended input	0x1
4	EN_DIFF_0	RW	ADC input working mode (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0: single-ended mode 1: differential mode	0x1
3:2	Reserved	RO	Not used	0
1:0	PD_SW_IN_0	RW	VS1-VS0 analog switch control (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0: strobe vs 1: disable	0x3

ADCH0CR0_2: Address(0x32)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:5	Reserved	RO	Not used	0

4:0	SN_MUX_0	RW	negative terminal of DC voltage channel. (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vtemp_n	0x10

ADCH0CR0_3: Address(0x33)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RO	Not used	0
4:0	SP_MUX_0	RW	Positive terminal of DC voltage channel. (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vtemp_p	0x10

ADCH0CR1_0: Address(0x34)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0
6:4	GAIN_PGA1_0	RW	First level of PGA gain selection (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256, do not use when GAIN_PGA2 equals 8 0b110: 256, do not use when GAIN_PGA2 equals 8 0b111: 256, do not use when GAIN_PGA2 equals 8	0x2
3	Reserved	RO	Not used	0
2:0	GAIN_PGA2_0	RW	second level of PGA gain selection (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

ADCH0CR1_1: Address(0x35)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RO	Not used	0
4	Reserved	RW	Not used	0

3	EN_PGA_0	RW	PGA enable switch (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0: disable 1: enable	0x0
2	PD_PGA1_0	RW	First level of PGA enable switch (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 1: disable 0: enable	0x0
1	PD_PGA2_0	RW	second level of PGA enable switch (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 1: disable 0: enable	0x0
0	PD_FILTER_0	RW	turn off the PGA2 filter (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 1: turn off 0: turn on	0x0

ADCH0CR1_2: Address(0x36)

Bit	Symbol	R/W	Description	Default
7:6	VREF_SEL_0	RW	VRP voltage selection (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0b00: 2.4V 0b01: 2.8V 0b10: 3.0V 0b11: 3.1V	0x1
5	VREF_GEN_SEL_0	RW	ADC refrence voltage selection (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0: AVDD 1: VRP	0x1
4	VCM_ADJ_0	RW	PGA output common mode voltage selection (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0: 0.5×AVDD 1: 0.5×AVDD-0.1	0x0
3	Reserved	RO	Not used	0
2:0	ADC_IBIAS_0	RW	ADC BIAS current control (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 2Ma 0b001: 2.5Ma 0b010: 3Ma 0b011: 3.5Ma 0b100: 4Ma 0b101: 4.5Ma 0b110: 5Ma 0b111: 5.5Ma	0x4

ADCH0CR1_3: Address(0x37)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0

6:4	PGA_IBIASE_0	RW	PGA module overall current selection (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 1Ma 0b001: 1.25Ma 0b010: 1.5Ma 0b011: 1.75Ma 0b100: 2Ma 0b101: 2.25Ma 0b110: 2.5Ma 0b111: 2.75Ma	0x4
3:2	Reserved	RO	Not used	0
1:0	BW_FILTER_0	RW	PGA RC filter output frequency selection (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0b00:50kHz 0b01:62.5kHz 0b10:125kHz 0b11:250kHz	0x3

DACH0CR_0: Address(0x38)

Bit	Symbol	R/W	Description	Default
7:1	Reserved	RO	Not used	0
0	VDAC_RANGE_0	RW	DAC calibration offset range (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0: 0.614×VS/3 1: 0.614×(2×VS/9)	0x0

DACH0CR_1: Address(0x39)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	EN_DAC_CAL_0	RW	enable digital DAC calibration loop operation (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0: disable 1: enable	0x0
4	EN_DAC_0	RW	enable calibration offset DAC (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0: disable 1: enable	0x0
3	EN_DAC_VIN_0	RW	turn on DAC negative current input (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0: turn off 1: turn on	0x1
2	DIR_DAC_0	RW	DAC direction select (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0: disable current direction 1: enable current direction	0x0
1	DIR_MODE0_0	RW	DAC direction select (configure channel0, 6 channels in total,the channel offset address is 0x10*channel)	0x0

			0: disable affect offset 1: enable affect offset	
0	DIR_MODE1_0	RW	DAC direction select (configure channel0, 6 channels in total,the channel offset address is 0x10*channel) 0: disable affect offset 1: enable affect offset	0x1

DACH0CR_2: Address(0x3A)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RO	Not used	0

DACH0CR_3: Address(0x3B)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RO	Not used	0

DACH0DR_0: Address(0x3C)

Bit	Symbol	R/W	Description	Default
7:0	DA_L_0	RW	D/A data register[7:0] (configure channel0, 6 channels in total,the channel offset address is 0x10*channel)	0x0

DACH0DR_1: Address(0x3D)

Bit	Symbol	R/W	Description	Default
7:3	Reserved	RO	Not used	0
2:0	DA_H_0	RW	D/A data register[10:8] (configure channel0, 6 channels in total,the channel offset address is 0x10*channel)	0x0

DACH0DR_2: Address(0x3E)

Bit	Symbol	R/W	Description	Default
7:0	AD_OS_L_0	RW	ADC OFFSET residual.directly save the Adc result[7:0],that is, the ADC code, and convert it to two's complement operation when used (configure channel0, 6 channels in total,the channel offset address is 0x10*channel)	0x0

DACH0DR_3: Address(0x3F)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5:0	AD_OS_H_0	RW	ADC OFFSET residual.directly save the Adc result[13:8],that is, the ADC code, and convert it to two's complement operation when used (configure channel0, 6 channels in total,the channel offset address is 0x10*channel)	0x0

ADCH1CR0_0: Address(0x40)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0

6:4	PD_AINP_1	RW	CHx sensor positive input selection (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0b000: sensor0 positive 0b001: sensor1 positive	0x0
3	Reserved	RO	Not used	0
2:0	PD_AINN_1	RW	CHx sensor negative e input selection (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0b000: sensor1 negative 0b001: sensor0 negative	0x0

ADCH1CR0_1: Address(0x41)

Bit	Symbol	R/W	Description	Default
7	RED_OS_1	RW	offset Residual cancellation enable signal (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0: no elimination of residuals 1: elimination of residuals	0x0
6	Reserved	RO	Not used	0
5	PD_DOUBLE_VIN_1	RW	in ADC single-ended mode, turn off the double-ended input (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0: double-ended input 1: single-ended input	0x1
4	EN_DIFF_1	RW	ADC input working mode (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0: single-ended mode 1: differential mode	0x1
3:2	Reserved	RO	Not used	0
1:0	PD_SW_IN_1	RW	VS1-VS0 analog switch control (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0: strobe vs 1: disable	0x3

ADCH1CR0_2: Address(0x42)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RO	Not used	0
4:0	SN_MUX_1	RW	negative terminal of DC voltage channel. (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vtemp_n	0x10

ADCH1CR0_3: Address(0x43)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RO	Not used	0
4:0	SP_MUX_1	RW	Positive terminal of DC voltage channel. (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vtemp_p	0x10

ADCH1CR1_0: Address(0x44)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0
6:4	GAIN_PGA1_1	RW	First level of PGA gain selection (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256, do not use when GAIN_PGA2 equals 8 0b110: 256, do not use when GAIN_PGA2 equals 8 0b111: 256, do not use when GAIN_PGA2 equals 8	0x2
3	Reserved	RO	Not used	0
2:0	GAIN_PGA2_1	RW	second level of PGA gain selection (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

ADCH1CR1_1: Address(0x45)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RO	Not used	0
4	Reserved	RW	Not used	0
3	EN_PGA_1	RW	PGA enable switch (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0: disable 1: enable	0x0
2	PD_PGA1_1	RW	First level of PGA enable switch (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 1: disable 0: enable	0x0

1	PD_PGA2_1	RW	second level of PGA enable switch (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 1: disable 0: enable	0x0
0	PD_FILTER_1	RW	turn off the PGA2 filter (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 1: turn off 0: turn on	0x0

ADCH1CR1_2: Address(0x46)

Bit	Symbol	R/W	Description	Default
7:6	VREF_SEL_1	RW	VRP voltage selection (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0b00: 2.4V 0b01: 2.8V 0b10: 3.0V 0b11: 3.1V	0x1
5	VREF_GEN_SEL_1	RW	ADC refrence voltage selection (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0: AVDD 1: VRP	0x1
4	VCM_ADJ_1	RW	PGA output common mode voltage selection (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0: 0.5×AVDD 1: 0.5×AVDD-0.1	0x0
3	Reserved	RO	Not used	0
2:0	ADC_IBIAS_1	RW	ADC BIAS current control (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 2Ma 0b001: 2.5Ma 0b010: 3Ma 0b011: 3.5Ma 0b100: 4Ma 0b101: 4.5Ma 0b110: 5Ma 0b111: 5.5Ma	0x4

ADCH1CR1_3: Address(0x47)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0

6:4	PGA_IBIASE_1	RW	PGA module overall current selection (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 1Ma 0b001: 1.25Ma 0b010: 1.5Ma 0b011: 1.75Ma 0b100: 2Ma 0b101: 2.25Ma 0b110: 2.5Ma 0b111: 2.75Ma	0x4
3:2	Reserved	RO	Not used	0
1:0	BW_FILTER_1	RW	PGA RC filter output frequency selection (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0b00:50kHz 0b01:62.5kHz 0b10:125kHz 0b11:250kHz	0x3

DACH1CR_0: Address(0x48)

Bit	Symbol	R/W	Description	Default
7:1	Reserved	RO	Not used	0
0	VDAC_RANGE_1	RW	DAC calibration offset range (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0: 0.614×VS/3 1: 0.614×(2×VS/9)	0x0

DACH1CR_1: Address(0x49)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	EN_DAC_CAL_1	RW	enable digital DAC calibration loop operation (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0: disable 1: enable	0x0
4	EN_DAC_1	RW	enable calibration offset DAC (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0: disable 1: enable	0x0
3	EN_DAC_VIN_1	RW	turn on DAC negative current input (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0: turn off 1: turn on	0x1
2	DIR_DAC_1	RW	DAC direction select (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0: disable current direction 1: enable current direction	0x0
1	DIR_MODE0_1	RW	DAC direction select (configure channel1, 6 channels in total,the channel offset address is 0x10*channel)	0x0

			0: disable affect offset 1: enable affect offset	
0	DIR_MODE1_1	RW	DAC direction select (configure channel1, 6 channels in total,the channel offset address is 0x10*channel) 0: disable affect offset 1: enable affect offset	0x1

DACH1CR_2: Address(0x4A)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RO	Not used	0

DACH1CR_3: Address(0x4B)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RO	Not used	0

DACH1DR_0: Address(0x4C)

Bit	Symbol	R/W	Description	Default
7:0	DA_L_1	RW	D/A data register[7:0] (configure channel1, 6 channels in total,the channel offset address is 0x10*channel)	0x0

DACH1DR_1: Address(0x4D)

Bit	Symbol	R/W	Description	Default
7:3	Reserved	RO	Not used	0
2:0	DA_H_1	RW	D/A data register[10:8] (configure channel1, 6 channels in total,the channel offset address is 0x10*channel)	0x0

DACH1DR_2: Address(0x4E)

Bit	Symbol	R/W	Description	Default
7:0	AD_OS_L_1	RW	ADC OFFSET residual.directly save the Adc result[7:0],that is, the ADC code, and convert it to two's complement operation when used (configure channel1, 6 channels in total,the channel offset address is 0x10*channel)	0x0

DACH1DR_3: Address(0x4F)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5:0	AD_OS_H_1	RW	ADC OFFSET residual.directly save the Adc result[13:8],that is, the ADC code, and convert it to two's complement operation when used (configure channel1, 6 channels in total,the channel offset address is 0x10*channel)	0x0

ADCH2CR0_0: Address(0x50)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0

6:4	PD_AINP_2	RW	CHx sensor positive input selection (configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0b000: sensor0 positive 0b001: sensor1 positive	0x0
3	Reserved	RO	Not used	0
2:0	PD_AINN_2	RW	CHx sensor negative input selection (configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0b000: sensor1 negative 0b001: sensor0 negative	0x0

ADCH2CR0_1: Address(0x51)

Bit	Symbol	R/W	Description	Default
7	RED_OS_2	RW	offset Residual cancellation enable signal (configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0: no elimination of residuals 1: elimination of residuals	0x0
6	Reserved	RO	Not used	0
5	PD_DOUBLE_VIN_2	RW	in ADC single-ended mode, turn off the double-ended input (configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0: double-ended input 1: single-ended input	0x1
4	EN_DIFF_2	RW	ADC input working mode (configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0: single-ended mode 1: differential mode	0x1
3:2	Reserved	RO	Not used	0
1:0	PD_SW_IN_2	RW	VS1-VS0 analog switch control (configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0: strobe vs 1: disable	0x3

ADCH2CR0_2: Address(0x52)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RO	Not used	0
4:0	SN_MUX_2	RW	negative terminal of DC voltage channel. (configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vtemp_n	0x10

ADCH2CR0_3: Address(0x53)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RO	Not used	0
4:0	SP_MUX_2	RW	Positive terminal of DC voltage channel. (configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vtemp_p	0x10

ADCH2CR1_0: Address(0x54)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0
6:4	GAIN_PGA1_2	RW	First level of PGA gain selection(configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256, do not use when GAIN_PGA2 equals 8 0b110: 256, do not use when GAIN_PGA2 equals 8 0b111: 256, do not use when GAIN_PGA2 equals 8	0x2
3	Reserved	RO	Not used	0
2:0	GAIN_PGA2_2	RW	second level of PGA gain selection(configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

ADCH2CR1_1: Address(0x55)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RO	Not used	0
4	Reserved	RW	Not used	0
3	EN_PGA_2	RW	PGA enable switch (configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0: disable 1: enable	0x0
2	PD_PGA1_2	RW	First level of PGA enable switch (configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 1: disable 0: enable	0x0

1	PD_PGA2_2	RW	second level of PGA enable switch (configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 1: disable 0: enable	0x0
0	PD_FILTER_2	RW	turn off the PGA2 filter (configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 1: turn off 0: turn on	0x0

ADCH2CR1_2: Address(0x56)

Bit	Symbol	R/W	Description	Default
7:6	VREF_SEL_2	RW	VRP voltage selection(configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0b00: 2.4V 0b01: 2.8V 0b10: 3.0V 0b11: 3.1V	0x1
5	VREF_GEN_SEL_2	RW	ADC refrence voltage selection(configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0: AVDD 1: VRP	0x1
4	VCM_ADJ_2	RW	PGA output common mode voltage selection(configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0: 0.5×AVDD 1: 0.5×AVDD-0.1	0x0
3	Reserved	RO	Not used	0
2:0	ADC_IBIAS_2	RW	ADC BIAS current control(configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 2Ma 0b001: 2.5Ma 0b010: 3Ma 0b011: 3.5Ma 0b100: 4Ma 0b101: 4.5Ma 0b110: 5Ma 0b111: 5.5Ma	0x4

ADCH2CR1_3: Address(0x57)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0

6:4	PGA_IBIASE_2	RW	PGA module overall current selection(configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 1Ma 0b001: 1.25Ma 0b010: 1.5Ma 0b011: 1.75Ma 0b100: 2Ma 0b101: 2.25Ma 0b110: 2.5Ma 0b111: 2.75Ma	0x4
3:2	Reserved	RO	Not used	0
1:0	BW_FILTER_2	RW	PGA RC filter output frequency selection(configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0b00:50kHz 0b01:62.5kHz 0b10:125kHz 0b11:250kHz	0x3

DACH2CR_0: Address(0x58)

Bit	Symbol	R/W	Description	Default
7:1	Reserved	RO	Not used	0
0	VDAC_RANGE_2	RW	DAC calibration offset range (configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0: 0.614×VS/3 1: 0.614×(2×VS/9)	0x0

DACH2CR_1: Address(0x59)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	EN_DAC_CAL_2	RW	enable digital DAC calibration loop operation(configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0: disable 1: enable	0x0
4	EN_DAC_2	RW	enable calibration offset DAC (configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0: disable 1: enable	0x0
3	EN_DAC_VIN_2	RW	turn on DAC negative current input(configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0: turn off 1: turn on	0x1
2	DIR_DAC_2	RW	DAC direction select (configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0: disable current direction 1: enable current direction	0x0

1	DIR_MODE0_2	RW	DAC direction select (configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0: disable affect offset 1: enable affect offset	0x0
0	DIR_MODE1_2	RW	DAC direction select (configure channel2, 6 channels in total,the channel offset address is 0x10*channel) 0: disable affect offset 1: enable affect offset	0x1

DACH2CR_2: Address(0x5A)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RO	Not used	0

DACH2CR_3: Address(0x5B)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RO	Not used	0

DACH2DR_0: Address(0x5C)

Bit	Symbol	R/W	Description	Default
7:0	DA_L_2	RW	D/A data register[7:0] (configure channel2, 6 channels in total,the channel offset address is 0x10*channel)	0x0

DACH2DR_1: Address(0x5D)

Bit	Symbol	R/W	Description	Default
7:3	Reserved	RO	Not used	0
2:0	DA_H_2	RW	D/A data register[10:8] (configure channel2, 6 channels in total,the channel offset address is 0x10*channel)	0x0

DACH2DR_2: Address(0x5E)

Bit	Symbol	R/W	Description	Default
7:0	AD_OS_L_2	RW	ADC OFFSET residual.directly save the Adc result[7:0],that is, the ADC code, and convert it to two's complement operation when used (configure channel2, 6 channels in total,the channel offset address is 0x10*channel)	0x0

DACH2DR_3: Address(0x5F)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5:0	AD_OS_H_2	RW	ADC OFFSET residual.directly save the Adc result[13:8],that is, the ADC code, and convert it to two's complement operation when used (configure channel2, 6 channels in total,the channel offset address is 0x10*channel)	0x0

ADCH3CR0_0: Address(0x60)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0

6:4	PD_AINP_3	RW	CHx sensor positive input selection (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0b000: sensor0 positive 0b001: sensor1 positive	0x0
3	Reserved	RO	Not used	0
2:0	PD_AINN_3	RW	CHx sensor negative input selection (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0b000: sensor1 negative 0b001: sensor0 negative	0x0

ADCH3CR0_1: Address(0x61)

Bit	Symbol	R/W	Description	Default
7	RED_OS_3	RW	offset Residual cancellation enable signal (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0: no elimination of residuals 1: elimination of residuals	0x0
6	Reserved	RO	Not used	0
5	PD_DOUBLE_VIN_3	RW	in ADC single-ended mode, turn off the double-ended input (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0: double-ended input 1: single-ended input	0x1
4	EN_DIFF_3	RW	ADC input working mode (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0: single-ended mode 1: differential mode	0x1
3:2	Reserved	RO	Not used	0
1:0	PD_SW_IN_3	RW	VS1-VS0 analog switch control (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0: strobe vs 1: disable	0x3

ADCH3CR0_2: Address(0x62)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RO	Not used	0
4:0	SN_MUX_3	RW	negative terminal of DC voltage channel. (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vtemp_n	0x10

ADCH3CR0_3: Address(0x63)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RO	Not used	0
4:0	SP_MUX_3	RW	Positive terminal of DC voltage channel. (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vtemp_p	0x10

ADCH3CR1_0: Address(0x64)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0
6:4	GAIN_PGA1_3	RW	First level of PGA gain selection (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256, do not use when GAIN_PGA2 equals 8 0b110: 256, do not use when GAIN_PGA2 equals 8 0b111: 256, do not use when GAIN_PGA2 equals 8	0x2
3	Reserved	RO	Not used	0
2:0	GAIN_PGA2_3	RW	second level of PGA gain selection (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

ADCH3CR1_1: Address(0x65)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RO	Not used	0
4	Reserved	RW	Not used	0
3	EN_PGA_3	RW	PGA enable switch (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0: disable 1: enable	0x0
2	PD_PGA1_3	RW	First level of PGA enable switch (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 1: disable 0: enable	0x0

1	PD_PGA2_3	RW	second level of PGA enable switch (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 1: disable 0: enable	0x0
0	PD_FILTER_3	RW	turn off the PGA2 filter (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 1: turn off 0: turn on	0x0

ADCH3CR1_2: Address(0x66)

Bit	Symbol	R/W	Description	Default
7:6	VREF_SEL_3	RW	VRP voltage selection (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0b00: 2.4V 0b01: 2.8V 0b10: 3.0V 0b11: 3.1V	0x1
5	VREF_GEN_SEL_3	RW	ADC refrence voltage selection (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0: AVDD 1: VRP	0x1
4	VCM_ADJ_3	RW	PGA output common mode voltage selection (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0: 0.5×AVDD 1: 0.5×AVDD-0.1	0x0
3	Reserved	RO	Not used	0
2:0	ADC_IBIAS_3	RW	ADC BIAS current control (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 2Ma 0b001: 2.5Ma 0b010: 3Ma 0b011: 3.5Ma 0b100: 4Ma 0b101: 4.5Ma 0b110: 5Ma 0b111: 5.5Ma	0x4

ADCH3CR1_3: Address(0x67)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0

6:4	PGA_IBIASE_3	RW	PGA module overall current selection (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 1Ma 0b001: 1.25Ma 0b010: 1.5Ma 0b011: 1.75Ma 0b100: 2Ma 0b101: 2.25Ma 0b110: 2.5Ma 0b111: 2.75Ma	0x4
3:2	Reserved	RO	Not used	0
1:0	BW_FILTER_3	RW	PGA RC filter output frequency selection (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0b00:50kHz 0b01:62.5kHz 0b10:125kHz 0b11:250kHz	0x3

DACH3CR_0: Address(0x68)

Bit	Symbol	R/W	Description	Default
7:1	Reserved	RO	Not used	0
0	VDAC_RANGE_3	RW	DAC calibration offset range (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0: 0.614×VS/3 1: 0.614×(2×VS/9)	0x0

DACH3CR_1: Address(0x69)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	EN_DAC_CAL_3	RW	enable digital DAC calibration loop operation (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0: disable 1: enable	0x0
4	EN_DAC_3	RW	enable calibration offset DAC (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0: disable 1: enable	0x0
3	EN_DAC_VIN_3	RW	turn on DAC negative current input (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0: turn off 1: turn on	0x1
2	DIR_DAC_3	RW	DAC direction select (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0: disable current direction 1: enable current direction	0x0
1	DIR_MODE0_3	RW	DAC direction select (configure channel3, 6 channels in total,the channel offset address is 0x10*channel)	0x0

			0: disable affect offset 1: enable affect offset	
0	DIR_MODE1_3	RW	DAC direction select (configure channel3, 6 channels in total,the channel offset address is 0x10*channel) 0: disable affect offset 1: enable affect offset	0x1

DACH3CR_2: Address(0x6A)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RO	Not used	0

DACH3CR_3: Address(0x6B)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RO	Not used	0

DACH3DR_0: Address(0x6C)

Bit	Symbol	R/W	Description	Default
7:0	DA_L_3	RW	D/A data register[7:0] (configure channel3, 6 channels in total,the channel offset address is 0x10*channel)	0x0

DACH3DR_1: Address(0x6D)

Bit	Symbol	R/W	Description	Default
7:3	Reserved	RO	Not used	0
2:0	DA_H_3	RW	D/A data register[10:8] (configure channel3, 6 channels in total,the channel offset address is 0x10*channel)	0x0

DACH3DR_2: Address(0x6E)

Bit	Symbol	R/W	Description	Default
7:0	AD_OS_L_3	RW	ADC OFFSET residual.directly save the Adc result[7:0],that is, the ADC code, and convert it to two's complement operation when used (configure channel3, 6 channels in total,the channel offset address is 0x10*channel)	0x0

DACH3DR_3: Address(0x6F)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5:0	AD_OS_H_3	RW	ADC OFFSET residual.directly save the Adc result[13:8],that is, the ADC code, and convert it to two's complement operation when used (configure channel3, 6 channels in total,the channel offset address is 0x10*channel)	0x0

ADCH4CR0_0: Address(0x70)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0

6:4	PD_AINP_4	RW	CHx sensor positive input selection (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0b000: sensor0 positive 0b001: sensor1 positive	0x0
3	Reserved	RO	Not used	0
2:0	PD_AINN_4	RW	CHx sensor negative input selection (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0b000: sensor1 negative 0b001: sensor0 negative	0x0

ADCH4CR0_1: Address(0x71)

Bit	Symbol	R/W	Description	Default
7	RED_OS_4	RW	offset Residual cancellation enable signal (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0: no elimination of residuals 1: elimination of residuals	0x0
6	Reserved	RO	Not used	0
5	PD_DOUBLE_VIN_4	RW	in ADC single-ended mode, turn off the double-ended input (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0: double-ended input 1: single-ended input	0x1
4	EN_DIFF_4	RW	ADC input working mode (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0: single-ended mode 1: differential mode	0x1
3:2	Reserved	RO	Not used	0
1:0	PD_SW_IN_4	RW	VS1-VS0 analog switch control (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0: strobe vs 1: disable	0x3

ADCH4CR0_2: Address(0x72)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RO	Not used	0
4:0	SN_MUX_4	RW	negative terminal of DC voltage channel. (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vtemp_n	0x10

ADCH4CR0_3: Address(0x73)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RO	Not used	0
4:0	SP_MUX_4	RW	Positive terminal of DC voltage channel. (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vtemp_p	0x10

ADCH4CR1_0: Address(0x74)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0
6:4	GAIN_PGA1_4	RW	First level of PGA gain selection (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256, do not use when GAIN_PGA2 equals 8 0b110: 256, do not use when GAIN_PGA2 equals 8 0b111: 256, do not use when GAIN_PGA2 equals 8	0x2
3	Reserved	RO	Not used	0
2:0	GAIN_PGA2_4	RW	second level of PGA gain selection (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

ADCH4CR1_1: Address(0x75)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RO	Not used	0
4	Reserved	RW	Not used	0
3	EN_PGA_4	RW	PGA enable switch (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0: disable 1: enable	0x0
2	PD_PGA1_4	RW	First level of PGA enable switch (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 1: disable 0: enable	0x0

1	PD_PGA2_4	RW	second level of PGA enable switch (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 1: disable 0: enable	0x0
0	PD_FILTER_4	RW	turn off the PGA2 filter (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 1: turn off 0: turn on	0x0

ADCH4CR1_2: Address(0x76)

Bit	Symbol	R/W	Description	Default
7:6	VREF_SEL_4	RW	VRP voltage selection (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0b00: 2.4V 0b01: 2.8V 0b10: 3.0V 0b11: 3.1V	0x1
5	VREF_GEN_SEL_4	RW	ADC refrence voltage selection (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0: AVDD 1: VRP	0x1
4	VCM_ADJ_4	RW	PGA output common mode voltage selection (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0: 0.5×AVDD 1: 0.5×AVDD-0.1	0x0
3	Reserved	RO	Not used	0
2:0	ADC_IBIAS_4	RW	ADC BIAS current control (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 2Ma 0b001: 2.5Ma 0b010: 3Ma 0b011: 3.5Ma 0b100: 4Ma 0b101: 4.5Ma 0b110: 5Ma 0b111: 5.5Ma	0x4

ADCH4CR1_3: Address(0x77)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0

6:4	PGA_IBIASE_4	RW	PGA module overall current selection(configure channel4, 8 channels in total,the channel offset address is 0x10 *channel +0x7) 0b000: 1Ma 0b001: 1.25Ma 0b010: 1.5Ma 0b011: 1.75Ma 0b100: 2Ma 0b101: 2.25Ma 0b110: 2.5Ma 0b111: 2.75Ma	0x4
3:2	Reserved	RO	Not used	0
1:0	BW_FILTER_4	RW	PGA RC filter output frequency selection (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0b00:50kHz 0b01:62.5kHz 0b10:125kHz 0b11:250kHz	0x3

DACH4CR_0: Address(0x78)

Bit	Symbol	R/W	Description	Default
7:1	Reserved	RO	Not used	0
0	VDAC_RANGE_4	RW	DAC calibration offset range (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0: 0.614×VS/3 1: 0.614×(2×VS/9)	0x0

DACH4CR_1: Address(0x79)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	0
5	EN_DAC_CAL_4	RW	enable digital DAC calibration loop operation (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0: disable 1: enable	0x0
4	EN_DAC_4	RW	enable calibration offset DAC (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0: disable 1: enable	0x0
3	EN_DAC_VIN_4	RW	turn on DAC negative current input (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0: turn off 1: turn on	0x1
2	DIR_DAC_4	RW	DAC direction select (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0: disable current direction 1: enable current direction	0x0

1	DIR_MODE0_4	RW	DAC direction select (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0: disable affect offset 1: enable affect offset	0x0
0	DIR_MODE1_4	RW	DAC direction select (configure channel4, 6 channels in total,the channel offset address is 0x10*channel) 0: disable affect offset 1: enable affect offset	0x1

DACH4CR_2: Address(0x7A)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RO	Not used	0

DACH4CR_3: Address(0x7B)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RO	Not used	0

DACH4DR_0: Address(0x7C)

Bit	Symbol	R/W	Description	Default
7:0	DA_L_4	RW	D/A data register[7:0] (configure channel4, 6 channels in total,the channel offset address is 0x10*channel)	0x0

DACH4DR_1: Address(0x7D)

Bit	Symbol	R/W	Description	Default
7:3	Reserved	RO	Not used	0
2:0	DA_H_4	RW	D/A data register[10:8] (configure channel4, 6 channels in total,the channel offset address is 0x10*channel)	0x0

DACH4DR_2: Address(0x7E)

Bit	Symbol	R/W	Description	Default
7:0	AD_OS_L_4	RW	ADC OFFSET residual.directly save the Adc result[7:0],that is, the ADC code, and convert it to two's complement operation when used (configure channel4, 6 channels in total,the channel offset address is 0x10*channel)	0x0

DACH4DR_3: Address(0x7F)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5:0	AD_OS_H_4	RW	ADC OFFSET residual.directly save the Adc result[13:8],that is, the ADC code, and convert it to two's complement operation when used (configure channel4, 6 channels in total,the channel offset address is 0x10*channel)	0x0

ADCH5CR0_0: Address(0x80)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0

6:4	PD_AINP_5	RW	CHx sensor positive input selection (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0b000: sensor0 positive 0b001: sensor1 positive	0x0
3	Reserved	RO	Not used	0
2:0	PD_AINN_5	RW	CHx sensor negative input selection (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0b000: sensor1 negative 0b001: sensor0 negative	0x0

ADCH5CR0_1: Address(0x81)

Bit	Symbol	R/W	Description	Default
7	RED_OS_5	RW	offset Residual cancellation enable signal (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0: no elimination of residuals 1: elimination of residuals	0x0
6	Reserved	RO	Not used	0
5	PD_DOUBLE_VIN_5	RW	in ADC single-ended mode, turn off the double-ended input (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0: double-ended input 1: single-ended input	0x1
4	EN_DIFF_5	RW	ADC input working mode (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0: single-ended mode 1: differential mode	0x1
3:2	Reserved	RO	Not used	0
1:0	PD_SW_IN_5	RW	VS1-VS0 analog switch control (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0: strobe vs 1: disable	0x3

ADCH5CR0_2: Address(0x82)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RO	Not used	0
4:0	SN_MUX_5	RW	negative terminal of DC voltage channel. (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0b10000: sensor negative input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vtemp_n	0x10

ADCH5CR0_3: Address(0x83)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RO	Not used	0
4:0	SP_MUX_5	RW	Positive terminal of DC voltage channel. (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0b10000: sensor positive input channel 0b01000: vtemp 0b00100: vs 0b00010: gnd 0b00001: vtemp_p	0x10

ADCH5CR1_0: Address(0x84)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0
6:4	GAIN_PGA1_5	RW	First level of PGA gain selection (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 1 0b001: 16 0b010: 32 0b011: 64 0b100: 128 0b101: 256, do not use when GAIN_PGA2 equals 8 0b110: 256, do not use when GAIN_PGA2 equals 8 0b111: 256, do not use when GAIN_PGA2 equals 8	0x2
3	Reserved	RO	Not used	0
2:0	GAIN_PGA2_5	RW	second level of PGA gain selection (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 5 0b101: 6 0b110: 7 0b111: 8	0x3

ADCH5CR1_1: Address(0x85)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RO	Not used	0
4	Reserved	RW	Not used	0
3	EN_PGA_5	RW	PGA enable switch (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0: disable 1: enable	0x0
2	PD_PGA1_5	RW	First level of PGA enable switch (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 1: disable 0: enable	0x0

1	PD_PGA2_5	RW	second level of PGA enable switch (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 1: disable 0: enable	0x0
0	PD_FILTER_5	RW	turn off the PGA2 filter (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 1: turn off 0: turn on	0x0

ADCH5CR1_2: Address(0x86)

Bit	Symbol	R/W	Description	Default
7:6	VREF_SEL_5	RW	VRP voltage selection (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0b00: 2.4V 0b01: 2.8V 0b10: 3.0V 0b11: 3.1V	0x1
5	VREF_GEN_SEL_5	RW	ADC refrence voltage selection (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0: AVDD 1: VRP	0x1
4	VCM_ADJ_5	RW	PGA output common mode voltage selection (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0: 0.5×AVDD 1: 0.5×AVDD-0.1	0x0
3	Reserved	RO	Not used	0
2:0	ADC_IBIAS_5	RW	ADC BIAS current control (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0b000: 2Ma 0b001: 2.5Ma 0b010: 3Ma 0b011: 3.5Ma 0b100: 4Ma 0b101: 4.5Ma 0b110: 5Ma 0b111: 5.5Ma	0x4

ADCH5CR1_3: Address(0x87)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0

6:4	PGA_IBIASE_5	RW	PGA module overall current selection(configure channel5, 8 channels in total,the channel offset address is 0x10 *channel +0x7) 0b000: 1Ma 0b001: 1.25Ma 0b010: 1.5Ma 0b011: 1.75Ma 0b100: 2Ma 0b101: 2.25Ma 0b110: 2.5Ma 0b111: 2.75Ma	0x4
3:2	Reserved	RO	Not used	0
1:0	BW_FILTER_5	RW	PGA RC filter output frequency selection (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0b00:50kHz 0b01:62.5kHz 0b10:125kHz 0b11:250kHz	0x3

DACH5CR_0: Address(0x88)

Bit	Symbol	R/W	Description	Default
7:1	Reserved	RO	Not used	0
0	VDAC_RANGE_5	RW	DAC calibration offset range (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0: 0.614×VS/3 1: 0.614×(2×VS/9)	0x0

DACH5CR_1: Address(0x89)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	EN_DAC_CAL_5	RW	enable digital DAC calibration loop operation (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0: disable 1: enable	0x0
4	EN_DAC_5	RW	enable calibration offset DAC (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0: disable 1: enable	0x0
3	EN_DAC_VIN_5	RW	turn on DAC negative current input (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0: turn off 1: turn on	0x1
2	DIR_DAC_5	RW	DAC direction select (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0: disable current direction 1: enable current direction	0x0

1	DIR_MODE0_5	RW	DAC direction select (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0: disable affect offset 1: enable affect offset	0x0
0	DIR_MODE1_5	RW	DAC direction select (configure channel5, 6 channels in total,the channel offset address is 0x10*channel) 0: disable affect offset 1: enable affect offset	0x1

DACH5CR_2: Address(0x8A)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RO	Not used	0

DACH5CR_3: Address(0x8B)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RO	Not used	0

DACH5DR_0: Address(0x8C)

Bit	Symbol	R/W	Description	Default
7:0	DA_L_5	RW	D/A data register[7:0] (configure channel5, 6 channels in total,the channel offset address is 0x10*channel)	0x0

DACH5DR_1: Address(0x8D)

Bit	Symbol	R/W	Description	Default
7:3	Reserved	RO	Not used	0
2:0	DA_H_5	RW	D/A data register[10:8] (configure channel5, 6 channels in total,the channel offset address is 0x10*channel)	0x0

DACH5DR_2: Address(0x8E)

Bit	Symbol	R/W	Description	Default
7:0	AD_OS_L_5	RW	ADC OFFSET residual.directly save the Adc result[7:0],that is, the ADC code, and convert it to two's complement operation when used (configure channel5, 6 channels in total,the channel offset address is 0x10*channel)	0x0

DACH5DR_3: Address(0x8F)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5:0	AD_OS_H_5	RW	ADC OFFSET residual.directly save the Adc result[13:8],that is, the ADC code, and convert it to two's complement operation when used (configure channel5, 6 channels in total,the channel offset address is 0x10*channel)	0x0

ADCH0DR_0: Address(0xb0)

Bit	Symbol	R/W	Description	Default

7:0	ADDR_0_L	RO	channel 0 value[7:0](configure channel0, 6 channels in total,the channel offset address is 2*channel) single-end input voltage = (ADDR_×[13:0] / 2^{14}) × Vref/GAIN_PGA , differential input voltage = ((ADDR_×[13:0] -0x2000)/ 2^{13}) × Vref/GAIN_PGA	0x0

ADCH0DR_1: Address(0xb1)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RO	Not used	0
5:0	ADDR_0_H	RO	channel 0 value[13:8](configure channel0, 6 channels in total,the channel offset address is 2*channel) single-end input voltage = (ADDR_×[13:0] / 2^{14}) × Vref/GAIN_PGA , differential input voltage = ((ADDR_×[13:0] -0x2000)/ 2^{13})× Vref/GAIN_PGA	0x0

ADCH1DR_0: Address(0xb2)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	ADDR_1_L	RO	channel 1 value[7:0](configure channel1, 6 channels in total,the channel offset address is 2*channel) single-end input voltage = (ADDR_×[13:0] / 2^{14})× Vref/GAIN_PGA , differential input voltage = ((ADDR_×[13:0] -0x2000)/ 2^{13}) × Vref/GAIN_PGA	0x0

ADCH1DR_1: Address(0xb3)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RO	Not used	0
5:0	ADDR_1_H	RO	channel 1 value[13:8](configure channel1, 6 channels in total,the channel offset address is 2*channel) single-end input voltage = (ADDR_×[13:0] / 2^{14}) × Vref/GAIN_PGA , differential input voltage = ((ADDR_×[13:0] -0x2000)/ 2^{13}) × Vref/GAIN_PGA	0x0

ADCH2DR_0: Address(0xb4)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	ADDR_2_L	RO	channel 2 value[7:0](configure channel2, 6 channels in total,the channel offset address is 2*channel) single-end input voltage = (ADDR_×[13:0] / 2^{14}) × Vref/GAIN_PGA , differential input voltage = ((ADDR_×[13:0] -0x2000)/ 2^{13}) × Vref/GAIN_PGA	0x0

ADCH2DR_1: Address(0xb5)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RO	Not used	0
5:0	ADDR_2_H	RO	channel 2 value[13:8](configure channel2, 6 channels in total,the channel offset address is 2*channel)	0x0

			single-end input voltage = (ADDR_×[13:0] / 2^{14}) × Vref/GAIN_PGA , differential input voltage = ((ADDR_×[13:0] -0x2000)/ 2^{13}) × Vref/GAIN_PGA	

ADCH3DR_0: Address(0xb6)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	ADDR_3_L	RO	channel 3 value[7:0](configure channel3, 6 channels in total,the channel offset address is 2*channel) single-end input voltage = (ADDR_×[13:0] / 2^{14}) × Vref/GAIN_PGA , differential input voltage = ((ADDR_×[13:0] -0x2000)/ 2^{13}) × Vref/GAIN_PGA	0x0

ADCH3DR_1: Address(0xb7)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RO	Not used	0
5:0	ADDR_3_H	RO	channel 3 value[13:8](configure channel3, 6 channels in total,the channel offset address is 2*channel) single-end input voltage = (ADDR_×[13:0] / 2^{14}) × Vref/GAIN_PGA , differential input voltage = ((ADDR_×[13:0] -0x2000)/ 2^{13}) × Vref/GAIN_PGA	0x0

ADCH4DR_0: Address(0xb8)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	ADDR_4_L	RO	channel 4 value[7:0](configure channel4, 6 channels in total,the channel offset address is 2*channel) single-end input voltage = (ADDR_×[13:0] / 2^{14}) × Vref/GAIN_PGA , differential input voltage = ((ADDR_×[13:0] -0x2000)/ 2^{13}) × Vref/GAIN_PGA	0x0

ADCH4DR_1: Address(0xb9)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RO	Not used	0
5:0	ADDR_4_H	RO	channel 4 value[13:8](configure channel4, 6 channels in total,the channel offset address is 2*channel) single-end input voltage = (ADDR_×[13:0] / 2^{14}) × Vref/GAIN_PGA , differential input voltage = ((ADDR_×[13:0] -0x2000)/ 2^{13}) × Vref/GAIN_PGA	0x0

ADCH5DR_0: Address(0xba)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	ADDR_5_L	RO	channel 5 value[7:0](configure channel5, 6 channels in total,the channel offset address is 2*channel) single-end input voltage = (ADDR_×[13:0] / 2^{14}) × Vref/GAIN_PGA , differential input voltage = ((ADDR_×[13:0] -0x2000)/ 2^{13}) × Vref/GAIN_PGA	0x0

ADCH5DR_1: Address(0xbb)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RO	Not used	0
5:0	ADDR_5_H	RO	channel 5 value[13:8](configure channel5, 6 channels in total,the channel offset address is 2*channel) single-end input voltage = (ADDR_×[13:0] / 2^{14}) × Vref/GAIN_PGA , differential input voltage = ((ADDR_×[13:0] -0x2000)/ 2^{13}) × Vref/GAIN_PGA	0x0

ADMCR_0: Address(0xc0)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RO	Not used	0
6	EN_AD_RST	RW	reset ADC after changing channel 0: disable 1: enable	0x1
5	TRGS	RW	A/D conversion trigger source selection. 0: AD conversion is initiated by software ADST 1: AD conversion is initiated by AFE timer or wakeup request or software ADST	0x0
4:2	ADMD	RW	A/D conversion operation mode control. 0b000: single conversion 0b001: single cycle scan 0b010: finite scan mode1 0b011: finite scan mode2 0b100: infinite scan mode 0b101: burst mode note : software clears ADST bit before changing operation mode	0x2
1	ADIE	RW	A/D interrupt enable control. 0: disable 1: enable	0x1
0	EN_ADC	RW	A/D enable conrol. 0: disable 1: enable	0x1

ADMCR_1: Address(0xc1)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	Reserved	RO	Not used	0
3	ADST	RW	A/D conversion begins. ADST will be automatically cleared by hardware after conversion in Single conversion mode and single-cycle scan mode. A/D conversion will continue until the software writes 0 or the system resets in the wireless periodic scan mode. 0: end 1: start	0x0
2:0	Reserved	RO	Not used	0

ADMCR_2: Address(0xc2)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	UNVLD_RS	RW	finite scan mode1 for invalid conversions 0b0000: 0 0b0001: 1 0b0010: 2 0b0011: 3 0b0100: 4 0b0101: 5 0b0110: 6 0b0111: 7 0b1000: 8 0b1001: 9 0b1010: 10 0b1011: 11 0b1100: 12 0b1101: 13 0b1110: 14 0b1111: 15	0x0
3	CAL_S	RW	Selection of operation mode in finite period scan mode 0: direc averaging 1: remove the maximum and minimum values before averaging	0x1
2:0	VALID_NS	RW	finite scan mode2 effective conversions 0b000: 2 0b001: 4 0b010: 8 0b011: 16 0b100: 32 0b101: 64 0b110: 64 0b111: 64 note: in finite period scanning 1 and 2 mode,the ADC data register value is the average of the number of valid conversions	0x2

ADMCR_3: Address(0xc3)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	Reserved	RO	Not used	0

ADTDR_0: Address(0xc4)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	ADC_WAIT_L	RW	ADC startup wait time(unit is clock period) , preferably greater T= (ADC_WAIT+1) × ADC_CLK	0xff

ADTDR_1: Address(0xc5)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:1	Reserved	RO	Not used	0

0	ADC_WAIT_H	RW	ADC startup wait time(unit is clock period) , preferably greater T=(ADC_WAIT+1)× ADC_CLK	0x1

ADTDR_2: Address(0xc6)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	Reserved	RO	Not used	0

ADTDR_3: Address(0xc7)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	Reserved	RO	Not used	0

ADSR_0: Address(0xc8)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RO	Not used	0
6:4	CHANNEL	RO	current conversion channel it indicates the channel being converted when BUSY=1 and indicates the channel to be converted next time when BUSY =1	0x0
3	BUSY	RO	busy/free 0: free 1: busy	0x0
2	CMPF1	RW	comparison flag1.write 1 to clear this flag. 0: no match 1: match	0x0
1	CMPF0	RW	comparison flag0.write 1 to clear this flag. 0: no match 1: match	0x0
0	ADF	RW	end of conversion flag it indicate the end of A/D conversion.write 1 to clear this flag. ADF is set under the following three conditions: 1,at the end of the single conversion mode 2,conversion ends for all specified channels in single scan mode and continuous scan mode 3,in burst mode, the FIFO stores more than 32 conversion result values 0: conversion 1: conversion finish	0x0

ADSR_1: Address(0xc9)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	Reserved	RO	Not used	0

ADSR_2: Address(0xca)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	Reserved	RO	Not used	0

ADSR_3: Address(0xcb)				
Bit	**Symbol**	**R/W**	**Description**	**Default**

7:0	Reserved	RO	Not used	0

ADCMPCR0_0: Address(0xcc)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RO	Not used	0
6:4	CMPCH0	RW	channel selection 0b000: channel 0 0b001: channel 1 0b010: channel2 0b011: channel3 0b100: channel4 0b101: channel5	0x0
3	CMPALLCHEN0	RW	channel selection 0: single channel 1: all channels	0x0
2	CMPCOND0	RW	Compare condition 0: less than 1: greater than or equal	0x0
1	CMPIE0	RW	Compare interrupt enable 0: disable comparator interrupt 1: enable comparator interrupt	0x0
0	CMPEN0	RW	Compare enable 0: disable comparator 1: enable comparator	0x0

ADCMPCR0_1: Address(0xcd)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RO	Not used	0
5:0	CMPMATCNT0	RW	Compare matches internal counter is incremented by 1 when the conversion value of the specified channel matches the comparision condition CMPCOND[2], the hardware will set the CMPFx when the counter reaches the set value	0x0

ADCMPCR0_2: Address(0xce)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	CMPD0_L	RW	Compare values[7:0] this 14-bit value will be compared with the conversion result of the specified channel	0x0

ADCMPCR0_3: Address(0xcf)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RO	Not used	0
5:0	CMPD0_H	RW	Compare values[13:8] this 14-bit value will be compared with the conversion result of the specified channel	0x0

ADCMPCR1_0: Address(0xd0)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RO	Not used	0

6:4	CMPCH1	RW	channel selection 0b000: channel 0 0b001: channel 1 0b010: channel2 0b011: channel3 0b100: channel4 0b101: channel5	0x0
3	CMPALLCHEN1	RW	channel selection 0: single channel 1: all channels	0x0
2	CMPCOND1	RW	Compare condition 0: less than 1: greater than or equal	0x0
1	CMPIE1	RW	Compare interrupt enable 0: disable comparator interrupt 1: enable comparator interrupt	0x0
0	CMPEN1	RW	Compare enable 0: disable comparator 1: enable comparator	0x0

ADCMPCR1_1: Address(0xd1)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5:0	CMPMATCNT1	RW	Compare matches internal counter is incremented by 1 when the conversion value of the specified channel matches the comparision condition CMPCOND[2], the hardware will set the CMPFx when the counter reaches the set value	0x0

ADCMPCR1_2: Address(0xd2)

Bit	Symbol	R/W	Description	Default
7:0	CMPD1_L	RW	Compare values[7:0] this 14-bit value will be compared with the conversion result of the specified channel	0x0

ADCMPCR1_3: Address(0xd3)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5:0	CMPD1_H	RW	Compare values[13:8] this 14-bit value will be compared with the conversion result of the specified channel	0x0

ADCHEN_0: Address(0xd4)

Bit	Symbol	R/W	Description	Default
7:0	ADCH_EN	RW	Channel enable 0: disable 1: enable	0x3

ADCHEN_1: Address(0xd5)

Bit	Symbol	R/W	Description	Default

7:0	Reserved	RO	Not used	0

ADCHEN_2: Address(0xd6)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RO	Not used	0

ADCHEN_3: Address(0xd7)

Bit	Symbol	R/W	Description	Default
7:0	Reserved	RO	Not used	0

DAOSDR_0: Address(0xd8)

Bit	Symbol	R/W	Description	Default
7:0	DAOS_L	RO	DAC offset calibration result	0x0

DAOSDR_1: Address(0xd9)

Bit	Symbol	R/W	Description	Default
7:3	Reserved	RO	Not used	0
2:0	DAOS_H	RO	DAC offset calibration result	0x0

DAOSDR_2: Address(0xda)

Bit	Symbol	R/W	Description	Default
7:2	AD_OS_L	RW	AD offset calibration residual	0x0
1	Reserved	RO	Not used	0
0	DAOSUP	RW	DAC offset calibration update channel DACHDR register enable 0: disable 1: enable	0x0

DAOSDR_3: Address(0xdb)

Bit	Symbol	R/W	Description	Default
7:0	AD_OS_H	RW	AD offset calibration residual	0x0

FACH0CR0: Address(0xdc)

Bit	Symbol	R/W	Description	Default
7:0	comp_hi_ch0_l	RW	Force algorithm channel 0 compare high threshold [7:0]	0x0

FACH0CR1: Address(0xdd)

Bit	Symbol	R/W	Description	Default
7:4	comp_lo_ch0_l	RW	Force algorithm channel 0 compare low threshold [3:0]	0x0
3:0	comp_hi_ch0_h	RW	Force algorithm channel 0 compare high threshold [11:8]	0x0

FACH0CR2: Address(0xde)

Bit	Symbol	R/W	Description	Default
7:0	comp_lo_ch0_h	RW	Force algorithm channel 0 compare low threshold [11:4]	0x0

FACH1CR0: Address(0xdf)

Bit	Symbol	R/W	Description	Default
7:0	comp_hi_ch1_l	RW	Force algorithm channel 1 compare high threshold [7:0]	0x0

FACH1CR1: Address(0xe0)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	comp_lo_ch1_l	RW	Force algorithm channel 1 compare low threshold [3:0]	0x0
3:0	comp_hi_ch1_h	RW	Force algorithm channel 1 compare high threshold [11:8]	0x0

FACH1CR2: Address(0xe1)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	comp_lo_ch1_h	RW	Force algorithm channel 1 compare low threshold [11:4]	0x0

FACH2CR0: Address(0xe2)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	comp_hi_ch2_l	RW	Force algorithm channel 2 compare high threshold [7:0]	0x0

FACH2CR1: Address(0xe3)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	comp_lo_ch2_l	RW	Force algorithm channel 2 compare low threshold [3:0]	0x0
3:0	comp_hi_ch2_h	RW	Force algorithm channel 2 compare high threshold [11:8]	0x0

FACH2CR2: Address(0xe4)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	comp_lo_ch2_h	RW	Force algorithm channel 2 compare low threshold [11:4]	0x0

FACH3CR0: Address(0xe5)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	comp_hi_ch3_l	RW	Force algorithm channel 3 compare high threshold [7:0]	0x0

FACH3CR1: Address(0xe6)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	comp_lo_ch3_l	RW	Force algorithm channel 3 compare low threshold [3:0]	0x0
3:0	comp_hi_ch3_h	RW	Force algorithm channel 3 compare high threshold [11:8]	0x0

FACH3CR2: Address(0xe7)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	comp_lo_ch3_h	RW	Force algorithm channel 3 compare low threshold [11:4]	0x0

FACHTR0: Address(0xe8)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	h_tcnt_l	RW	Force algorithm compare event time count[7:0]	0x0

FACHTR1: Address(0xe9)				
Bit	**Symbol**	**R/W**	**Description**	**Default**

7:0	h_tcnt_h	RW	Force algorithm compare event time count[15:8]	0x0

FACFTR: Address(0xea)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	f_tcnt	RW	Force algorithm compare filter time count	0x0

FACR0: Address(0xeb)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RO	Not used	0
5	en_alg0	RW	Force algorithm module 0 enable 0: disable 1: enable	0x0
4	base_mode0	RW	Force algorithm module 0 base trigger method 0: negedge trigger 1: posedge trigger	0x0
3:2	Reserved	RO	Not used	0
1:0	en_ch0	RW	Force algorithm module 0 channel select 0b00: channel 0 0b01: channel 1 0b10: channel 2 0b11: channel 3	0x0

FACR1: Address(0xec)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RO	Not used	0
5	en_alg1	RW	Force algorithm module 1 enable 0: disable 1: enable	0x0
4	base_mode1	RW	Force algorithm module 1 base trigger method 0: negedge trigger 1: posedge trigger	0x0
3:2	Reserved	RO	Not used	0
1:0	en_ch1	RW	Force algorithm module 1 channel select 0b00: channel 0 0b01: channel 1 0b10: channel 2 0b11: channel 3	0x0

FAMR: Address(0xed)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:1	Reserved	RO	Not used	0
0	en_force_abs	WO	Force algorithm negative pressing enable, raw data take absolute value, write only 0: disable 1: enable	0x0

FASR0: Address(0xee)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RO	Not used	0

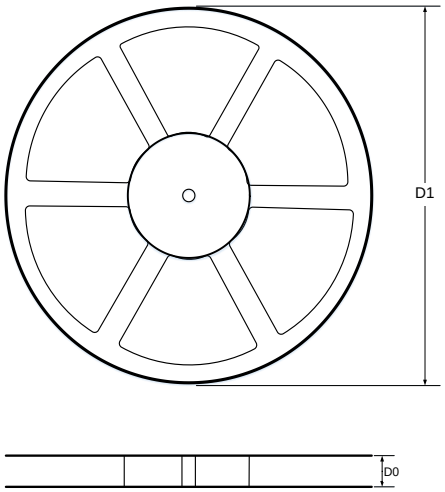
6	cur_event_force1	WC	Force algorithm module 1 current force event status 0: unvalid 1: valid	0x0
5	his_event_force_pos1	WC	Force algorithm module 1 history force event posedge status 0: unvalid 1: valid	0x0
4	his_event_force_neg1	WC	Force algorithm module 1 history force event negedge status 0: unvalid 1: valid	0x0
3	Reserved	RO	Not used	0
2	cur_event_force0	WC	Force algorithm module 0 current force event status 0: unvalid 1: valid	0x0
1	his_event_force_pos0	WC	Force algorithm module 0 history force event posedge status 0: unvalid 1: valid	0x0
0	his_event_force_neg0	WC	Force algorithm module 0 history force event negedge status 0: unvalid 1: valid (write this register to clear all of history event)	0x0

FASR1: Address(0xef)

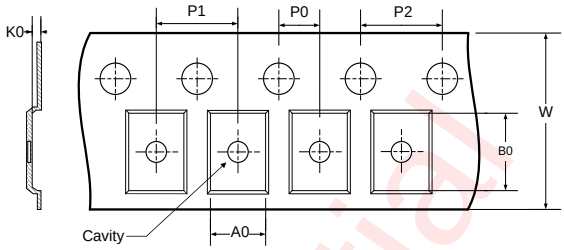
Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	cur_event_base1	WC	Force algorithm module 1 current base event status 0: unvalid 1: valid	0x0
4	his_event_base1	WC	Force algorithm module 1 history base event status 0: unvalid 1: valid	0x0
3:2	Reserved	RO	Not used	0
1	cur_event_base0	WC	Force algorithm module 0 current base event status 0: unvalid 1: valid	0x0
0	his_event_base0	WC	Force algorithm module 0 history base event status 0: unvalid 1: valid (write this register to clear all of history event)	0x0

Tape And Reel Information

REEL DIMENSIONS

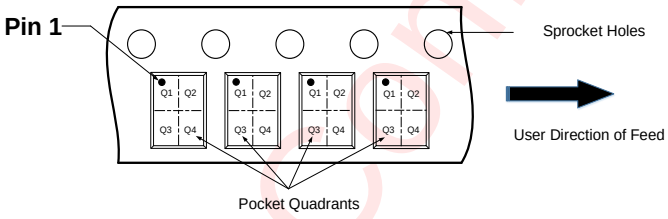


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



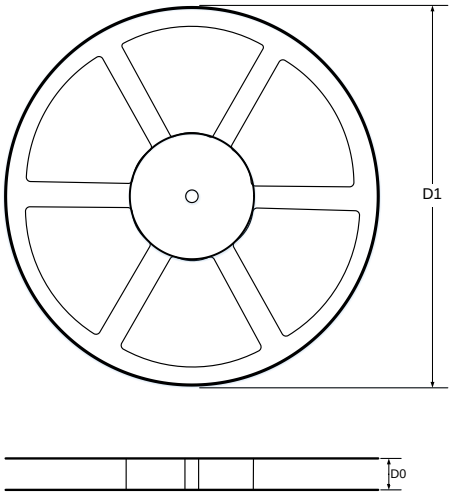
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	1.58	1.58	0.45	2.00	4.00	4.00	8.00	Q1

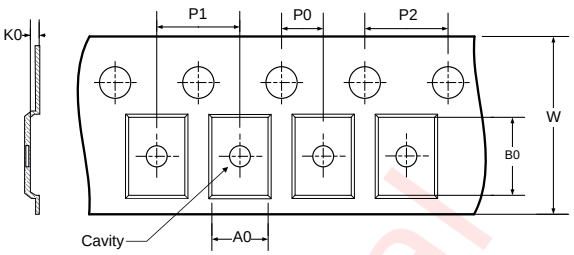
All dimensions are nominal

AW86862CSR Tape And Reel Information

REEL DIMENSIONS

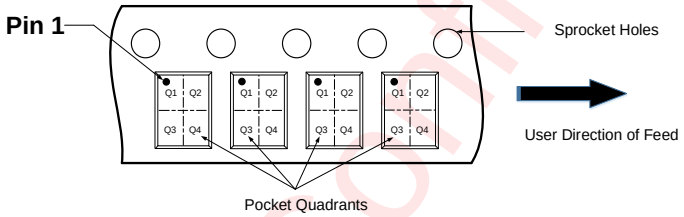


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



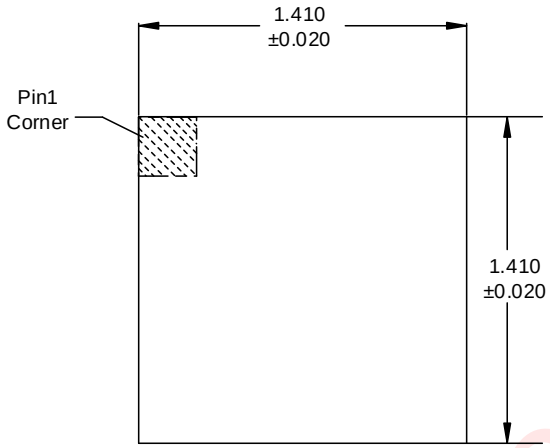
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
180	8.4	1.81	1.81	0.76	2	4	4	8	Q1

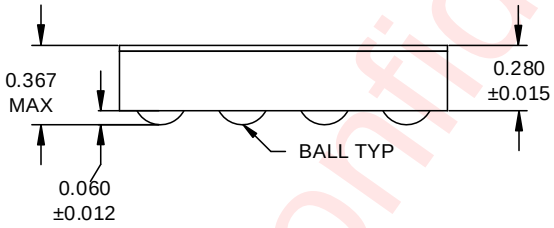
All dimensions are nominal

AW86862FCR Tape And Reel Information

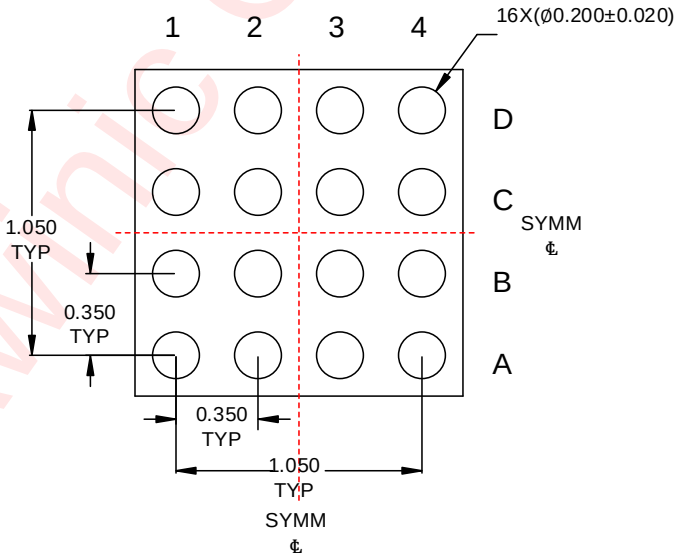
Package Description



Top View



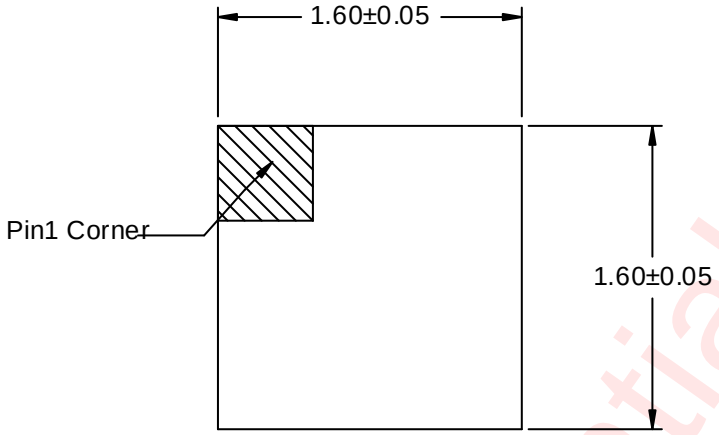
Side View



Bottom View

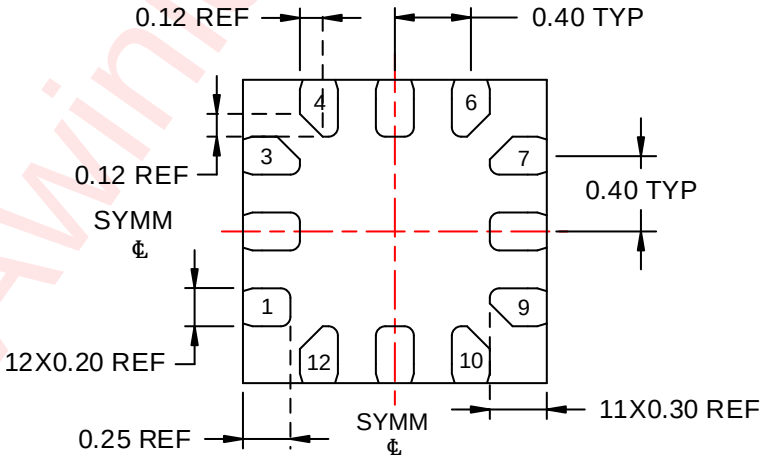
Unit：mm

AW86862CSR Package Description



Top View

Side View

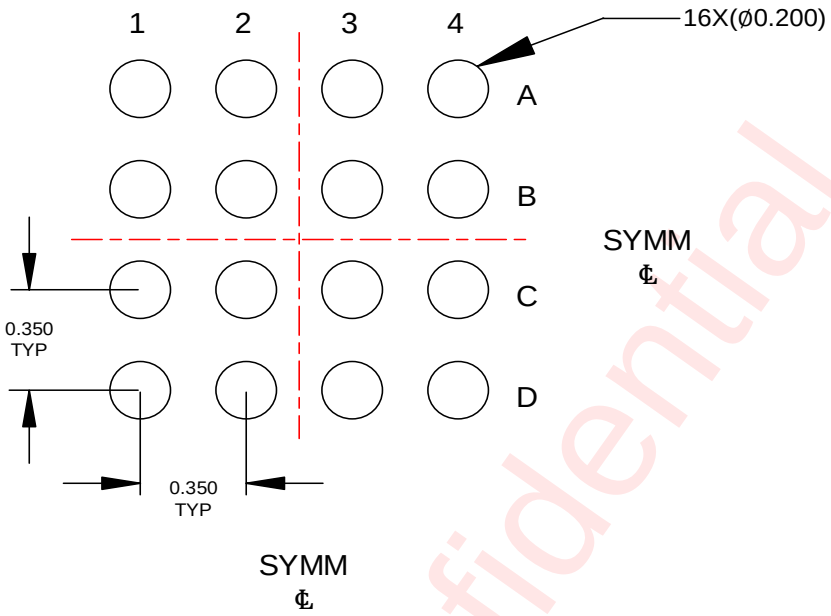


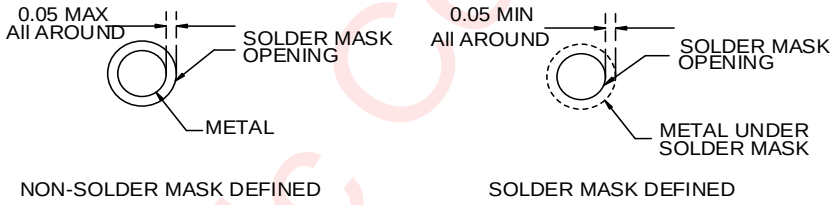
Bottom View

Unit:mm

AW86862FCR Package Description

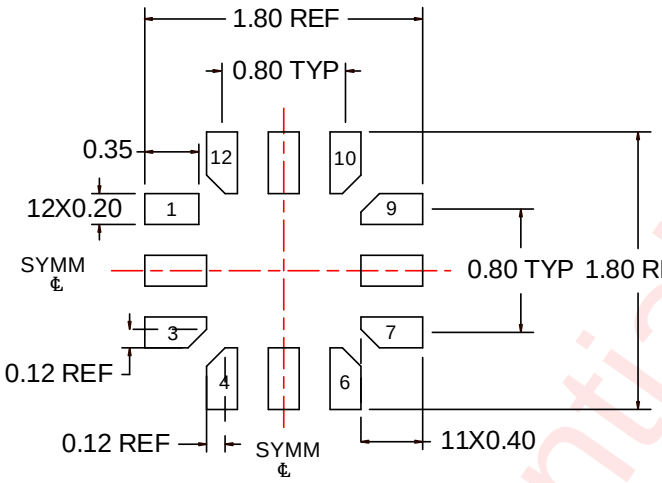
Land Pattern Data

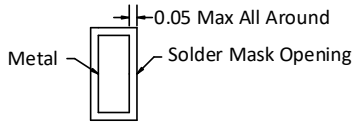




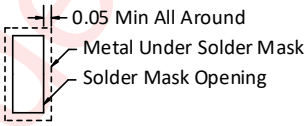
Unit: mm

AW86862CSR Land Pattern Data





Non-solder Mask Defined



Solder Mask Defined

Unit:mm

AW86862FCR Land Pattern Data

Revision History

Version	Date	Change Record
V1.0	Mar. 2021	Officially Released
V1.1	Jun. 2021	Add I²C device address description
V1.2	Jul. 2021	Update Chip ID
V1.3	Sept. 2021	Update the power consumption of 10Hz, add time calculation formula, improve register description
V1.4	May. 2022	Update Default of HOSC_SEL, and VS voltage adjustment
V1.5	Aug. 2022	Update 0xee and 0xef register types
V1.6	Dec. 2022	Update the description of Active Current
V1.7	Mar. 2023	Update the minimum of Analog supply voltage and 1 MHz SDA setup time
V1.8	May. 2024	Update the description of Power On Sequence. Modify I2C to I²C. Modify the description of the chip device address. Delete the register description of 0x23,0x24.

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