

## 0.1-3.8 GHz SP8T TRX Switch with MIPI

### Features

- Broadband frequency range: 0.1 to 3.8 GHz
- Low insertion loss: 0.65dB typical @ 2.7 GHz
- High isolation: 25dB typical @ 2.7 GHz
- P0.1dB @ 37dBm
- MIPI RFFE V2.1 interface
- QFN 2.0mm x 2.0mm x 0.55mm-14L package
- No DC blocking capacitors required (unless external DC is applied to the RF ports)

### Applications

- 2G/3G/4G antenna diversity
- Cellular modems , tablets and USB Devices
- Other RF front-end modules

### General Description

The AW13508TQNR is a SP8T switch with low insertion loss and high isolation. It can be used to support band switching and mode switching in antenna transmit and receive systems for 2G/3G/4G, data cards and tablets.

The AW13508TQNR is perfectly compatible with MIPI RFFE V2.1 control interface. It is provided in a compact QFN 2.0mm x 2.0mm x 0.55mm-14L package.

### Typical Application Circuit

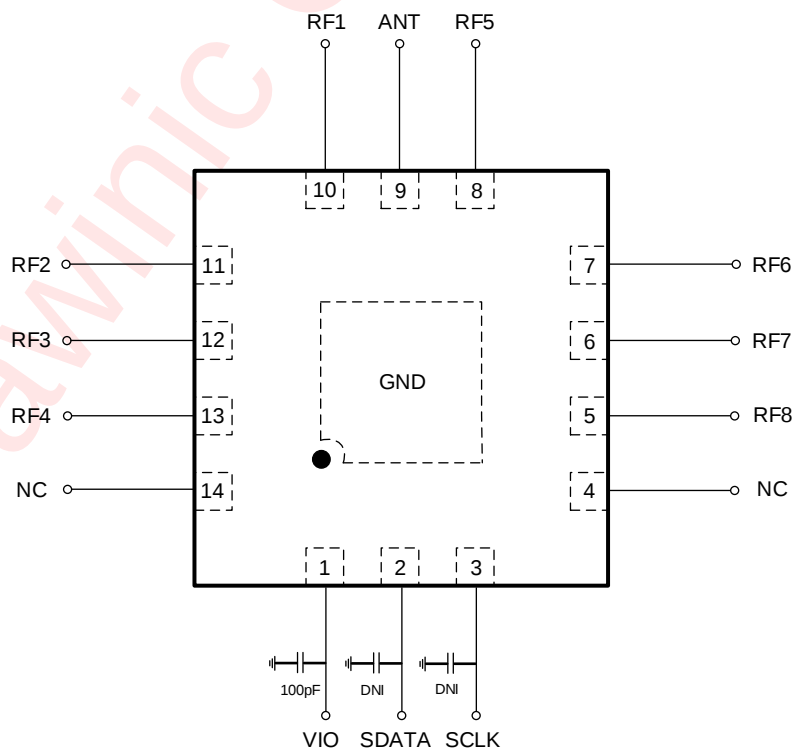


Figure 1 Typical Application Circuit of AW13508TQNR

## Pin Configuration And Top Mark

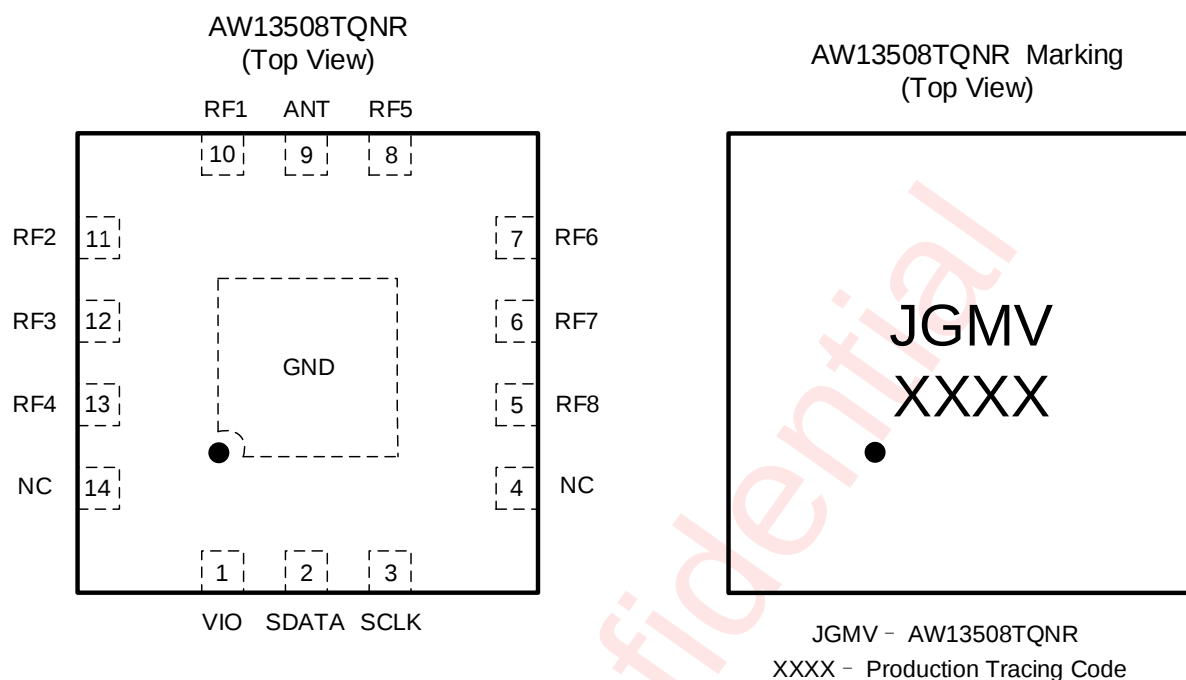


Figure 2 Pin Configuration and Top Mark

## Pin Definition

| No. | NAME            | DESCRIPTION            |
|-----|-----------------|------------------------|
| 1   | V <sub>IO</sub> | Power supply           |
| 2   | SDATA           | MIPI data input/output |
| 3   | SCLK            | MIPI clock             |
| 4   | NC              | Not Connect or Ground  |
| 5   | RF8             | RF8 port               |
| 6   | RF7             | RF7 port               |
| 7   | RF6             | RF6 port               |
| 8   | RF5             | RF5 port               |
| 9   | ANT             | Antenna port           |
| 10  | RF1             | RF1 port               |
| 11  | RF2             | RF2 port               |
| 12  | RF3             | RF3 port               |
| 13  | RF4             | RF4 port               |
| 14  | NC              | Not Connect            |

## Functional Block Diagram

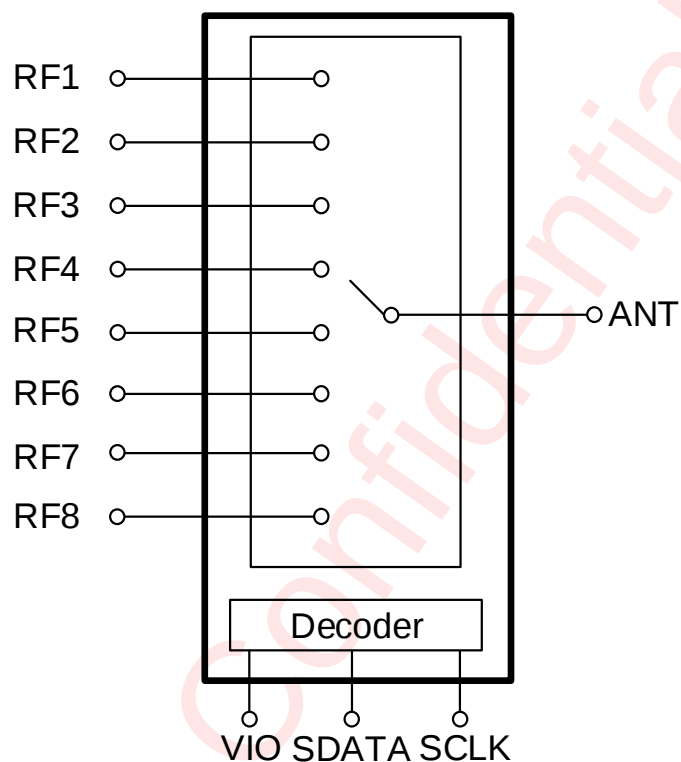


Figure 3 Functional Block Diagram

## Ordering Information

| Part Number | Temperature | Package                               | Marking | Moisture Sensitivity Level | Environmental Information | Delivery Form                  |
|-------------|-------------|---------------------------------------|---------|----------------------------|---------------------------|--------------------------------|
| AW13508TQNR | -40°C~85°C  | QFN<br>2.0mm x 2.0mm x<br>0.55mm -14L | JGMV    | MSL1                       | ROHS+HF                   | 4500<br>units/Tape<br>and Reel |

**Absolute Maximum Ratings** (NOTE 1)

| PARAMETERS                                  | RANGE          |
|---------------------------------------------|----------------|
| Interface Supply Voltage Range $V_{IO}$     | -0.3V to 2.5V  |
| Interface Control Voltage Range SDATA, SCLK | -0.3V to 2.5V  |
| RF input power<br>(RF1 to RF8 )             | 38dBm          |
| Operating Free-air Temperature Range        | -40°C to 85°C  |
| Storage temperature $T_{STG}$               | -65°C to 150°C |
| Lead temperature (soldering 10 seconds)     | 260°C          |
| ESD                                         |                |
| HBM(Human Body Model)(NOTE 2)               | ±1000V         |
| CDM (Charged Device Model) (NOTE 3)         | ±500V          |

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS-002-2018.

## Electrical Characteristics

V<sub>IO</sub>=1.8V, P<sub>IN</sub>=0dBm, VSWR=1:1, Temp=25°C. (unless otherwise noted)

| PARAMETER                |                                           | TEST CONDITION                                                | MIN                  | TYP             | MAX                 | UNIT |
|--------------------------|-------------------------------------------|---------------------------------------------------------------|----------------------|-----------------|---------------------|------|
| <b>DC Specifications</b> |                                           |                                                               |                      |                 |                     |      |
| V <sub>IO</sub>          | Supply Voltage                            |                                                               | 1.6                  | 1.8             | 2.0                 | V    |
| I <sub>VIO</sub>         | V <sub>IO</sub> Supply Current            | Active Mode                                                   |                      | 37              | 65                  | μA   |
|                          |                                           | Low Power Mode                                                |                      | 2               | 10                  | μA   |
| V <sub>IH</sub>          | SDATA,SCLK Control Voltage High           | Must not exceed V <sub>IO</sub> voltage                       | 0.8* V <sub>IO</sub> | V <sub>IO</sub> | 2.0                 | V    |
| V <sub>IL</sub>          | SDATA,SCLK Control Voltage Low            | Must not exceed V <sub>IO</sub> voltage                       | 0                    | 0               | 0.3*V <sub>IO</sub> | V    |
| T <sub>ON</sub>          | Wakeup Time                               | From end of Low Power State 50% SCLK to 90% of final RF power |                      | 10              | 20                  | μs   |
| T <sub>SW</sub>          | Switching Speed<br>One RF port to another | 10% to 90% RF                                                 |                      | 0.75            | 1.6                 | μs   |
| <b>RF Specifications</b> |                                           |                                                               |                      |                 |                     |      |
| IL                       | Insertion loss<br>(ANT pin to RF pins)    | 0.1-1.0GHz                                                    |                      | 0.55            | 0.70                | dB   |
|                          |                                           | 1.0-2.0GHz                                                    |                      | 0.60            | 0.80                | dB   |
|                          |                                           | 2.0-2.7GHz                                                    |                      | 0.65            | 0.90                | dB   |
|                          |                                           | 3.3-3.8GHz                                                    |                      | 0.75            | 1.0                 | dB   |
| RL                       | Return loss<br>(ANT pin to RF pins)       | 0.1-1.0GHz                                                    | 18                   | 25              |                     | dB   |
|                          |                                           | 1.0-2.0GHz                                                    | 15                   | 20              |                     | dB   |
|                          |                                           | 2.0-2.7GHz                                                    | 12                   | 18              |                     | dB   |
|                          |                                           | 3.3-3.8GHz                                                    | 10                   | 15              |                     | dB   |
| ISO                      | Isolation<br>(ANT pin to RF pins)         | 0.1-1.0GHz                                                    | 25                   | 30              |                     | dB   |
|                          |                                           | 1.0-2.0GHz                                                    | 22                   | 28              |                     | dB   |
|                          |                                           | 2.0-2.7GHz                                                    | 20                   | 25              |                     | dB   |
|                          |                                           | 3.3-3.8GHz                                                    | 18                   | 22              |                     | dB   |

| PARAMETER          |                                                 | TEST CONDITION                               | MIN | TYP | MAX | UNIT |
|--------------------|-------------------------------------------------|----------------------------------------------|-----|-----|-----|------|
| $2f_0$             | Second Harmonics<br>(ANT pin to RF pins)        | Freq@900MHz,<br>$P_{IN}=+26\text{dBm}$ , CW  |     | 90  |     | dBc  |
| $3f_0$             | Third Harmonics<br>(ANT pin to RF pins)         | Freq@900MHz,<br>$P_{IN}=+26\text{dBm}$ , CW  |     | 84  |     | dBc  |
| $2f_0$             | Second Harmonics<br>(ANT pin to RF pins)        | Freq@1900MHz,<br>$P_{IN}=+26\text{dBm}$ , CW |     | 90  |     | dBc  |
| $3f_0$             | Third Harmonics<br>(ANT pin to RF pins)         | Freq@1900MHz,<br>$P_{IN}=+26\text{dBm}$ , CW |     | 88  |     | dBc  |
| $P_{0.1\text{dB}}$ | 0.1dB Compression Point<br>(ANT pin to RF pins) | 0.1-3.8GHz                                   |     | 37  |     | dBm  |

## Timing Diagram (Power On and Off Sequence)

- Once  $V_{IO}$  is powered down to 0 V, wait at least  $10\ \mu\text{s}$  to reapply power to  $V_{IO}$ .

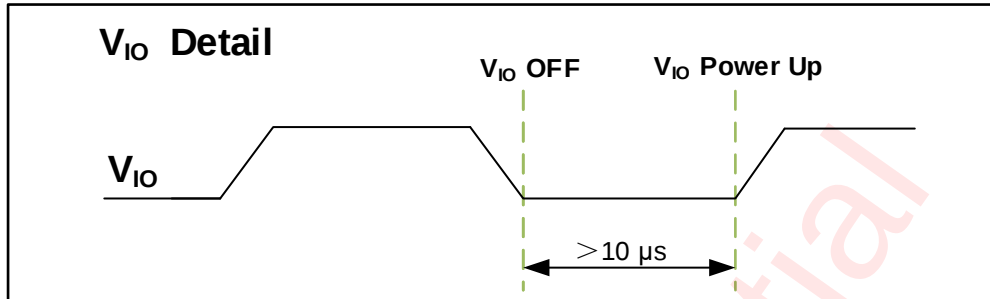


Figure 4 Digital Supply Detail

- Before applying RF power,  $V_{IO}$  must be turned on for at least  $20\ \mu\text{s}$ .

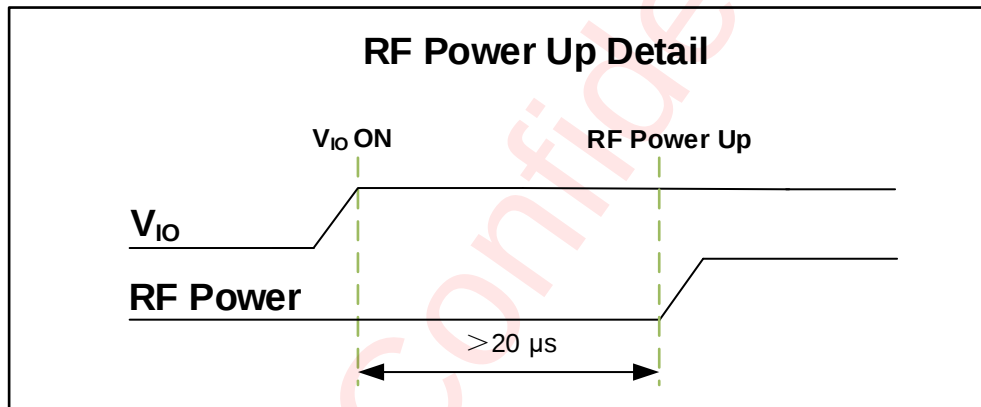


Figure 5 RF Power-Up Detail

- Before sending SDATA/SCLK,  $V_{IO}$  must be applied for at least  $800\ \text{ns}$  to ensure correct data transmission. And after the RFFE bus is idle, wait at least  $20\ \mu\text{s}$  to apply the RF signal.

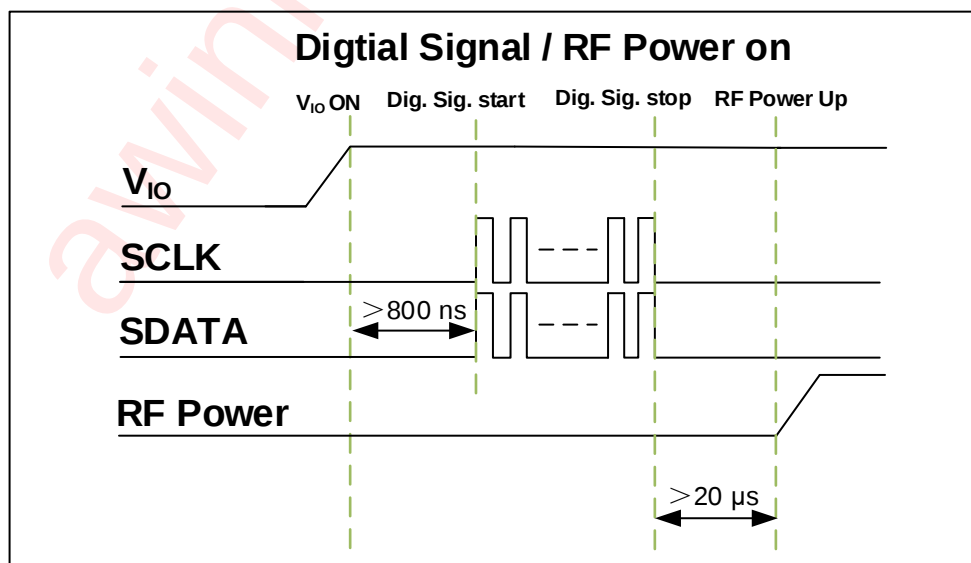


Figure 6 Digital Signal / RF Power-On Detail

4. There shall be no RFFE bus operations during RF Signal active to protect the device. So RF input signal shall be applied after RFFE bus operations being finished and be removed before RFFE bus operations being started.

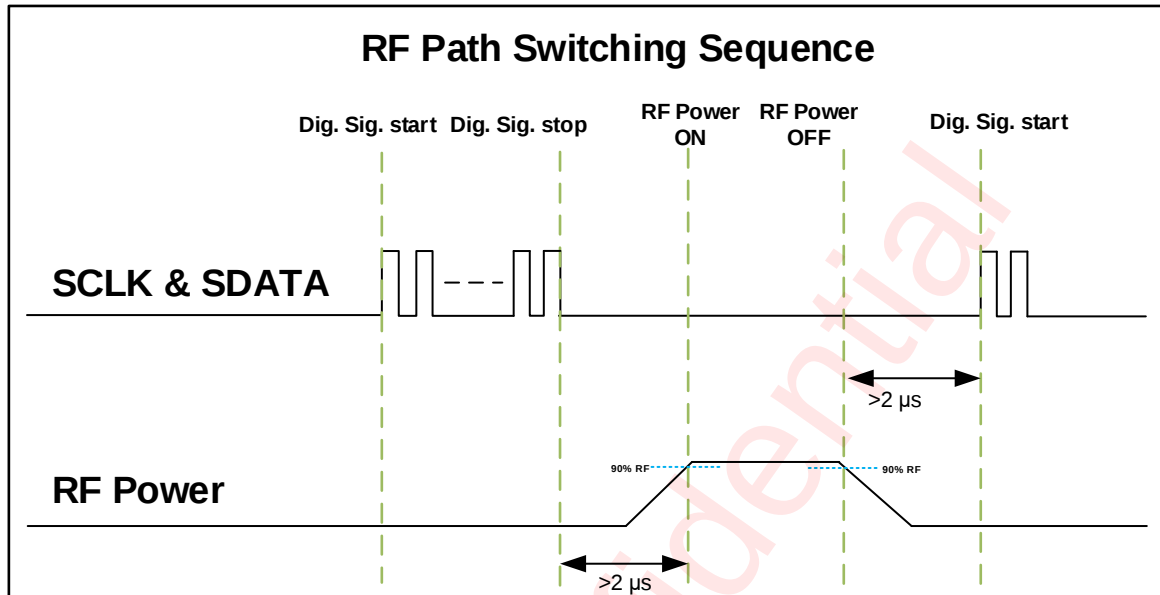


Figure 7 RF Path Switching Sequence

5. If “Lower Power Mode” is used, there must be a 10 μs delay before exiting “Lower Power Mode”.

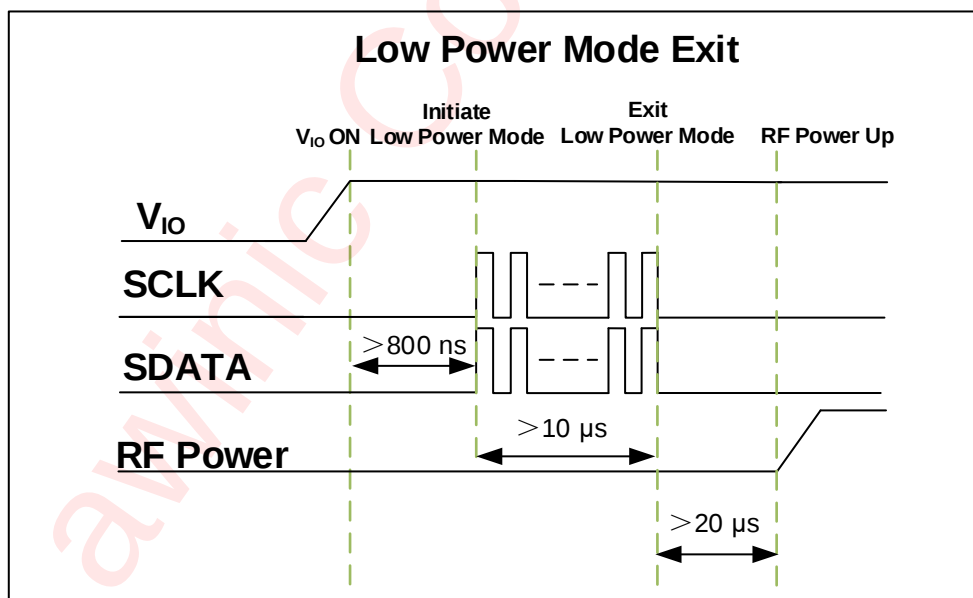


Figure 8 Lower Power Mode Exit Timing

## MIPI RFFE Specification

The MIPI RFFE interface is working in systems following the 'MIPI Alliance Specification for RF Front-End Control Interface version 2.1.

**TABLE1: MIPI FEATURES**

| Feature                                                  | Supported | Comment                                                        |
|----------------------------------------------------------|-----------|----------------------------------------------------------------|
| MIPI RFFE 2.1 standard                                   | Yes       |                                                                |
| Register 0 write command sequence                        | Yes       |                                                                |
| Register read and write command sequence                 | Yes       |                                                                |
| Extended register read and write command sequence        | Yes       |                                                                |
| Masked write command sequence                            | Yes       | Indicated as MW in below register mapping tables               |
| Support for standard frequency range operations for SCLK | Yes       | Up to 26 MHz for read and write                                |
| Support for extended frequency range operations for SCLK | Yes       | Up to 52 MHz for write                                         |
| Half speed read                                          | Yes       |                                                                |
| Full speed read<br>Full speed write                      | Yes       |                                                                |
| Longer Reach RFFE Bus Length Feature                     | Yes       |                                                                |
| Programmable driver strength                             | Yes       |                                                                |
| Programmable Group SID                                   | Yes       |                                                                |
| Programmable USID                                        | Yes       | Support for three registers write and extended write sequences |
| Trigger functionality                                    | Yes       |                                                                |
| Extended Triggers and Trigger Masks                      | Yes       |                                                                |
| Broadcast / GSID write to PM TRIG register               | Yes       |                                                                |
| Reset                                                    | Yes       | Via VIO, PM TRIG or software register                          |
| Status / error sum register                              | Yes       |                                                                |
| Extended product ID register                             | Yes       |                                                                |
| Revision ID register                                     | Yes       |                                                                |
| Group SID register                                       | Yes       |                                                                |
| USID select pin                                          | No        |                                                                |

TABLE2: Start-up Behavior

| Feature          | State          | Comment                                          |
|------------------|----------------|--------------------------------------------------|
| Power status     | Low power mode | Low power mode after start-up                    |
| Trigger function | Enable         | Enable after start-up. Programmable via register |

## MIPI Read and Write Timing

### Register 0 Write:

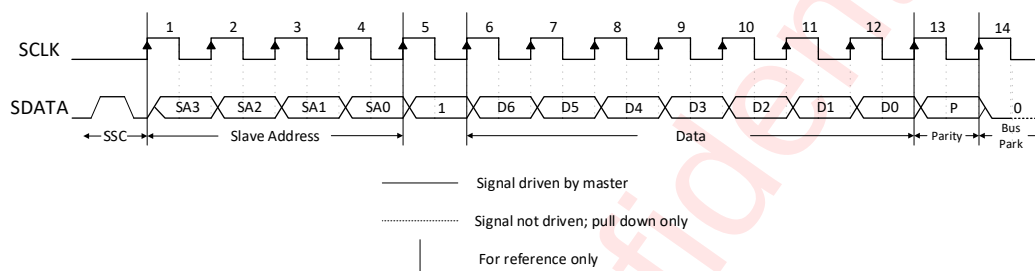


Figure 9 Register 0 Write Command Sequence

### Register Write:

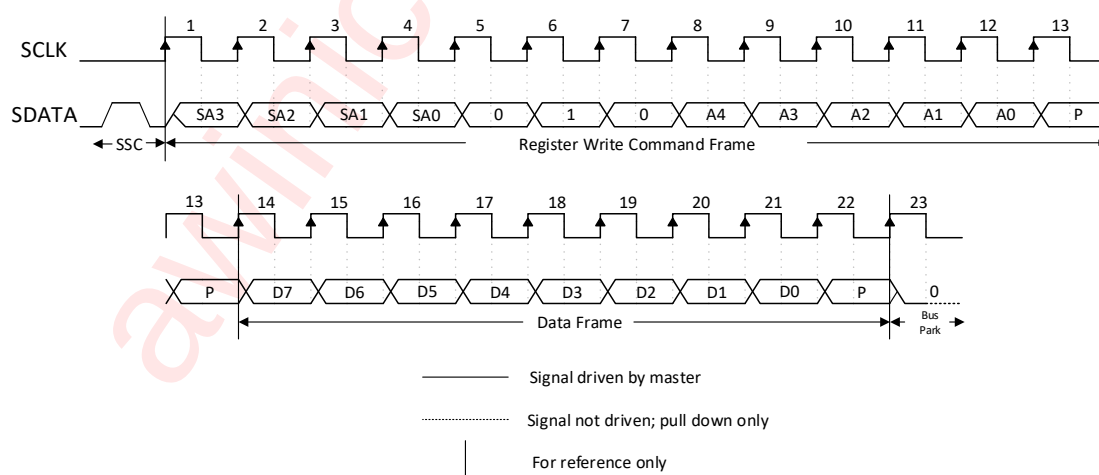
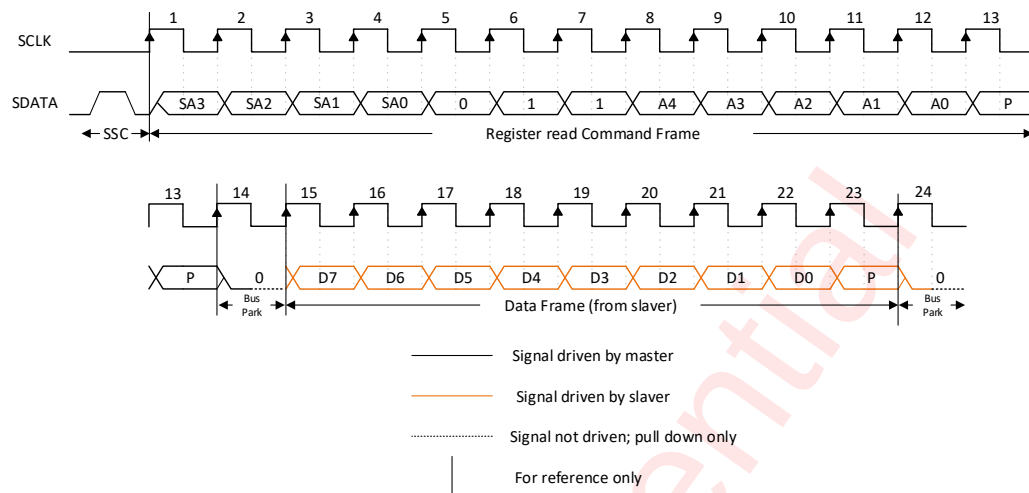
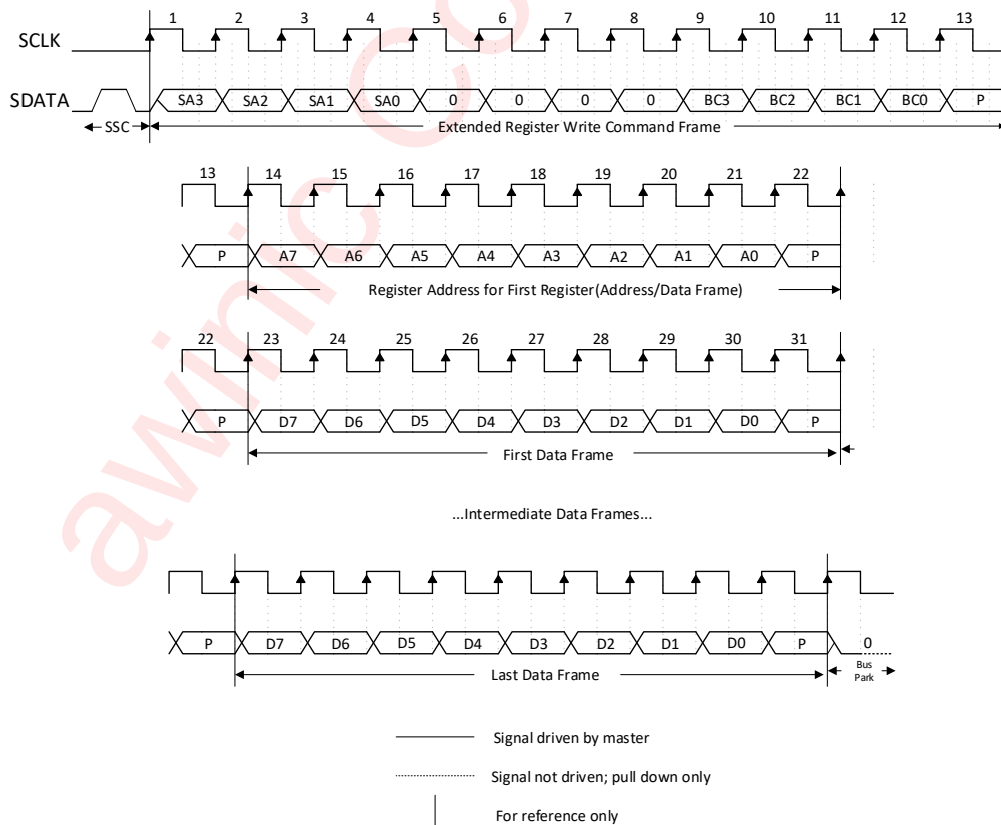
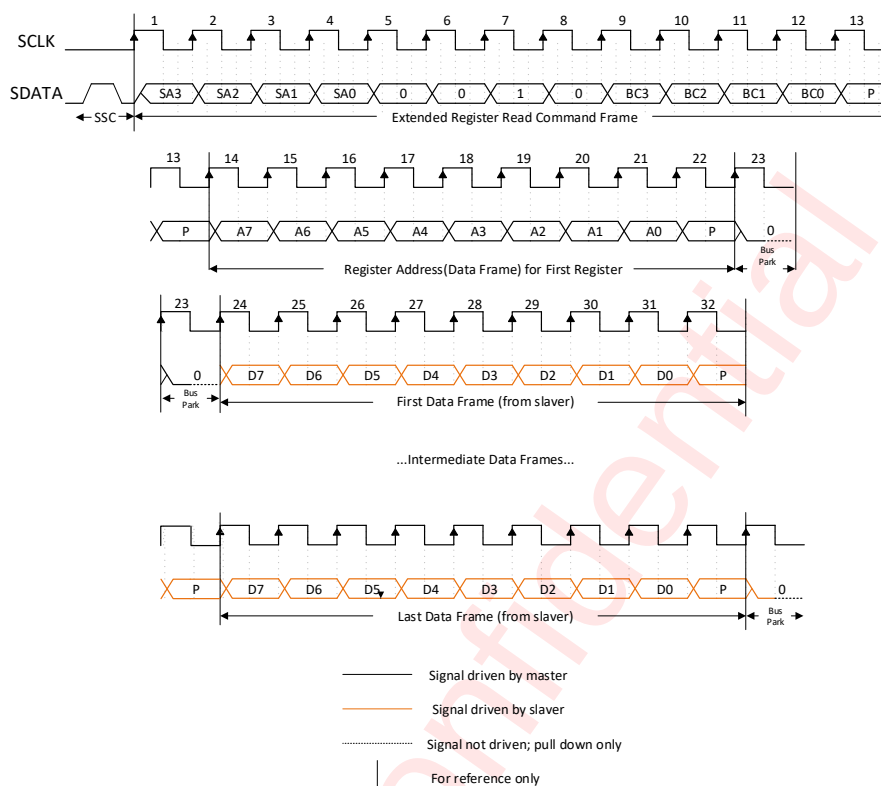
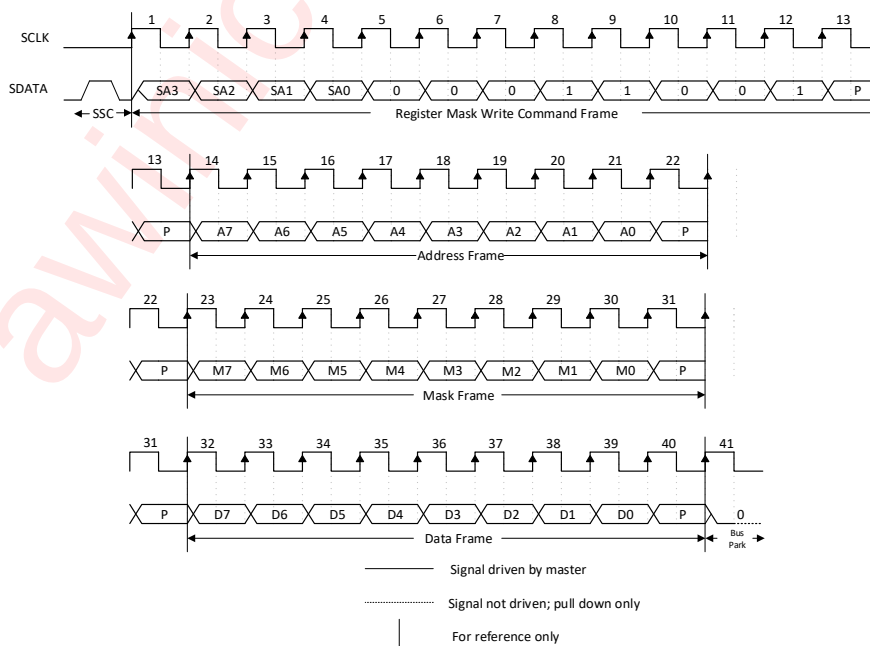


Figure 10 Register Write Command Sequence

**Register Read:****Figure 11 Register Read Command Sequence****Extended Register Write:****Figure 12 Extended Register Write Command Sequence**

**Extended Register Read:****Figure 13 Extended Register Read Command Sequence****Masked Write:****Figure 14 Masked Write Command Sequence**

## Register Configuration

### Register Detailed Description

#### REGISTER\_0 : Mode Control Register(Address 0000h)

|       |         | Register_0 Bits |    |    |    |    |    |    |    |
|-------|---------|-----------------|----|----|----|----|----|----|----|
| State | Mode    | D7              | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1     | ALL OFF | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| 2     | RF2 ON  | x               | x  | x  | x  | x  | 1  | x  | x  |
| 3     | RF3 ON  | x               | x  | x  | x  | x  | x  | 1  | x  |
| 4     | RF5 ON  | x               | x  | x  | 1  | x  | x  | x  | x  |
| 5     | RF6 ON  | x               | x  | 1  | x  | x  | x  | x  | x  |
| 6     | RF7 ON  | x               | 1  | x  | x  | x  | x  | x  | x  |

#### REGISTER\_1 : Mode Control Register(Address 0001h)

|       |         | Register_1 Bits |    |    |    |    |    |    |    |
|-------|---------|-----------------|----|----|----|----|----|----|----|
| State | Mode    | D7              | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1     | ALL OFF | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| 2     | RF1 ON  | x               | x  | x  | x  | x  | x  | x  | 1  |
| 3     | RF4 ON  | x               | x  | x  | x  | 1  | x  | x  | x  |
| 4     | RF8 ON  | x               | x  | x  | x  | x  | 1  | x  | x  |

#### RFFE\_STATUS : RFFE Status Register(Address 001Ah)

| Bit | Symbol        | Description                                                                                                     | R/W | B/G | Trig | Default |
|-----|---------------|-----------------------------------------------------------------------------------------------------------------|-----|-----|------|---------|
| 7   | UDR_RST       | Reset all configurable non-RFFE reserved register to default values<br>0: normal operation<br>1: software reset | W   | No  | No   | 0       |
| 6   | CMD_FR_P_ERR  | Command Frame received with a parity error                                                                      | RW  | No  | No   | 0       |
| 5   | CMD_LEN_ERR   | Command Sequence received with an incorrect length                                                              | RW  | No  | No   | 0       |
| 4   | ADDR_FR_P_ERR | Address Frame received with a parity error                                                                      | RW  | No  | No   | 0       |
| 3   | DATA_FR_P_ERR | Data Frame received with a parity error                                                                         | RW  | No  | No   | 0       |
| 2   | RD_INVLD_ADDR | Read Command Sequence received with an invalid address                                                          | RW  | No  | No   | 0       |
| 1   | WR_INVLD_ADDR | Write Command Sequence received with an invalid address                                                         | RW  | No  | No   | 0       |
| 0   | BID_GID_ERR   | Read Command Sequence received with a BSID or GSID                                                              | RW  | No  | No   | 0       |

**GSID0\_1 : Group ID 0-1 Register(Address 001Bh)**

| Bit | Symbol | Description     | R/W | B/G | Trig | Default |
|-----|--------|-----------------|-----|-----|------|---------|
| 7:4 | GSID0  | Group Slave ID0 | RW  | No  | No   | 0000    |
| 3:0 | GSID1  | Group Slave ID1 | RW  | No  | No   | 0000    |

**PM\_TRIG : Pwr\_mode and Trig Register(Address 001Ch)**

| Bit | Symbol       | Description                                                   | R/W      | B/G | Trig | Default |
|-----|--------------|---------------------------------------------------------------|----------|-----|------|---------|
| 7   | PWR_MODE[1]  | 0: normal operation<br>1: low power                           | RW<br>MW | Yes | No   | 1       |
| 6   | PWR_MODE[0]  | 0: active<br>1: start up – Reset all register to default      | RW<br>MW | Yes | No   | 0       |
| 5:3 | TRIGGER_MASK | Setting bit TRIGGER[n] loads TRIGGER[n]'s associated register | RW<br>MW | No  | No   | 000     |
| 2:0 | TRIGGER      | Setting bit TRIGGER[n] loads TRIGGER[n]'s associated register | RW<br>MW | Yes | No   | 000     |

**PRODUCT\_ID : Product ID Register(Address 001Dh)**

| Bit | Symbol  | Description                    | R/W | B/G | Trig | Default |
|-----|---------|--------------------------------|-----|-----|------|---------|
| 7:0 | PROD_ID | Lower eight bits of Product ID | R   | No  | No   | 0x0E    |

**MANUFACTURER\_ID : Manufacture ID Register(Address 001Eh)**

| Bit | Symbol | Description                         | R/W | B/G | Trig | Default |
|-----|--------|-------------------------------------|-----|-----|------|---------|
| 7:0 | MFG_ID | Lower eight bits of Manufacturer ID | R   | No  | No   | 0x49    |

**MAN\_USID : User ID Register(Address 001Fh)**

| Bit | Symbol | Description                        | R/W | B/G | Trig | Default |
|-----|--------|------------------------------------|-----|-----|------|---------|
| 7:4 | MFG_ID | Upper four bits of Manufacturer ID | R   | No  | No   | 0000    |
| 3:0 | USID   | Unique Slave ID                    | RW  | No  | No   | 1010    |

**EXT\_PRODUCT\_ID : Extend Product ID Register(Address 0020h)**

| Bit | Symbol  | Description                    | R/W | B/G | Trig | Default |
|-----|---------|--------------------------------|-----|-----|------|---------|
| 7:0 | PROD_ID | Upper eight bits of Product ID | R   | No  | No   | 0x00    |

**REVISION\_ID : Revision ID Register(Address 0021h)**

| Bit | Symbol | Description | R/W | B/G | Trig | Default |
|-----|--------|-------------|-----|-----|------|---------|
| 7:0 | REV_ID | Revision ID | R   | No  | No   | 0x00    |

**GSID2\_3 : Group ID 2-3 Register(Address 0022h)**

| Bit | Symbol | Description     | R/W | B/G | Trig | Default |
|-----|--------|-----------------|-----|-----|------|---------|
| 7:4 | GSID2  | Group Slave ID2 | R/W | No  | No   | 0000    |
| 3:0 | GSID3  | Group Slave ID3 | R/W | No  | No   | 0000    |

**UDR\_RST : UDR Reset Register(Address 0023h)**

| Bit | Symbol   | Description                                                                                           | R/W | B/G | Trig | Default |
|-----|----------|-------------------------------------------------------------------------------------------------------|-----|-----|------|---------|
| 7   | UDR_RST  | Reset all configurable non-RFFE reserved register to default values<br>0: normal<br>1: software reset | R/W | Yes | No   | 0       |
| 6:0 | RESERVED | Reserved                                                                                              | R/W | No  | No   | 0x00    |

**ERR\_SUM : Error Command Status Register(Address 0024h)**

| Bit | Symbol        | Description                                             | R/W | B/G | Trig | Default |
|-----|---------------|---------------------------------------------------------|-----|-----|------|---------|
| 7   | SPARE         | Reserved for future use                                 | R/W | No  | No   | 0       |
| 6   | COM_FR_P_ERR  | Command Frame received with a parity error              | R/W | No  | No   | 0       |
| 5   | COM_LEN_ERR   | Command Sequence received with an incorrect length      | R/W | No  | No   | 0       |
| 4   | ADDR_FR_P_ERR | Address Frame received with a parity error              | R/W | No  | No   | 0       |
| 3   | DATA_FR_P_ERR | Data Frame received with a parity error                 | R/W | No  | No   | 0       |
| 2   | RD_INVLD_ADDR | Read Command Sequence received with an invalid address  | R/W | No  | No   | 0       |
| 1   | WR_INVLD_ADDR | Write Command Sequence received with an invalid address | R/W | No  | No   | 0       |
| 0   | BID_GID_ERR   | Read Command Sequence received with a BSID or GSID      | R/W | No  | No   | 0       |

**BUS\_LD : SDATA Driver Strength Register(Address 002Bh)**

| Bit | Symbol   | Description                                | R/W | B/G | Trig | Default |
|-----|----------|--------------------------------------------|-----|-----|------|---------|
| 7:1 | reserved | reserved                                   | R/W | No  | No   | 0x00    |
| 0   | BUS_LD   | SDATA drive strength<br>0: 50pf<br>1: 80pf | R/W | No  | No   | 0       |

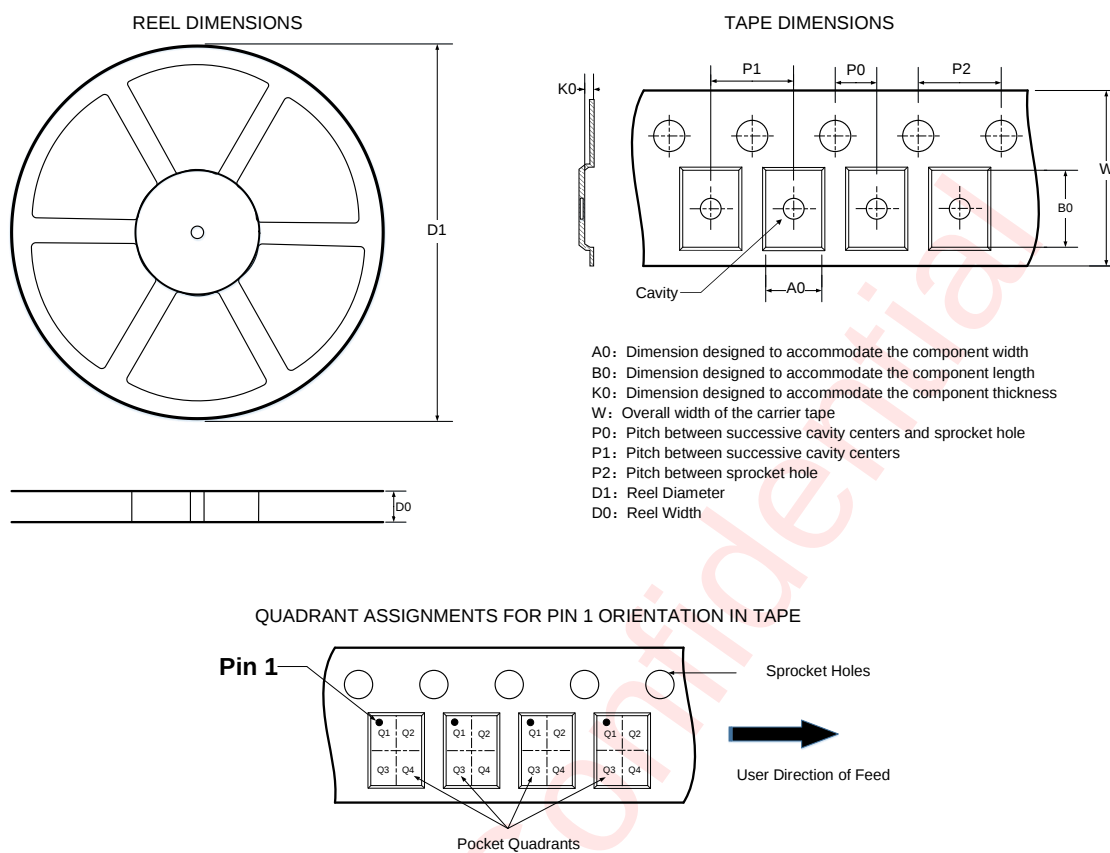
**EXT\_TRIG\_MASK : Extend Trig Mask Register(Address 002Dh)**

| Bit | Symbol        | Description                                       | R/W      | B/G | Trig | Default |
|-----|---------------|---------------------------------------------------|----------|-----|------|---------|
| 7:0 | EXT_TRIG_MASK | Setting bit EXT_TRIG_MASK[n] disables EXT_TRIG[n] | RW<br>MW | No  | No   | 0xFF    |

**EXT\_TRIG : Extend Trig Register(Address 002Eh)**

| Bit | Symbol   | Description                                                     | R/W      | B/G | Trig | Default |
|-----|----------|-----------------------------------------------------------------|----------|-----|------|---------|
| 7:0 | EXT_TRIG | Setting bit EXT_TRIG[n] loads EXT_TRIG[n]'s associated register | RW<br>MW | Yes | No   | 0x00    |

## Tape And Reel Information



Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

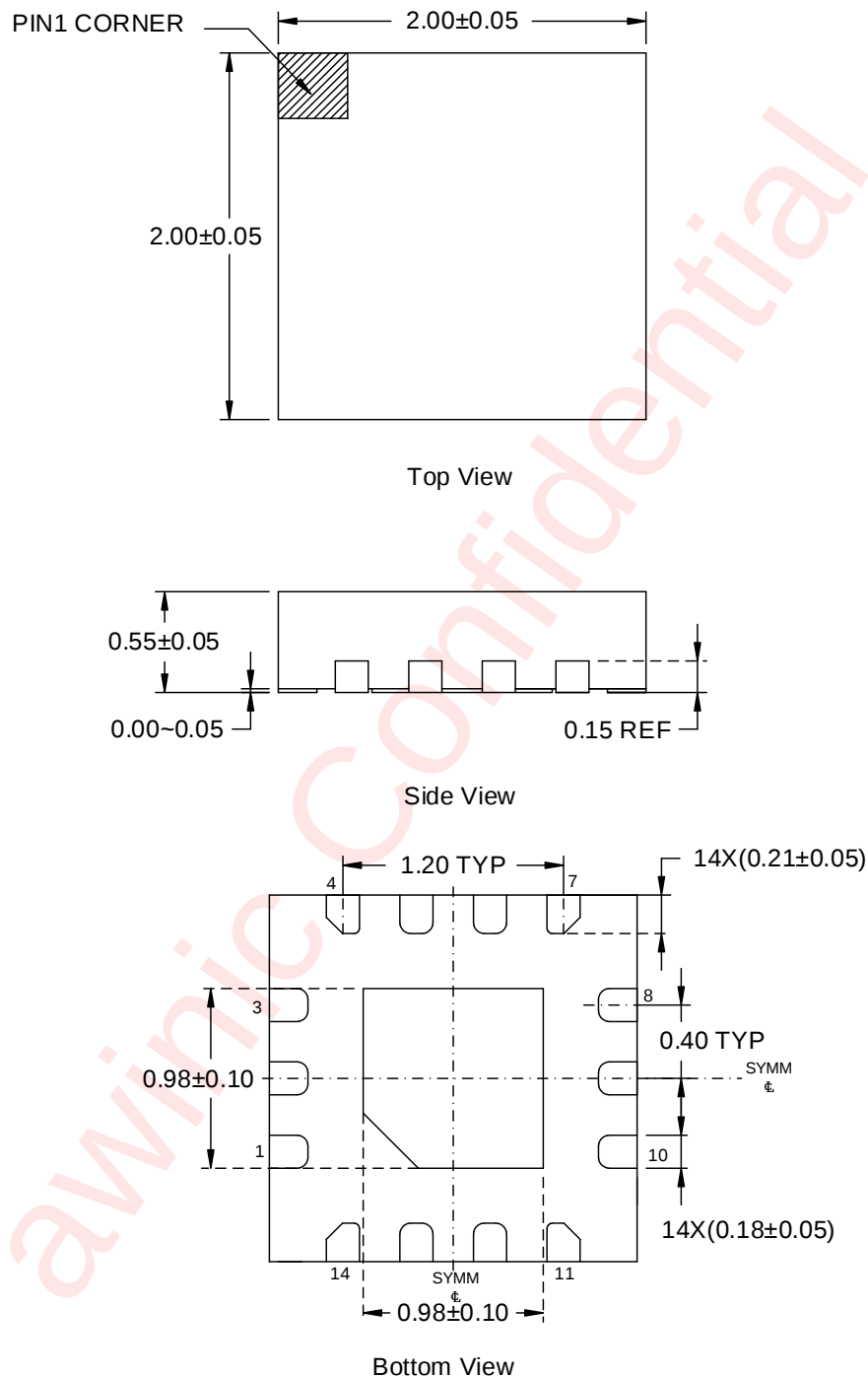
DIMENSIONS AND PIN1 ORIENTATION

| D1<br>(mm) | D0<br>(mm) | A0<br>(mm) | B0<br>(mm) | K0<br>(mm) | P0<br>(mm) | P1<br>(mm) | P2<br>(mm) | W<br>(mm) | Pin1 Quadrant |
|------------|------------|------------|------------|------------|------------|------------|------------|-----------|---------------|
| 178        | 8.4        | 2.25       | 2.25       | 0.75       | 2          | 4          | 4          | 8         | Q1            |

All dimensions are nominal

Figure 15 Tape and Reel

## Package Description



Unit: mm

Figure 16 Package Outline

## Land Pattern Data

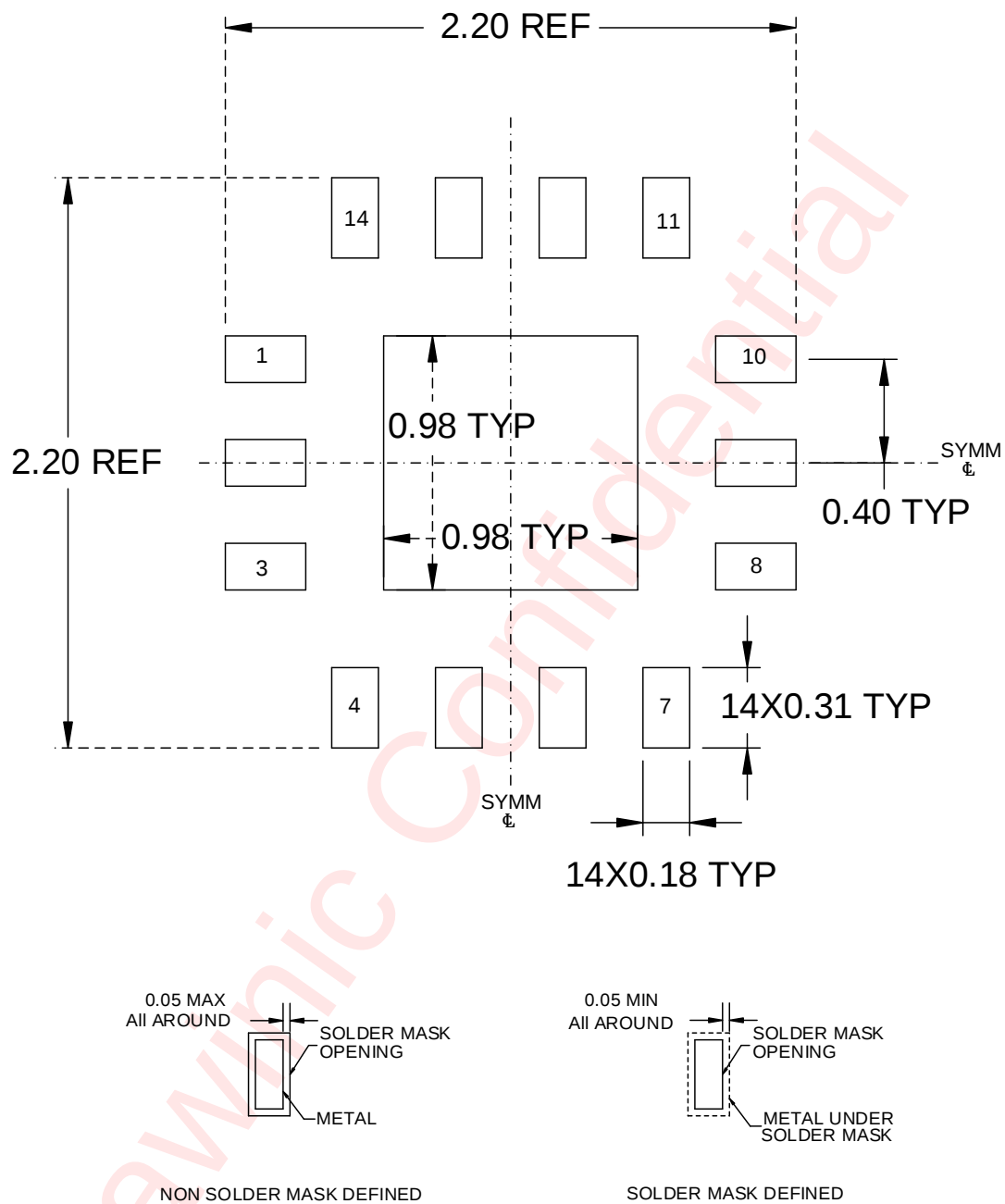


Figure 17 Land Pattern Data

## Revision History

| Version | Date      | Change Record                                                                                            |
|---------|-----------|----------------------------------------------------------------------------------------------------------|
| V1.0    | Dec. 2021 | Officially Released                                                                                      |
| V1.1    | Feb. 2022 | Update Supply Voltage Range and Control Voltage Range (P4&P5)<br>Change the spec of T <sub>sw</sub> (P5) |
| V1.2    | Aug. 2022 | Fix Some Formatting Issues and Revise the Pin 4 Definition                                               |

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