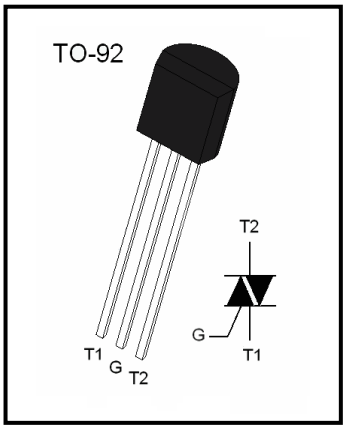
BT131-800

TO-92 Plastic-Encapsulate Triacs



GENERAL DESCRIPTION

Logic level sensitive gate triac intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

FEATURES

- Blocking voltage to 800V
- RMS on-state current to 0.8A
- Sensitive gate in all four quadrants

Absolute Maximum Rating (Ta=25℃)

Limiting values in accordance with the Absolute Maximum System

Parameter	Symbol	Conditions		Rating	Unit
Repetitive peak off-state voltages	V_{DRM}			-800 800	V
On-State RMS Current	$I_{T(RMS)}$	full sine wave; $T_{mb} \leq 108$ °C		1	A
Non-repetitive peak on-state current	I_{TSM}	full sine wave; $T_j = 25$ °C prior to surge	t = 20 ms	10	A
			t = 16.7 ms	11	
I^2t for fusing	I^2t	t = 10 ms		0.5	A^2s
Repetitive rate of rise of on-state current after triggering	dI_T/dt	$I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/μs	T2+ G+	50	A/μs
			T2+ G-	50	
			T2- G-	50	
			T2- G+	10	
Peak gate current	I_{GM}			2	A
Peak Gate Voltage	V_{GM}			5	V
Peak gate power	P_{GM}			5	W
Average gate power	$P_{G(AV)}$	over any 20 ms period		0.5	W
Storage Temperature	T_{stg}			-40~150	℃
Operating junction temperature	T_J			125	℃

Thermal Resistances

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Thermal resistance junction to solder point	Rth j-sp	full or half cycle	-		15	K/W
Thermal resistance junction to ambient	Rth j-a	pcb mounted; minimum footprint pcb mounted;	-	156 70		K/W

Static Characteristics T_j = 25 °C unless otherwise stated

Parameter	Symbol	Conditions		Min	Typ	Max			Unit
						···	···F	···G	
Gate trigger current	I_{GT}	V_D = 12 V I_T = 0.1 A	T2+ G+	-		35	25	50	mA
			T2+ G-	-		35	25	50	
			T2- G-	-		35	25	50	
			T2- G+	-		70	70	100	
Latching current	I_L	V_D = 12 V I_{GT} = 0.1 A	T2+ G+	-		20	20	30	mA
			T2+ G-	-		30	30	45	
			T2- G-	-		20	20	30	
			T2- G+	-		30	30	45	
Holding current	I_H	V_D = 12 V, I_{GT} = 0.1 A				15	15	30	mA
On-state voltage	V_T	I_T = 2A			1.2	1.5			V
Gate trigger voltage	V_{GT}	V_D = 12 V; I_T = 0.1 A				1.5			V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 °C		0.25					
Off-state leakage current	I_D	V_D = $V_{DRM(max)}$; T_j = 125 °C				0.5			mA

Dynamic Characteristics Tj = 25 ˚C unless otherwise stated

Parameter	Symbol	Conditions	Min			Typ	Max	Unit
			···	···F	···G			
Critical rate of rise of Critical rate of rise of	dV_D/dt	V_{DM} =67% V_{DRM}(max); V_{DM} =67% V_{DRM}(max); V_{DM} =67% V_{DRM}(max); circuit	100	50	200	250	-	V/μs
Critical rate of change of commutating voltage	dVcom/dt	V_{DM} = 400 V; T_j = 95˚C; $I_{T(RMS)}$ = 1 A; d_{Icom}/dt = 1.8 A/ms; gate open circuit	-	-	10	50	-	V/μs
Gate controlled turn-on time	tgt	I_{TM} = 1.5 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/μs;						μs

Typical Characteristics

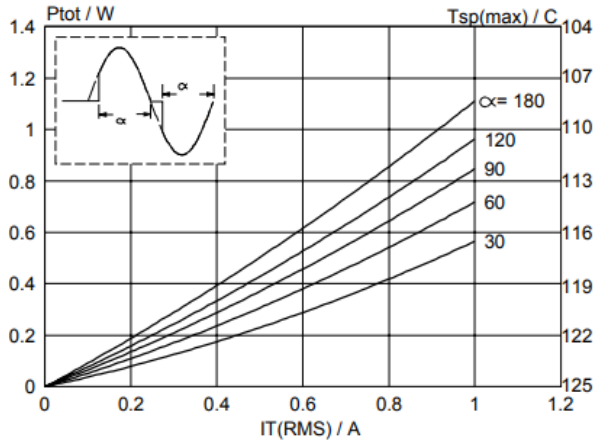


Fig.1. Maximum on-state dissipation, Ptot, vs rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

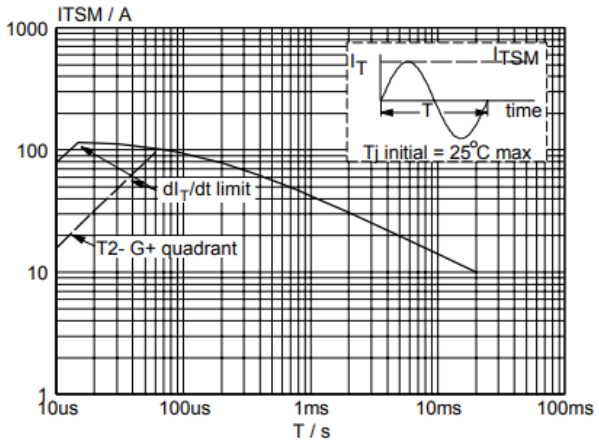


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, vs pulse width tp, for sinusoidal currents, tp ≤ 20ms.

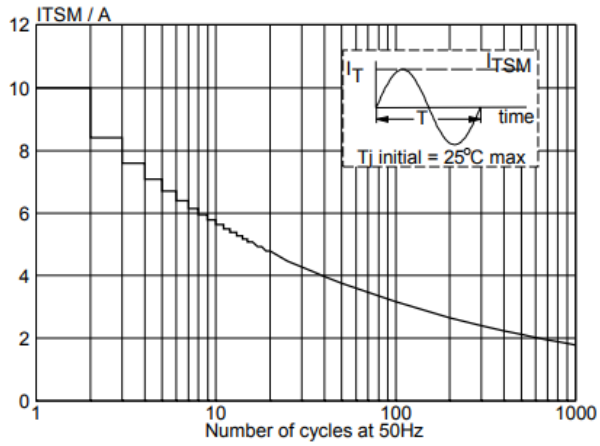


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, vs number of cycles, for sinusoidal currents, f = 50 Hz.

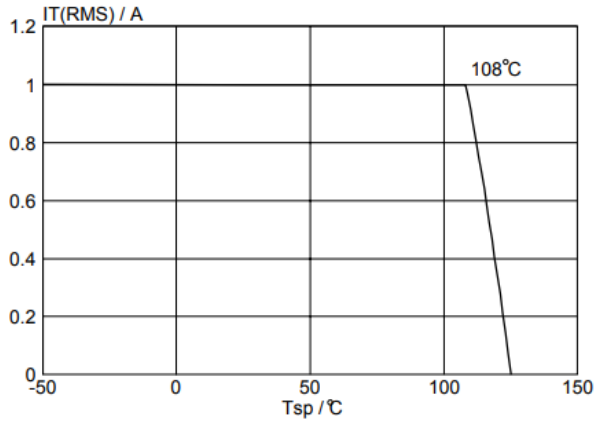


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, vs solder point temperature Tsp.

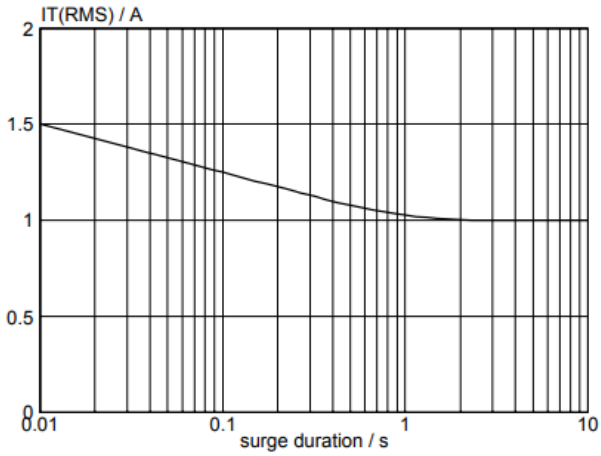


Fig.5. Maximum ermissible repetitive rms n-state current $I_{T(RMS)}$, vs surge duration, for sinusoidal currents, f = 50Hz; T_{sp} ≤ 108˚C.

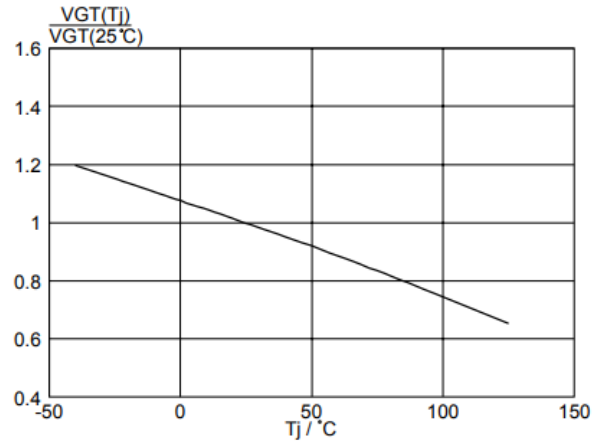
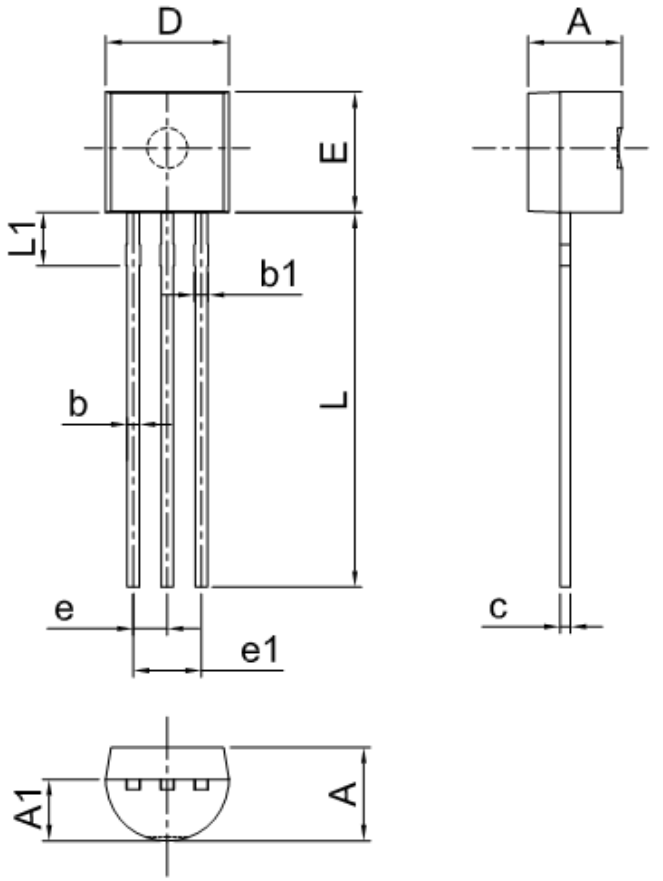


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25˚C)$, vs junction temperature T_j .

Package Dimensions (Unit:mm)



Symbol	TO-92		
	Min.	Typ	Max.
A	3.30	3.50	3.70
A1	2.10	2.30	2.50
b	0.40	0.45	0.50
b1	0.50	0.55	0.60
c	0.35	0.40	0.45
D	4.45	4.55	4.65
E	4.45	4.55	4.65
e	1.17	1.27	1.37
e1	2.34	2.54	2.64
L	13.50	14.00	14.50
L1	1.80	2.00	2.20