

## Triple Outputs Switching Converter for AMOLED Display

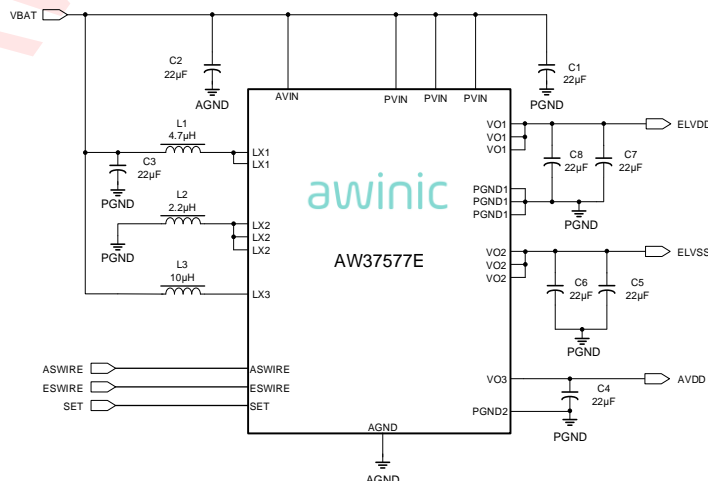
### FEATURES

- Input voltage: 2.5V ~ 5.0V
- Excellent line and load transient response
- Programmable output voltage by ESWIRE from 4.6V to 5V in 100mV steps (Default: 4.6V)
- Programmable output voltage by ESWIRE from -6.6V to -1V in 100mV steps (Default: -4V)
- Programmable output voltage by ASWIRE from 6.9V to 7.9V in 50mV & 7.1V to 7.8V in 100mV steps (Default: 7.6V)
- Max Output current for ELVDD and ELVSS
  - 600mA @  $V_{IN}=2.5V$ , ELVDD=4.6V, ELVSS= -4V
  - 750mA @  $V_{IN}=3.2V$ , ELVDD=4.6V, ELVSS= -6V
  - 800mA @  $V_{IN}=3.2V$ , ELVDD=4.6V, ELVSS= -5V
  - 800mA @  $V_{IN}=3.4V$ , ELVDD=4.6V, ELVSS= -6V
  - 850mA @  $V_{IN}=3.0V$ , ELVDD=4.6V, ELVSS= -4V
- 150mA Max Output current for AVDD
- Short Circuit Protection (SCP)
- WLCSP 2.05X2.05 - 25B

### APPLICATIONS

Active Matrix OLED

### TYPICAL APPLICATION CIRCUIT

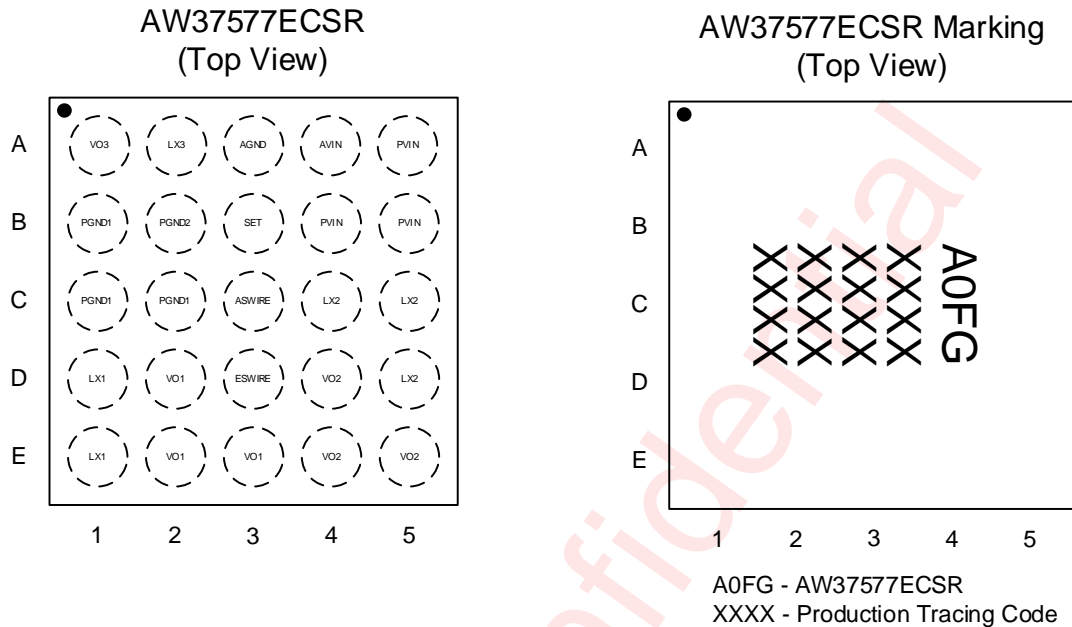


### GENERAL DESCRIPTION

The AW37577E is specially designed for AMOLED (Active Matrix organic LED) Display panels. It integrates two high performance boost converters, VO1 (positive voltage ELVDD) and VO3 (AVDD), one inverting buck-boost converter for VO2 (negative voltage ELVSS). These converters have excellent line and load transient response.

The VO3 can be programmed by ASWIRE, the VO1 and VO2 can be programmed by ESWIRE. All these interfaces can turn on/off corresponding converters.

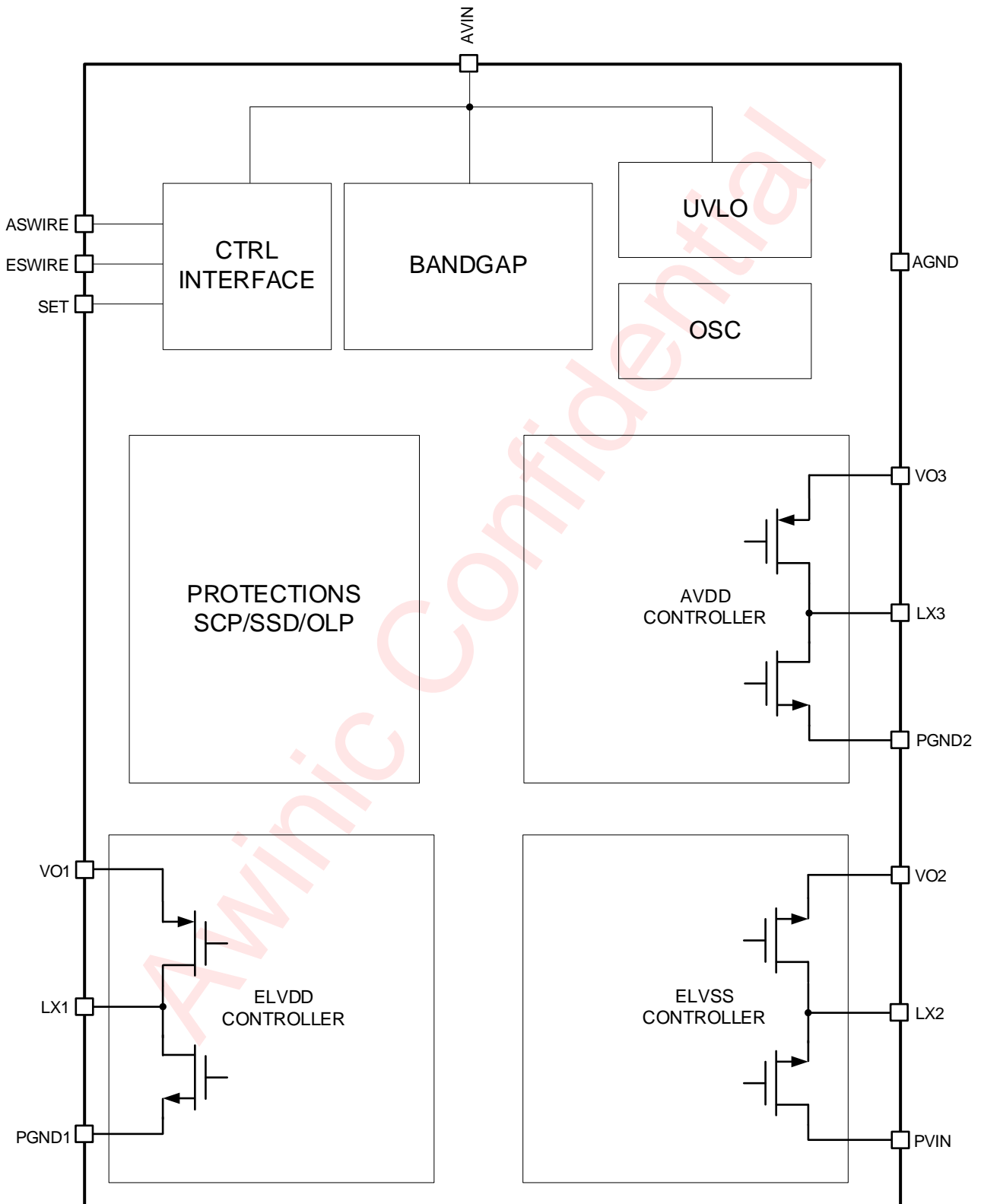
## PIN CONFIGURATION AND TOP MARK



## PIN DEFINITION

| Ball No.   | Symbol | I/O    | Description   |
|------------|--------|--------|---|
| D1, E1     | LX1    | Output | Switching node of ELVDD Boost converter                   |
| D2, E2, E3 | VO1    | Output | Output voltage of ELVDD Boost converter                   |
| B1, C1, C2 | PGND1  | GND    | Power ground for ELVDD Boost converter                    |
| C4, C5, D5 | LX2    | Output | Switching node of ELVSS inverting Buck-Boost converter    |
| D4, E4, E5 | VO2    | Output | Output voltage of ELVSS inverting Buck-Boost converter    |
| A5, B4, B5 | PVIN   | Input  | Input supply voltage for Power                            |
| A2         | LX3    | Output | Switching node of AVDD Boost converter                    |
| A1         | VO3    | Output | Output voltage of AVDD Boost converter                    |
| B2         | PGND2  | GND    | Power ground for AVDD Boost converter                     |
| A4         | AVIN   | Input  | Input supply voltage for analog                           |
| A3         | AGND   | GND    | Analog ground   |
| D3         | ESWIRE | Input  | S-wire control input (Active-High) for ELVSS              |
| C3         | ASWIRE | Input  | S-wire control input (Active-High) for AVDD and FD enable |
| B3         | SET    | Input  | GPIO input to select AVDD output voltage range            |

FUNCTIONAL BLOCK DIAGRAM



## ORDERING INFORMATION

| Part Number | Temperature  | Package                  | Marking | Moisture Sensitivity Level | Environmental Information | Delivery Form                |
|-------------|--------------|--------------------------|---------|----------------------------|---------------------------|------------------------------|
| AW37577ECSR | -40°C ~ 85°C | WLCSP<br>2.05X2.05 - 25B | A0FG    | MSL1                       | RoHS+HF                   | 3000 units/<br>Tape and Reel |

ABSOLUTE MAXIMUM RATINGS<sup>(NOTE1)</sup>

| PARAMETERS   |                     | RANGE                      |
|--|---------------------|----------------------------|
| Supply voltage range AVIN, PVIN                      |                     | -0.3V to 6V                |
| Input voltage range                                  | ASWIRE, ESWIRE, SET | -0.3V to 6V                |
| Output voltage range                                 | VO1                 | -0.3V to 6V                |
|  | LX1                 | -0.3V to 7V                |
|  | VO3                 | -0.3V to 10V               |
|  | LX3                 | -0.3V to VO3+0.3V          |
|  | VO2                 | -8V to -0.3V               |
|  | LX2                 | -8V to PVIN+0.3V           |
| Junction-to-ambient thermal resistance $\theta_{JA}$ |                     | 69°C/W                     |
| Operating free-air temperature range $T_A$           |                     | -40°C to 85°C              |
| Operating junction temperature range $T_J$           |                     | -40°C to 125°C             |
| Maximum operating junction temperature $T_{JMAX}$    |                     | 160°C                      |
| Storage temperature $T_{STG}$                        |                     | -65°C to 160°C             |
| Lead temperature (soldering 10 seconds)              |                     | 260°C                      |
| ESD(Including HBM CDM) <sup>(NOTE 2)</sup>           |                     |                            |
| HBM  |                     | ±2kV                       |
| CDM  |                     | ±1.5kV                     |
| Latch-Up   |                     |                            |
| Test condition:<br>JEDEC78E                          |                     | +IT: +200mA<br>-IT: -200mA |

**NOTE1:** Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

**NOTE2:** The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017. ESDA/JEDEC JS-002-2018(CDM).

## Recommended Operating Conditions

| Symbol                   | Parameter                            | Min.             | Typ. | Max. | Unit               |
|--------------------------|--------------------------------------|------------------|------|------|--------------------|
| $V_{IN}$                 | Input voltage                        | 2.5              | 3.7  | 5    | V                  |
| $C_{IN}$                 | Input capacitance                    | 40               | 66   |      | $\mu\text{F}$      |
| $C_{OUT}(\text{NOTE 3})$ | Output capacitance                   | $C_{OUT}$ of VO1 | 44   |      | $\mu\text{F}$      |
|                          |                                      | $C_{OUT}$ of VO2 | 44   |      | $\mu\text{F}$      |
|                          |                                      | $C_{OUT}$ of VO3 | 22   |      | $\mu\text{F}$      |
| $L_1(\text{NOTE 4})$     | Inductance for VO1                   | 2.2              | 4.7  |      | $\mu\text{H}$      |
| $L_2$                    | Inductance for VO2                   |                  | 2.2  |      | $\mu\text{H}$      |
| $L_3$                    | Inductance for VO3                   |                  | 10   |      | $\mu\text{H}$      |
| $T_A$                    | Operating free-air temperature range | -40              | 25   | 85   | $^{\circ}\text{C}$ |

**NOTE3:** The minimum value of the required capacitor for 800mA load at  $V_{VO1} = 4.6\text{V}$  or  $V_{VO2} = -4.0\text{V}$  is 13.2 $\mu\text{F}$  and for 150mA load at  $V_{VO3} = 7.6\text{V}$  is 3.9 $\mu\text{F}$ .

**NOTE4:** To improve the combined efficiency at heavy load and maximum output current capability of VO1 and VO2, the inductance for VO1 can be replaced with a value of 2.2 $\mu\text{H}$ .

## ELECTRICAL CHARACTERISTICS

AVIN = PVIN = 3.7V, typical values are at  $T_A = T_J = 25^\circ\text{C}$  (unless otherwise noted)

| PARAMETER   |   | TEST CONDITIONS  | MIN  | TYP            | MAX  | UNIT             |
|---|---|--|------|----------------|------|------------------|
| <b>SUPPLY CURRENT AND THERMAL PROTECTION</b>      |   |  |      |                |      |                  |
| AVIN, PVIN  | Input voltage range                       |  | 2.5  | 3.7            | 5    | V                |
| $I_{SD}$  | Shutdown current                          | ESWIRE = ASWIRE = GND, total current flowing into AVIN and PVIN    |      |                | 1    | $\mu\text{A}$    |
| $I_Q$   | Quiescent current                         | ESWIRE = ASWIRE = HIGH, total current flowing into AVIN and PVIN   |      |                | 5    | mA               |
| $V_{UVLO}$  | Under-voltage lockout threshold           | AVIN Falling   | 2.10 |                | 2.25 | V                |
|   |   | AVIN Rising  | 2.27 |                | 2.45 | V                |
| $T_{SD}$  | Thermal shutdown temperature              | Temperature Rising   |      | 160            |      | $^\circ\text{C}$ |
| <b>ELVDD BOOST CONVERTER(VO1)</b>                 |   |  |      |                |      |                  |
| $V_{VO1}$   | Output voltage                            |  | 4.6  | 4.6            | 5    | V                |
|   | Output voltage accuracy                   | No load  | -0.5 |                | 0.5  | %                |
|   |   | No load, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$          | -0.8 |                | 0.8  | %                |
| $I_{O1MAX}$ (NOTE 5)                              | Maximum Output Current                    | AVIN = PVIN = 2.5V ~ 5.0V, $V_{VO2} = -4\text{V}$                  | 600  |                |      | mA               |
|   |   | AVIN = PVIN = 3.2V ~ 5.0V, $V_{VO2} = -6\text{V}$                  | 750  |                |      | mA               |
|   |   | AVIN = PVIN = 3.2V ~ 5.0V, $V_{VO2} = -5\text{V}$                  | 800  |                |      | mA               |
|   |   | AVIN = PVIN = 3.4V ~ 5.0V, $V_{VO2} = -6\text{V}$                  | 800  |                |      | mA               |
|   |   | AVIN = PVIN = 3.0V ~ 5.0V, $V_{VO2} = -4\text{V}$                  | 850  |                |      | mA               |
| $R_{DS(ON)}$                                      | Switch on-resistance                      | $I_{DS} = 200\text{ mA}$   |      | 120            |      | $\text{m}\Omega$ |
| $R_{DS(ONR)}$                                     | Rectifier on-resistance                   |  |      | 140            |      | $\text{m}\Omega$ |
| $f_{SW1}$   | Switching frequency                       |  |      | 1.45           |      | MHz              |
|   |   |  | -8   |                | 8    | %                |
| $I_{LIMIT1}$                                      | Switch current limit                      | Inductor peak current  | 2.20 | 2.75           | 3.30 | A                |
| $V_{SCP1}$  | Short-circuit threshold in operation      | Voltage decrease from nominal $V_{VO1}$                            |      | 0.9x $V_{VO1}$ |      | V                |
| $t_{SCP1}$  | Short-circuit detection time in operation |  |      | 1              |      | ms               |
| $R_{DCHG}$  | Discharge resistance                      | FD = ON, $I_{O1} = 1\text{ mA}$                                    | 30   | 50             | 70   | $\Omega$         |
| Line Regulation                                   | $V_{VO1\_LINEREG}$                        | $I_{O1} = 100\text{ mA}$ , $V_{IN} = 2.5\text{V}$ to $4.5\text{V}$ |      | 0.018          |      | %/V              |
| Load Regulation                                   | $V_{VO1\_LOADREG}$                        | $I_{O1} = 1\text{ mA} \sim 600\text{ mA}$                          |      | 0.3            |      | %/A              |
| <b>ELVSS INVERTING BUCK-BOOST CONVERTER (VO2)</b> |   |  |      |                |      |                  |
| $V_{VO2}$   | Output voltage range                      |  | -6.6 | -4.0           | -1.0 | V                |
|   | Output voltage accuracy                   | No load  | -25  |                | 25   | mV               |
|   |   | No load, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$          | -40  |                | 40   | mV               |
| $I_{O2MAX}$ (NOTE 5)                              | Maximum Output Current                    | AVIN = PVIN = 2.5V ~ 5.0V, $V_{VO2} = -4\text{V}$                  |      |                | -600 | mA               |
|   |   | AVIN = PVIN = 3.2V ~ 5.0V, $V_{VO2} = -6\text{V}$                  |      |                | -750 | mA               |
|   |   | AVIN = PVIN = 3.2V ~ 5.0V, $V_{VO2} = -5\text{V}$                  |      |                | -800 | mA               |
|   |   | AVIN = PVIN = 3.4V ~ 5.0V, $V_{VO2} = -6\text{V}$                  |      |                | -800 | mA               |
|   |   | AVIN = PVIN = 3.0V ~ 5.0V, $V_{VO2} = -4\text{V}$                  |      |                | -850 | mA               |

|                                      |  |   |      |                          |      |     |
|--------------------------------------|--|---|------|--------------------------|------|-----|
| R <sub>DSONS</sub>                   | Switch on-resistance                                 | I <sub>DS</sub> = 200 mA                                |      | 120                      |      | mΩ  |
| R <sub>DSONR</sub>                   | Rectifier on-resistance                              |   |      | 70                       |      | mΩ  |
| f <sub>SW2</sub>                     | Switching frequency                                  |   |      | 1.45                     |      | MHz |
|                                      |  |   |      | -8                       | 8    | %   |
| I <sub>LIMIT2</sub>                  | Switch current limit                                 | AVIN = PVIN = 2.5 V                                     | 3.60 | 4.60                     | 5.60 | A   |
| R <sub>DCHG</sub>                    | Discharge resistance                                 | FD = ON, I <sub>O2</sub> = 1 mA                         | 30   | 50                       | 70   | Ω   |
| V <sub>SCP2</sub>                    | Short circuit threshold in operation                 | Voltage increase from nominal V <sub>VO2</sub>          |      | 0.9x<br>V <sub>VO2</sub> |      | V   |
| t <sub>SCP2</sub>                    | Short circuit detection time in operation            |   |      | 1                        |      | ms  |
| V <sub>SSD</sub>                     | Start-up short detection threshold                   |   |      | 200                      |      | mV  |
| t <sub>SSD</sub>                     | Start-up short detection time                        |   |      | 10                       |      | ms  |
| Line Regulation                      | V <sub>VO2_LINEREG</sub>                             | I <sub>O2</sub> = 100mA, V <sub>IN</sub> = 2.5V to 4.5V |      | 0.03                     |      | %/V |
| Load Regulation                      | V <sub>VO2_LINEREG</sub>                             | I <sub>O2</sub> = 1mA ~ 600mA                           |      | 0.3                      |      | %/A |
| <b>AVDD BOOST CONVERTER (VO3)</b>    |  |   |      |                          |      |     |
| V <sub>VO3</sub>                     | Output voltage                                       | SET = HIGH  | 6.9  | 7.6                      | 7.9  | V   |
|                                      |  | SET = LOW   | 7.1  | 7.6                      | 7.8  | V   |
|                                      | Output voltage accuracy                              | No load   | -0.8 |                          | 0.8  | %   |
|                                      |  | No load, T <sub>A</sub> = -40°C to +85°C                | -1.0 |                          | 1.0  | %   |
| I <sub>O3MAX</sub>                   | Maximum Output Current                               | AVIN = PVIN = 2.5V ~ 5.0V                               | 150  |                          |      | mA  |
| R <sub>DSONS</sub>                   | Switch on-resistance                                 | I <sub>DS</sub> = 30 mA                                 |      | 250                      |      | mΩ  |
| R <sub>DSONR</sub>                   | Rectifier on-resistance                              |   |      | 750                      |      | mΩ  |
| f <sub>SW3</sub>                     | Switching frequency                                  |   |      | 1.45                     |      | MHz |
|                                      |  |   |      | -8                       | 8    | %   |
| I <sub>LIMIT3</sub>                  | Switch current limit                                 | Inductor peak current                                   | 0.9  | 1.1                      | 1.3  | A   |
| R <sub>DCHG</sub>                    | Discharge resistance                                 | FD = ON, I <sub>O3</sub> = 1 mA                         | 30   | 50                       | 70   | Ω   |
| V <sub>SCP3</sub>                    | Short-circuit threshold in operation                 | Voltage decrease from nominal V <sub>VO3</sub>          |      | 0.9x<br>V <sub>VO3</sub> |      | V   |
| t <sub>SCP3</sub>                    | Short-circuit detection time in operation            |   |      | 1                        |      | ms  |
| Line Regulation                      | V <sub>VO3_LINEREG</sub>                             | I <sub>O3</sub> = 50mA, V <sub>IN</sub> = 2.5V to 4.5V  |      | 0.05                     |      | %/V |
| Load Regulation                      | V <sub>VO3_LINEREG</sub>                             | I <sub>O3</sub> = 1mA ~ 150mA                           |      | 0.25                     |      | %/A |
| <b>LOGIC SET</b>                     |  |   |      |                          |      |     |
| V <sub>IH</sub>                      | High level input voltage                             | AVIN = PVIN = 2.5V ~ 5.0V                               | 0.84 |                          |      | V   |
| V <sub>IL</sub>                      | Low level input voltage                              | AVIN = PVIN = 2.5V ~ 5.0V                               |      |                          | 0.4  | V   |
| <b>CTRL INTERFACE(ASWIRE,ESWIRE)</b> |  |   |      |                          |      |     |
| V <sub>IH</sub>                      | High level input voltage                             | AVIN = PVIN = 2.5V ~ 5.0V                               | 0.84 |                          |      | V   |
| V <sub>IL</sub>                      | Low level input voltage                              | AVIN = PVIN = 2.5V ~ 5.0V                               |      |                          | 0.4  | V   |
| R <sub>SWIRE</sub>                   | Pull down resistance of ASWIRE and ESWIRE interfaces | V <sub>SWIRE</sub> =1.8V                                |      | 270                      |      | kΩ  |

|                             |  |         |     |     |     |    |
|-----------------------------|--|---------|-----|-----|-----|----|
| t <sub>LOW</sub> (NOTE 6)   | Low-level pulse duration                     |         | 2   | 10  | 25  | μs |
| t <sub>HIGH</sub> (NOTE 6)  | High-level pulse duration                    |         | 2   | 10  | 25  | μs |
| t <sub>OFF</sub> (NOTE 6)   | Shutdown pulse duration(ASWIRE/ESWIRE = low) |         | 200 |     |     | μs |
| t <sub>INIT</sub> (NOTE 6)  | Initialization time                          |         |     | 300 | 400 | μs |
| t <sub>STORE</sub> (NOTE 6) | Data storage/accept time period              |         | 160 |     |     | μs |
| <b>POWER SEQUENCE</b>       |  |         |     |     |     |    |
| t <sub>DELAY</sub> (NOTE 6) | VO2 start up time delay<br>VO1               | SSD ON  |     | 7   |     | ms |
|                             |  | SSD OFF |     | 0   |     | ms |

NOTE5: The specific parameters of the peripheral inductors are as follows:

L1: DFE252012F-4R7M=P2 2.4A, 160mΩ, 252012 L2: DFE252012F-2R2M=P2 3.6A, 68mΩ, 252012

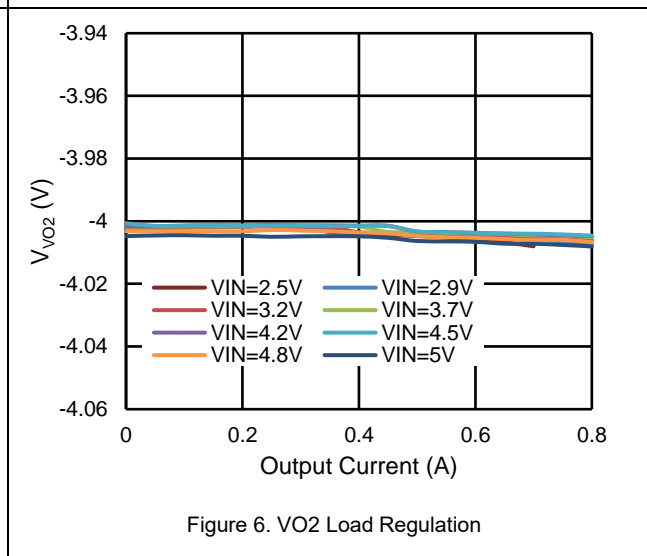
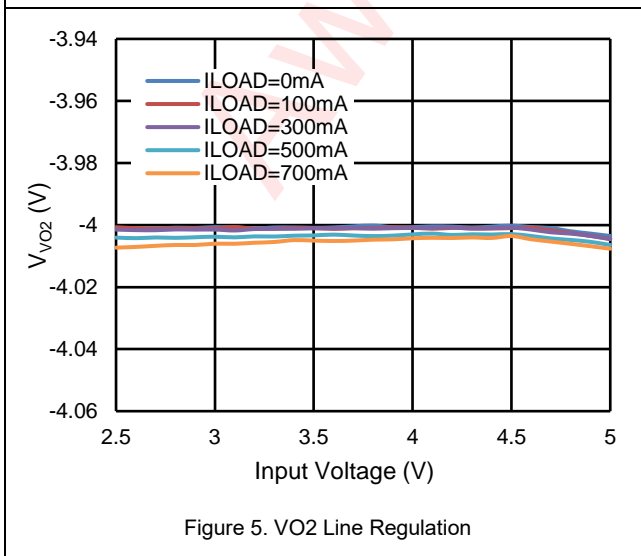
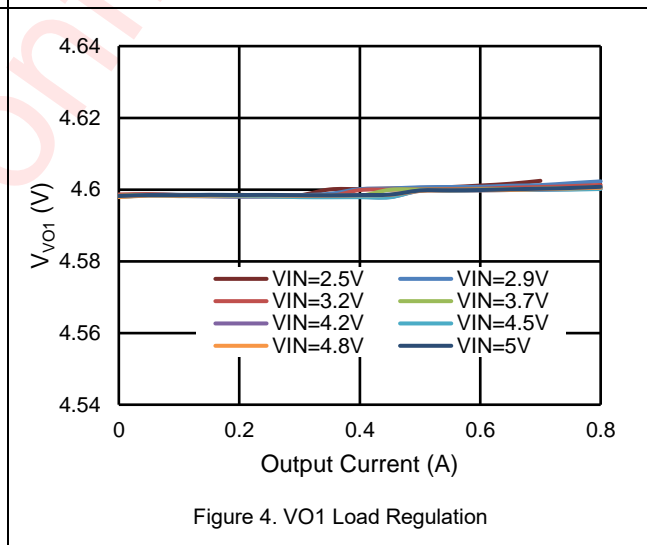
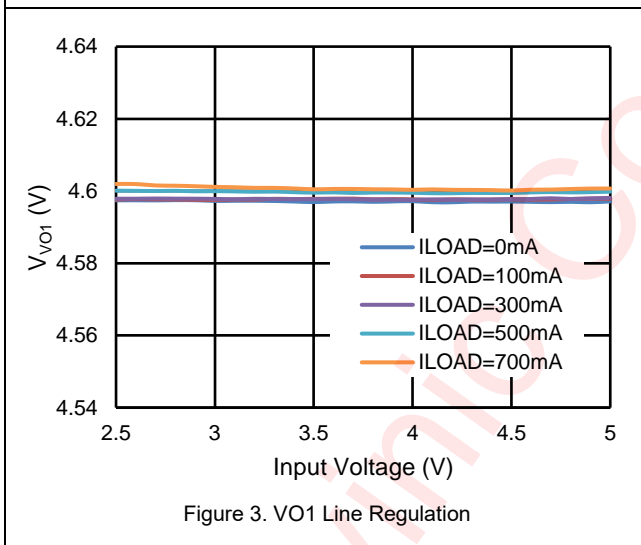
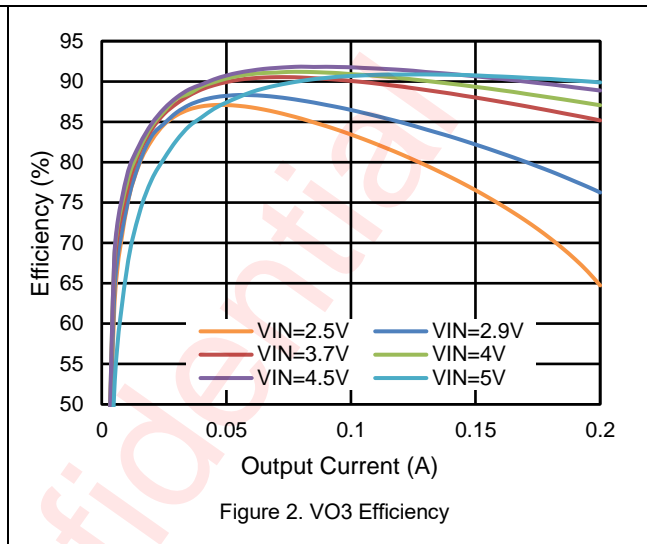
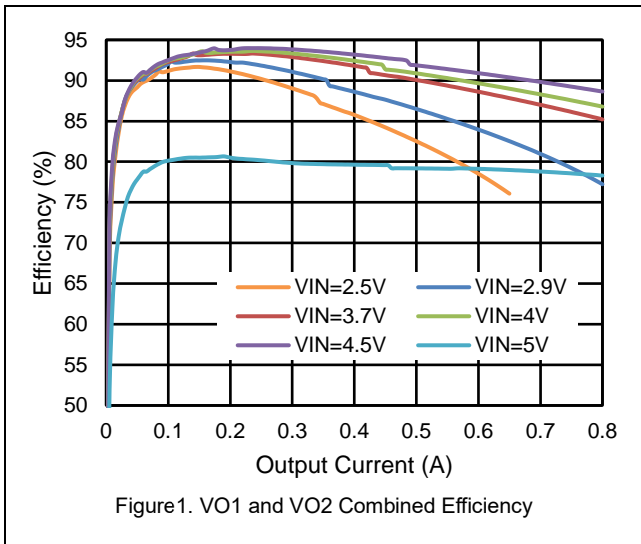
L3: DFE252012F-100M=P2 1.6A, 400mΩ, 252012

Test Condition: Ambient temperature is 60°C, the load current is only between the VO1 and VO2, VO3 is no load, AW37577E works stably in laboratory test environment.

NOTE6: Guaranteed by design characterization and correlation with process controls. Not fully test in production.

## TYPICAL CHARACTERISTICS

$AVIN = PVIN = VIN = 3.7V$ ,  $V_{VO1} = 4.6V$ ,  $V_{VO2} = -4V$ ,  $V_{VO3} = 7.6V$ . Typical values are at  $T_A = T_J = 25^\circ C$  (unless otherwise noted)



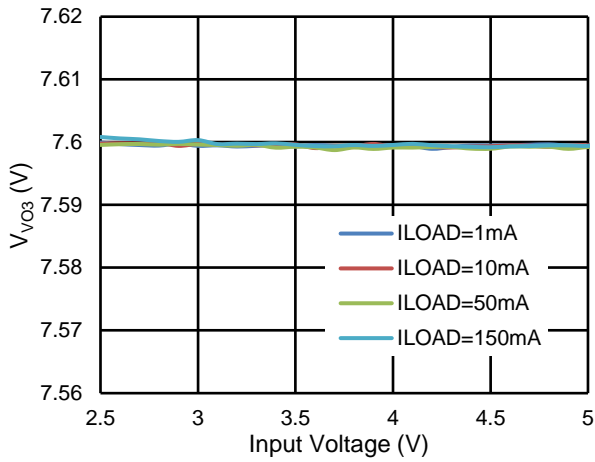


Figure 7. VO3 Line Regulation

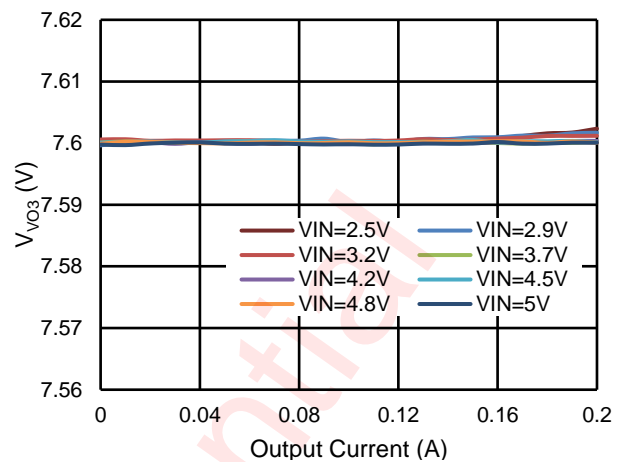


Figure 8. VO3 Load Regulation

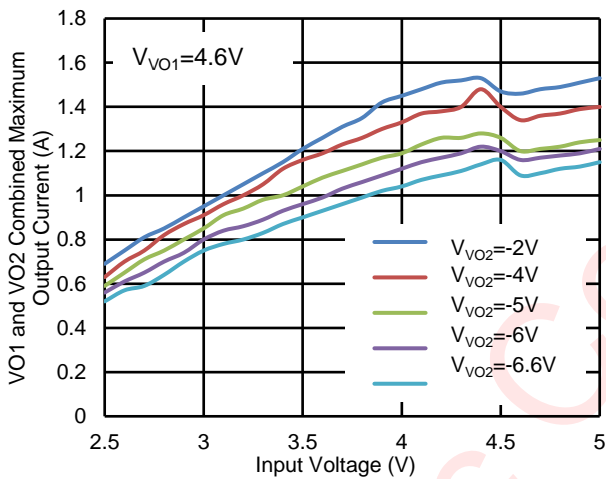


Figure 9. VO1 and VO2 Combined Maximum Output Current<sup>(NOTE5,6)</sup>

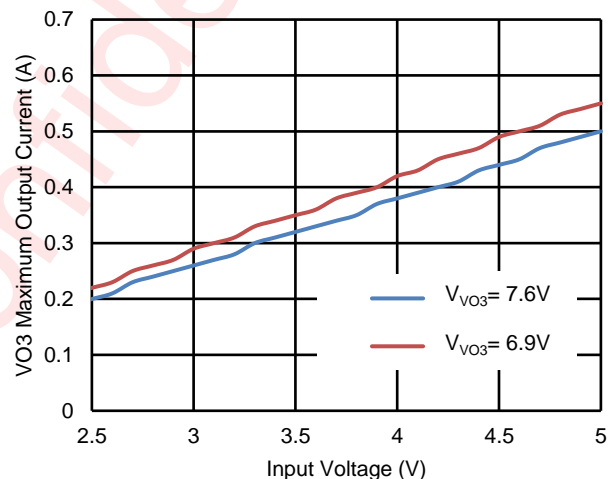


Figure 10. VO3 Maximum Output Current<sup>(NOTE5,6)</sup>

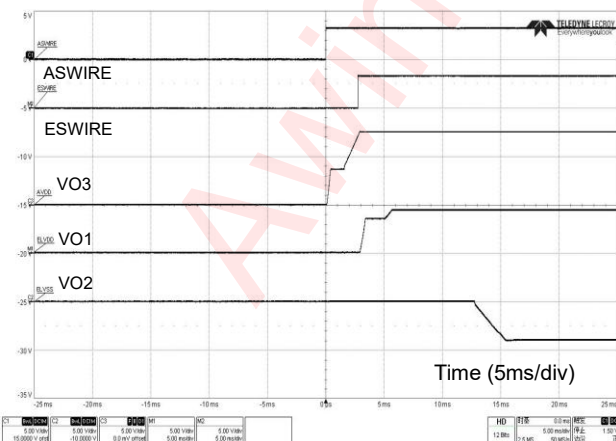


Figure 11. Start up Sequence  
(ASWIRE starts 3ms before ESWIRE)

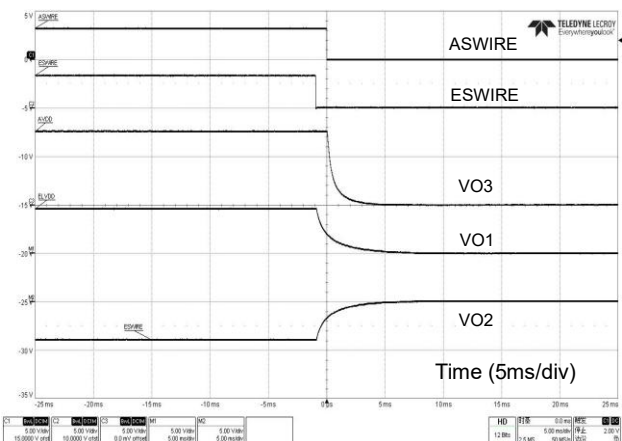


Figure 12. Shut down Sequence with FD ON  
(ASWIRE stops 1ms later than ESWIRE)

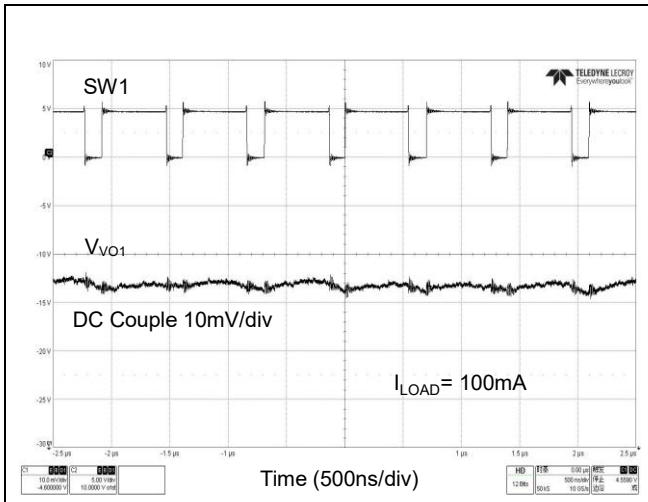


Figure 13. VO1 Switching and Output Waveforms

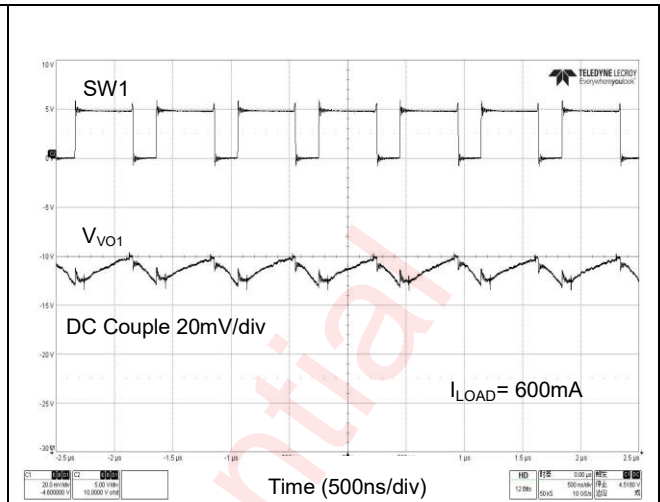


Figure 14. VO1 Switching and Output Waveforms

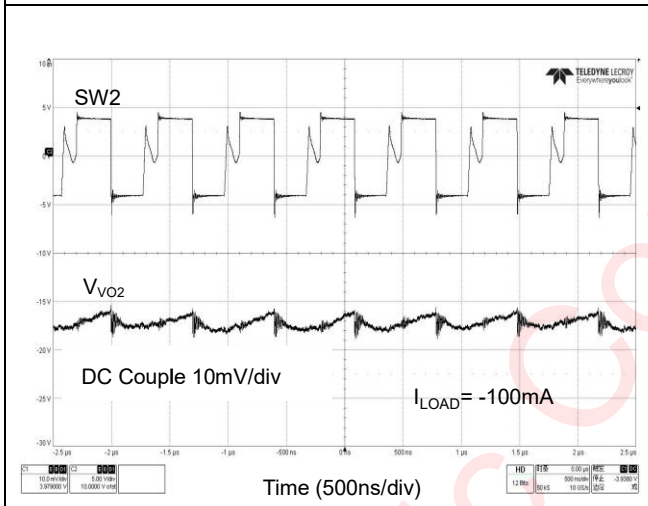


Figure 15. VO2 Switching and Output Waveforms

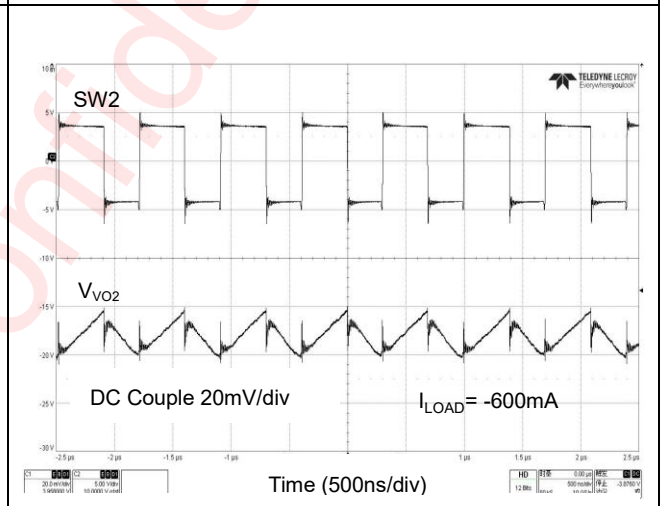


Figure 16. VO2 Switching and Output Waveforms

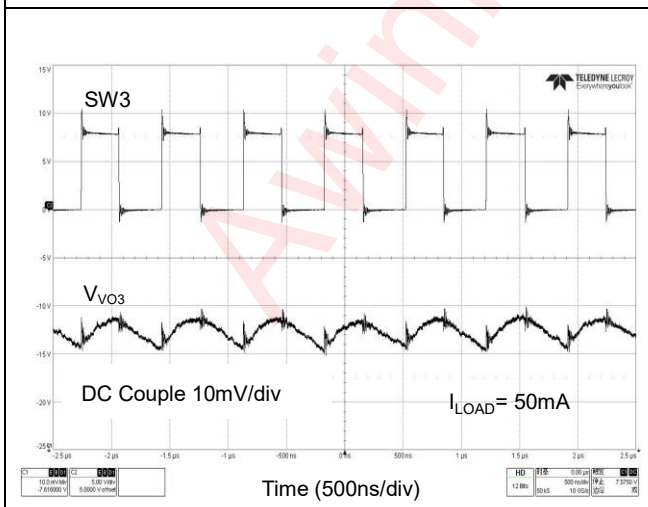


Figure 17. VO3 Switching and Output Waveforms

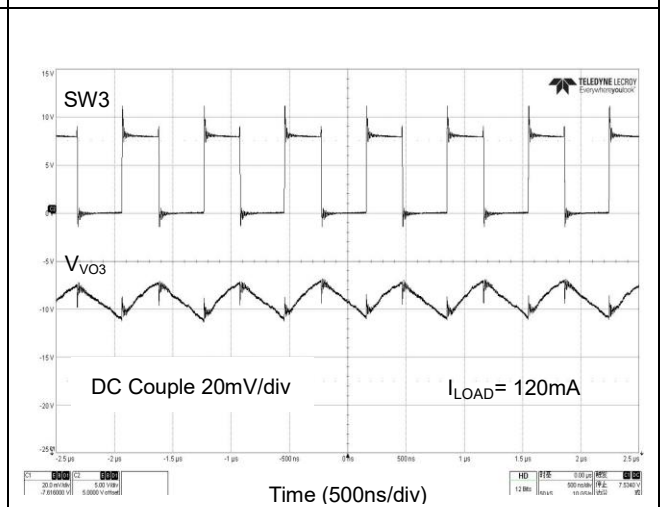


Figure 18. VO3 Switching and Output Waveforms

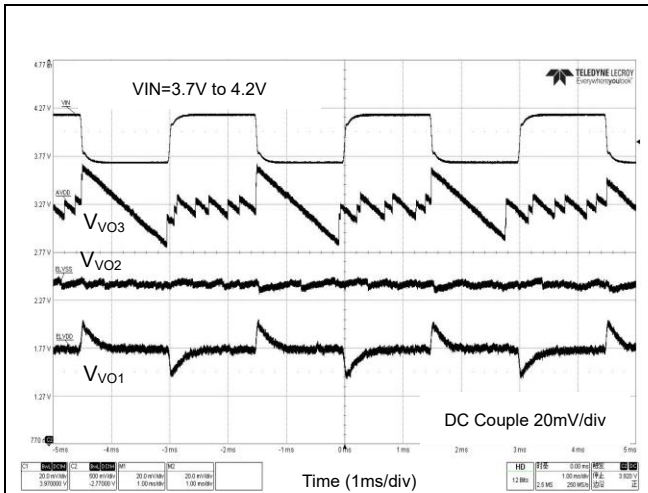


Figure 19. Line transient at No Load

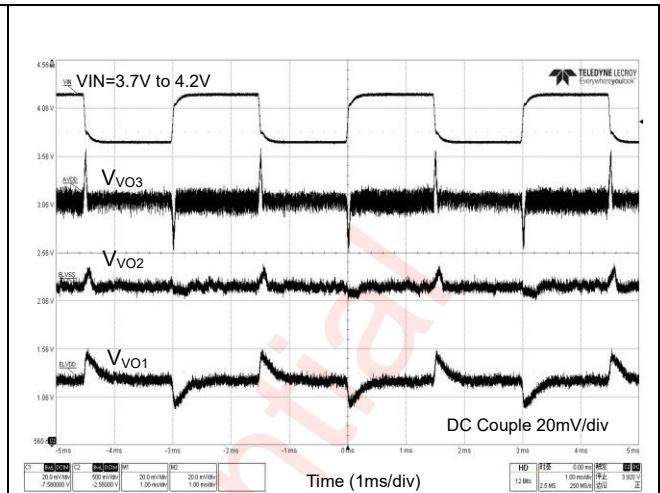


Figure 20. Line transient at Light Load (10mA)

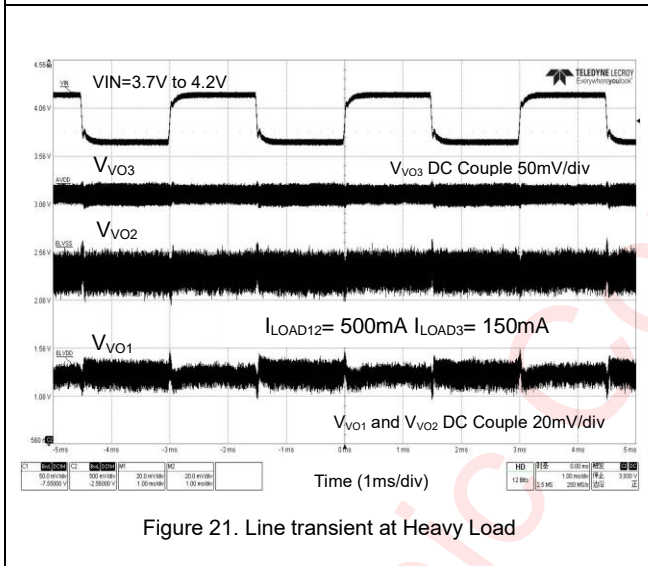


Figure 21. Line transient at Heavy Load

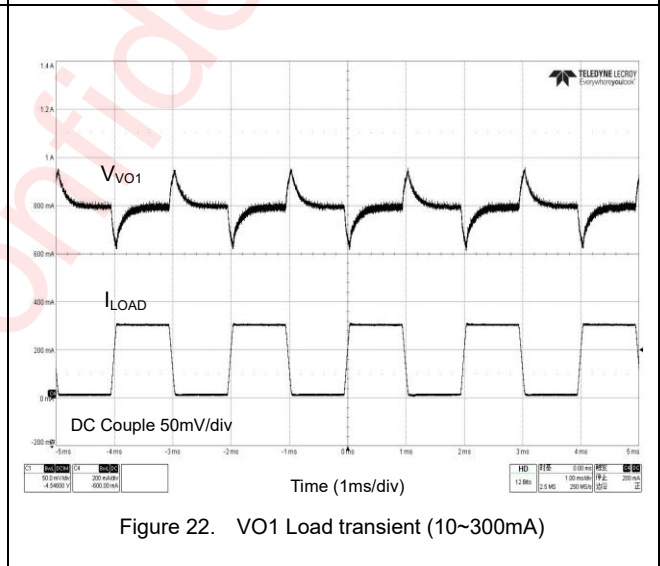


Figure 22. VO1 Load transient (10~300mA)

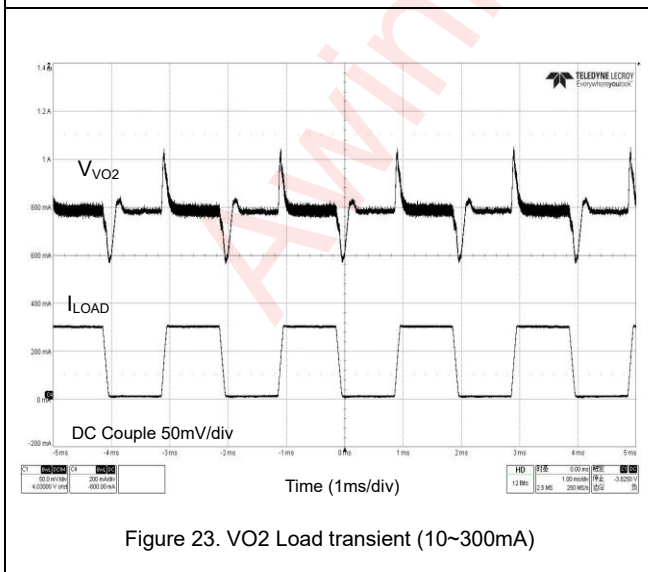


Figure 23. VO2 Load transient (10~300mA)

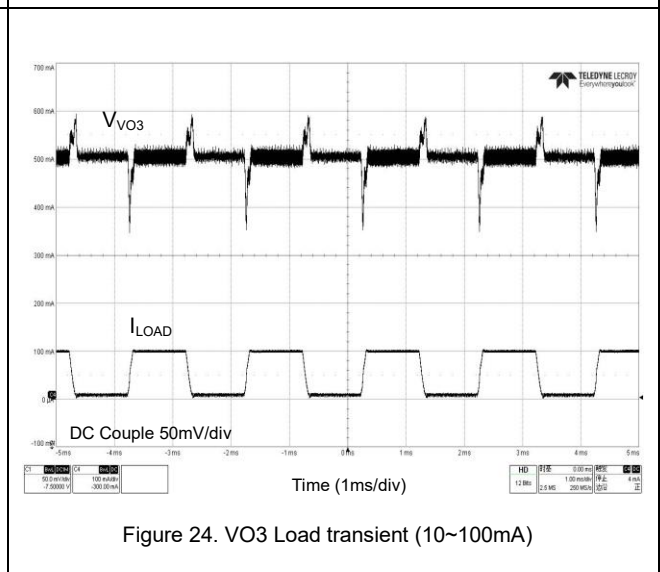


Figure 24. VO3 Load transient (10~100mA)

## DETAILED FUNCTIONAL DESCRIPTION

### Sequence

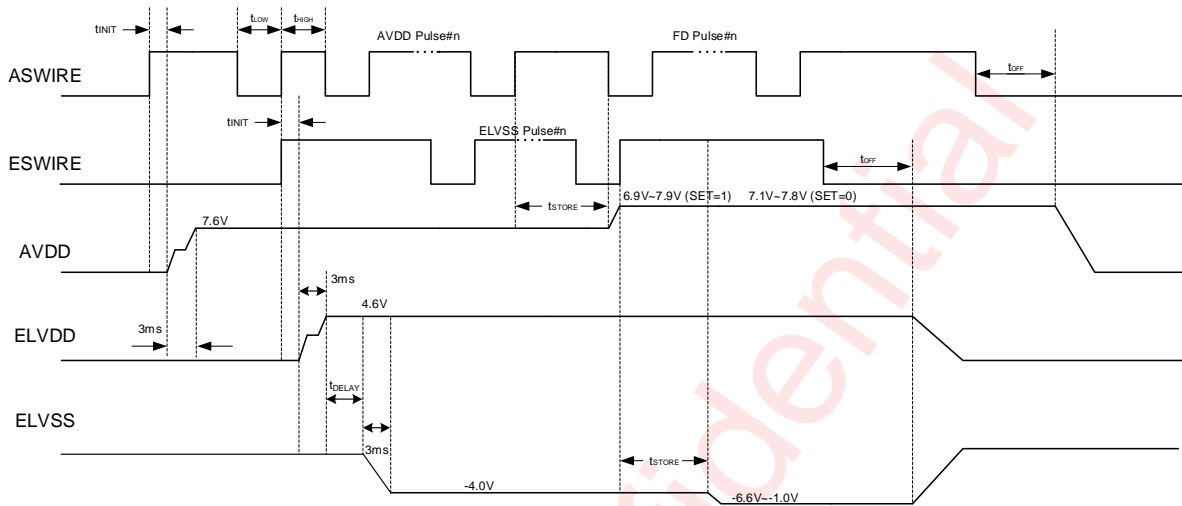


Figure 25. Timing diagram

The AVDD boost converter operates with a cycle-by-cycle peak current limit topology and fixed 1.45MHz frequency. The AVDD output voltage can be programmed through ASWIRE interface, and the output voltage table can be changed by the condition of SET interface. When SET = LOW, AVDD is available from 7.1V to 7.8V with 100mV steps, while SET = HIGH, AVDD is available from 6.9V to 7.9V with 50mV steps. The programming table of AVDD output voltage is shown in Table 1.

The AVDD boost converter begins soft-start to its default voltage 7.6V with a  $t_{INIT}$  time delay after the ASWIRE logic level goes high. The soft-start lasts for 3ms typically.

The AVDD output voltage is programmable by applying different pulses to ASWIRE interface, which counts the rise edges, plus a high logic level to ASWIRE lasts longer than a  $t_{STORE}$  time is detected after control pulses stop, AVDD starts altering to the target voltage. The AVDD boost converter turns off with a  $t_{OFF}$  time delay after the logic level of ASWIRE interface goes from high to low.

Table 1. Programming of AVDD output voltage

| SET=0        |      | SET=1        |       |
|--------------|------|--------------|-------|
| ASWIRE Pulse | AVDD | ASWIRE Pulse | AVDD  |
| 0            | 7.6V | 0            | 7.60V |
| 1            | 7.8V | 1            | 7.90V |
| 2            | 7.7V | 2            | 7.85V |
| 3            | 7.6V | 3            | 7.80V |
| 4            | 7.5V | 4            | 7.75V |
| 5            | 7.4V | 5            | 7.70V |
| 6            | 7.3V | 6            | 7.65V |

| SET=0        |      | SET=1        |              |
|--------------|------|--------------|--------------|
| ASWIRE Pulse | AVDD | ASWIRE Pulse | AVDD         |
| 7            | 7.2V | 7            | <b>7.60V</b> |
| 8            | 7.1V | 8            | 7.55V        |
|              |      | 9            | 7.50V        |
|              |      | 10           | 7.45V        |
|              |      | 11           | 7.40V        |
|              |      | 12           | 7.35V        |
|              |      | 13           | 7.30V        |
|              |      | 14           | 7.25V        |
|              |      | 15           | 7.20V        |
|              |      | 16           | 7.15V        |
|              |      | 17           | 7.10V        |
|              |      | 18           | 7.05V        |
|              |      | 19           | 7.00V        |
|              |      | 20           | 6.95V        |
|              |      | 21           | 6.90V        |

The inverting buck-boost and boost converters both operate with a cycle-by-cycle peak current limit topology and fixed 1.45MHz frequency. The ELVSS output voltage can be programmed from -6.6V to -1.0V with 100mV steps. The programming table of ELVSS output voltage is shown in Table 2. The ELVDD output voltage can be programmed from 4.6V to 5.0V with 100mV steps by ESWIRE interface as well. The programming table of ELVDD output voltage is shown in Table 3.

The ESWIRE interface controls the on and off state of ELVDD and ELVSS. The ELVDD boost converter begins soft-start to its default voltage 4.6V with a  $t_{INIT}$  time delay after the ESWIRE logic level goes high. When SSD function is on, the ELVSS inverting buck-boost converter with -4V default value starts to operate 10ms later than the ELVDD boost converter; on the other hand, SSD function is off, the ELVSS inverting buck-boost converter with -4V default value starts to operate when the ELVDD output voltage establishes completely.

Both converters are implemented with a 3ms soft-start to limit the inrush current. When ESWIRE interface goes low for  $t_{OFF}$  time, the ELVDD and ELVSS converters stop operation simultaneously.

The ELVDD and ELVSS output voltage both are programmable by applying different pulses to ESWIRE interface, which also counts the rise edges, plus a high logic level of ESWIRE lasts longer than a  $t_{STORE}$  time is detected after controll pulses stop, the ELVDD and ELVSS outputs start altering to the target voltage.

Table 2. Programming of ELVSS output voltage

| ESWIRE Pulse | ELVSS | ESWIRE Pulse | ELVSS |
|--------------|-------|--------------|-------|
| 0            | -4.0V | 31           | -3.6V |
| 1            | -6.6V | 32           | -3.5V |
| 2            | -6.5V | 33           | -3.4V |
| 3            | -6.4V | 34           | -3.3V |
| 4            | -6.3V | 35           | -3.2V |
| 5            | -6.2V | 36           | -3.1V |
| 6            | -6.1V | 37           | -3.0V |
| 7            | -6.0V | 38           | -2.9V |
| 8            | -5.9V | 39           | -2.8V |
| 9            | -5.8V | 40           | -2.7V |
| 10           | -5.7V | 41           | -2.6V |
| 11           | -5.6V | 42           | -2.5V |
| 12           | -5.5V | 43           | -2.4V |
| 13           | -5.4V | 44           | -2.3V |
| 14           | -5.3V | 45           | -2.2V |
| 15           | -5.2V | 46           | -2.1V |
| 16           | -5.1V | 47           | -2.0V |
| 17           | -5.0V | 48           | -1.9V |
| 18           | -4.9V | 49           | -1.8V |
| 19           | -4.8V | 50           | -1.7V |
| 20           | -4.7V | 51           | -1.6V |
| 21           | -4.6V | 52           | -1.5V |
| 22           | -4.5V | 53           | -1.4V |
| 23           | -4.4V | 54           | -1.3V |
| 24           | -4.3V | 55           | -1.2V |
| 25           | -4.2V | 56           | -1.1V |
| 26           | -4.1V | 57           | -1.0V |
| 27           | -4.0V |              |       |
| 28           | -3.9V |              |       |
| 29           | -3.8V |              |       |
| 30           | -3.7V |              |       |

AW37577E operates with an input voltage range of 2.5V to 5.0V. However, due to different input and output voltage, the maximum output current capability is quite different, and also affected by peripheral inductors and capacitors, additional input capacitors are recommended for lower input supply voltage.

AW37577E also has the slew rate control during the transition of the ELVSS output voltage, which aims to accomplish smooth voltage changes. The ramp time is 90 $\mu$ s typically, step is 100mV, the wider the transition range of the ELVSS output voltage, the longer the transition time.

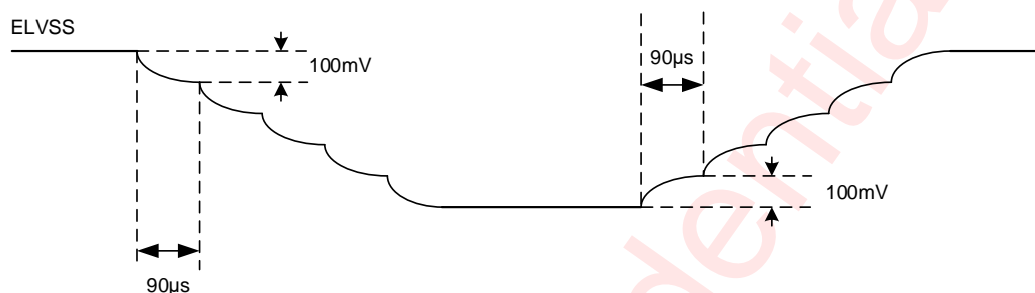


Figure 26. The output voltage of ELVSS transition time

Table 3. Programming of ELVDD output voltage

| ESWIRE Pulse | ELVDD |
|--------------|-------|
| 0/no pulse   | 4.6V  |
| 76           | 5.0V  |
| 77           | 4.9V  |
| 78           | 4.8V  |
| 79           | 4.7V  |

### Under Voltage Lock-Out

Under Voltage Lock-Out (UVLO) is implemented to detect the input voltage AVIN. Once AVIN drops below UVLO falling threshold, all of the three converters (AVDD, ELVDD and ELVSS) stop switching; If AVIN increases above UVLO rising threshold, the three converters restart switching and resume to their previous settings.

### Start-up Short Detection (SSD)

The start-up short detection block detects the ELVSS output voltage to monitor whether ELVSS and ELVDD are short connected. If the ELVSS output voltage is pulled up to 0.2V in 10ms after ESWIRE interface goes high, SSD function is triggered and the ELVDD and ELVSS converters shut down immediately. FD function is on at the same time. Resetting the power supply or pulling the ESWIRE interface low for more than a  $t_{OFF}$  time can restart the device.

SSD function is enabled and disabled by the pulse numbers of ASWIRE interface. Number of controll pulse is set differently depending on the logic condition of SET interface. SSD function is on by default, the pulse numbers are shown in Table 4.

Table 4. ASWIRE pulses for SSD function

| SET=0        |     | SET=1        |     |
|--------------|-----|--------------|-----|
| ASWIRE Pulse | SSD | ASWIRE Pulse | SSD |
| 0/no pulse   | ON  | 0/no pulse   | ON  |
| 9            | OFF | 22           | OFF |
| 10           | ON  | 23           | ON  |

### Fast discharge (FD)

The output voltage (AVDD, ELVDD and ELVSS) fast discharge function is enabled and disabled by the pulse numbers of ASWIRE interface. Number of control pulse is set differently depending on the logic condition of SET interface. The pulse numbers are shown in Table 5, FD function is off by default.

When FD function is active, either ASWIRE or ESWIRE interface keeps high state, all outputs of the device are discharged to GND.

Table 5. ASWIRE pulses for FD function

| SET=0        |     | SET=1        |     |
|--------------|-----|--------------|-----|
| ASWIRE Pulse | FD  | ASWIRE Pulse | FD  |
| 0/no pulse   | OFF | 0/no pulse   | OFF |
| 11           | ON  | 25           | ON  |
| 12           | OFF | 26           | OFF |

### Short Circuit Protection (SCP)

The short circuit protection block monitors the output voltages of the AVDD, ELVDD and ELVSS converters to protect the device of short connections to ground or overload. When an SCP or overload event occurs, all the three converters shut down and FD function is enabled simultaneously. Only resetting the power supply or both pulling the ASWIRE and ESWIRE interface to low at the same time for more than a  $t_{OFF}$  time can restart the device.

An SCP or overload event occurs in the following cases:

- (1) After the output voltages of all the three converters are properly established, if any output voltage falls below 90% of the target voltage and lasts for 1ms;
- (2) In soft-start process,  $V_{ELVDD}$  and  $V_{ELVSS}$  are not in regulation 4ms when ELVDD and ELVSS output voltages begin to establish;
- (3) In soft-start process,  $V_{AVDD}$  is not in regulation 1ms when AVDD output voltage begins to establish.

### Thermal Shut-Down (TSD)

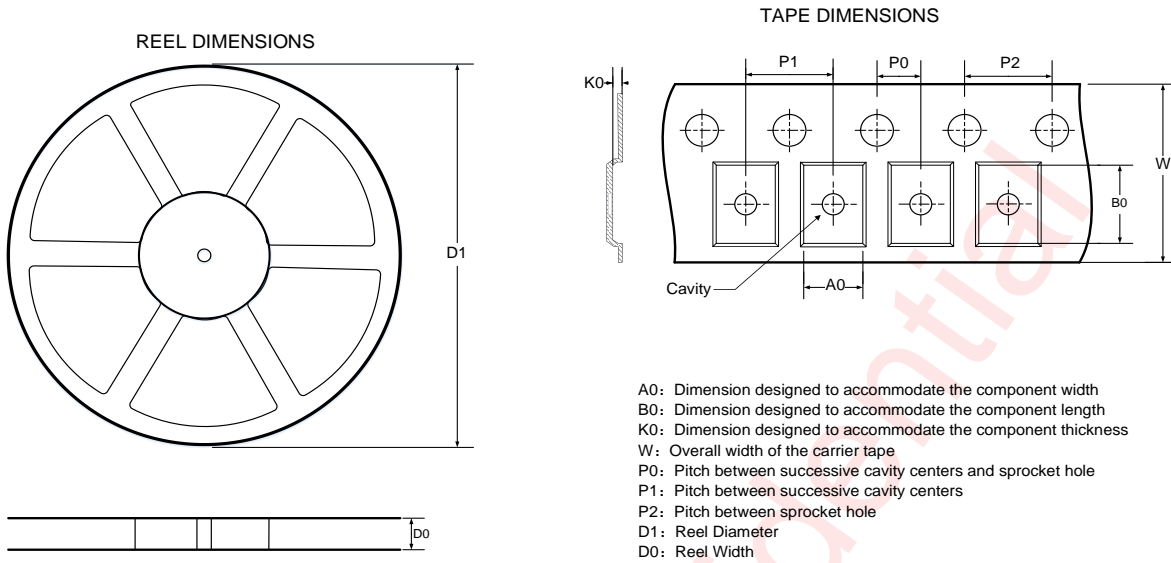
The Thermal Shut-Down (TSD) function protects the device when overheating occurs. If the IC's junction temperature exceeds 160°C, three converters stop operation. It can not exit this state automatically. Pulling the SWIRE interface to low for more than a  $t_{OFF}$  time or a power-cycle on the input supply restarts the device with the default values.

## Device Reset

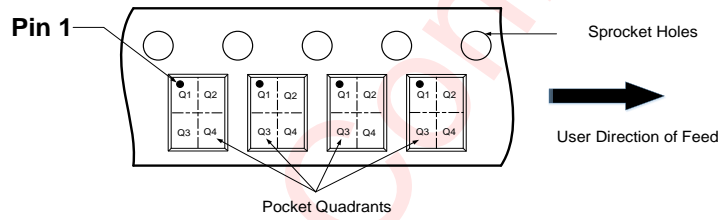
- (1) Power resetting resets the device to default settings;
- (2) Pulling ASWIRE interface low for  $t_{OFF}$  then the output voltage of AVDD is reset to default value of 7.6V;
- (3) Pulling ESWIRE interface low for  $t_{OFF}$  then the output voltage of ELVDD and ELVSS are reset to default value of 4.6V and -4V.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



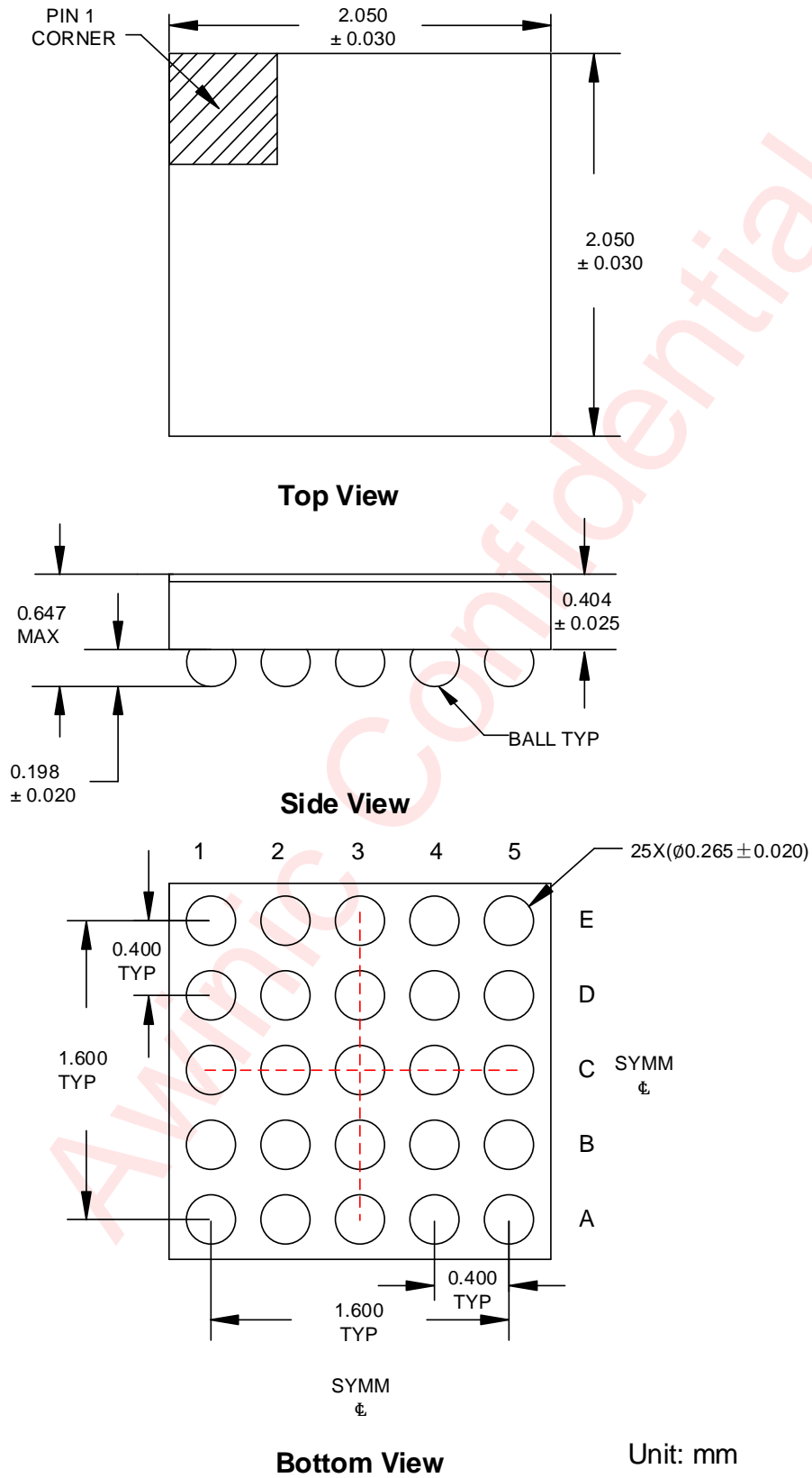
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

### DIMENSIONS AND PIN1 ORIENTATION

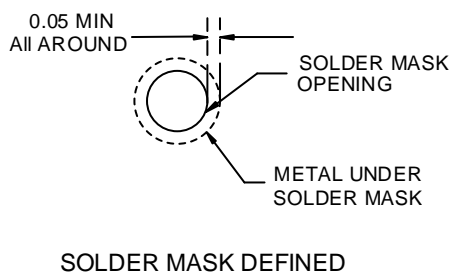
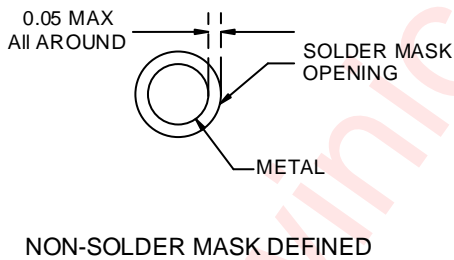
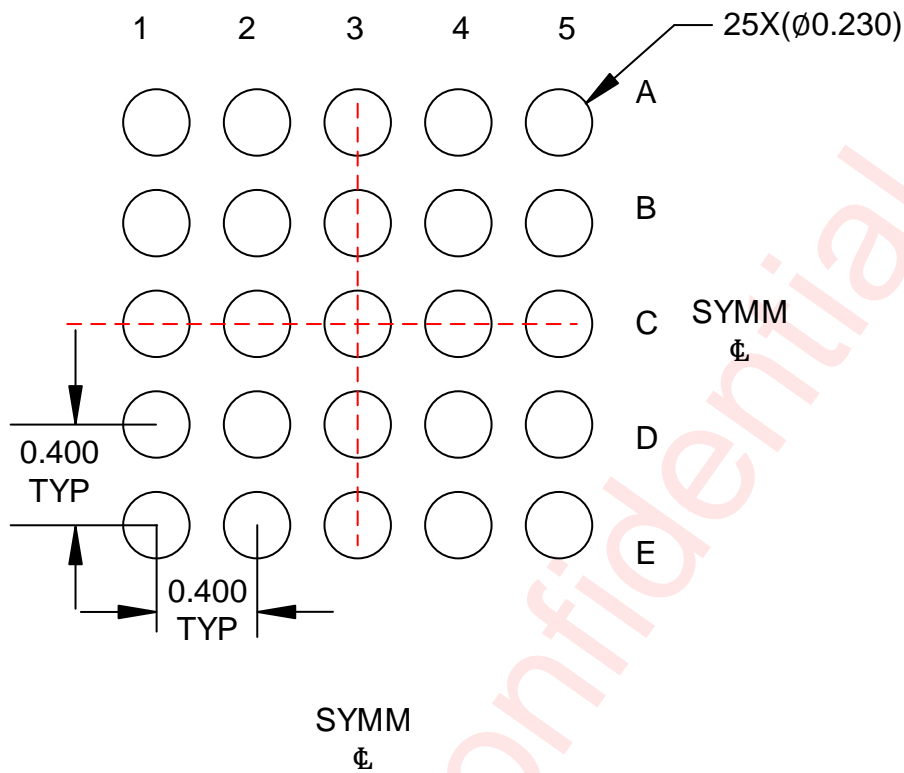
| D1 (mm) | D0 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---------|---------|---------|---------|---------|---------|---------|---------|--------|---------------|
| 179.00  | 9.00    | 2.250   | 2.250   | 0.80    | 2.00    | 4.00    | 4.00    | 8.00   | Q1            |

All dimensions are nominal

**PACKAGE DESCRIPTION**



LAND PATTERN DATA



Unit: mm

## REVISION HISTORY

| Version | Date      | Change Record   |
|---------|-----------|---|
| V1.0    | Dec.2022  | Officially released   |
| V1.1    | Feb. 2023 | Added 1.2V IO description (Page7)   |
| V1.2    | Oct. 2023 | <ol style="list-style-type: none"> <li>Updated the input voltage range from 2.9V~5.0V to 2.5V~5.0V</li> <li>Updated the maximum output current for ELVDD and ELVSS from 700mA to 750mA (Page1)</li> <li>Updated Electrical Characteristics (Page6 ~ Page7)</li> <li>Updated Typical Characteristics (Page8 ~ Page11)</li> <li>Added recovery ways of SSD and SCP (Page 16)</li> </ol>   |
| V1.3    | Jan. 2024 | <ol style="list-style-type: none"> <li>Added the maximum output current of the different ELVSS output voltages in FEATURES (Page1)</li> <li>Added the minimum value of L1 in Recommended Operating Conditions, and added NOTE (Page5)</li> <li>Added the line regulation and load regulation of <math>V_{VO1}</math>, <math>V_{VO2}</math> and <math>V_{VO3}</math> in Electrical Characteristics (Page6 and Page7)</li> <li>Updated Figure9 (Page 10)</li> <li>Updated the detection time of AVDD SCP events in soft-start from 4ms to 1ms (Page 17)</li> </ol>  |
| V1.4    | Jun. 2024 | <ol style="list-style-type: none"> <li>Added the maximum output current at <math>V_{IN}=3.0V</math> and <math>ELVSS=-4V</math> in FEATURES and Electrical Characteristics (Page1 and Page6)</li> <li>Updated the range of LX3 and added the operating junction temperature range in Absolute Maximum Ratings (Page4)</li> <li>Updated the maximum value of <math>V_{UVLO}</math> from 2.40V to 2.45V when AVIN rising (Page6)</li> <li>Updated the range of <math>I_{LIMIT1}</math> (Page6)</li> <li>Added the AVDD boost converter SCP detection threshold and time in operation and updated the range of <math>I_{LIMIT3}</math> (Page7)</li> <li>Updated the maximum value of <math>V_{IL}</math> from 0.36V to 0.4V (Page7)</li> <li>Updated the range of <math>t_{STORE}</math> (Page8)</li> </ol> |
| V1.5    | Aug. 2024 | <ol style="list-style-type: none"> <li>Updated Figure 24 (Page 13)</li> <li>Added the way to configure SSD function through ASWIRE pulses (Page17)</li> </ol>   |
| V1.6    | Apr. 2025 | <ol style="list-style-type: none"> <li>Added the <math>t_{DELAY}</math> time based on SSD function in EC Table (Page 8)</li> <li>Updated the minimum value of <math>t_{STORE}</math> (Page8)</li> <li>Updated Figure 25 (Page 13)</li> <li>Added the delay time description for SSD function in Sequence (Page 14)</li> </ol>   |

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