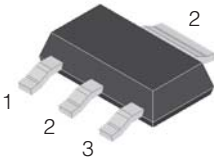
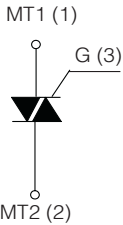



LOGIC LEVEL TRIAC

<p>SOT-223</p>  	<p>On-State Current 1 Amp</p>	<p>Gate Trigger Current < 10 mA</p>	
	<p>Off-State Voltage 400 V ÷ 800 V</p>		
	<p>FEATURES</p> <ul style="list-style-type: none"> • Glass/passivated die junctions • Low current Triac • Ideal for automated placement • Low thermal resistance • High surge current capability • Low forward voltage drop • Solder dip 260°C, 10s • Component in accordance to RoHS 2011/65/EU and WEEE 2002/96/EC • Meets MSL level 3, per J-STD-020, LF maximum peak of 260° C 		
	<p>MECHANICAL DATA</p> <ul style="list-style-type: none"> • Case: SOT-223. Epoxy meets UL 94V-0 flammability rating. • Polarity: As marked on the body. • Terminals: Matte tin plated leads, solderable per MIL-STD-750 Method 2026, J-STD-002 and JESD22-B102. Consumer grade, meets JESD 201 class 1A whisker test. 		
<p>TYPICAL APPLICATIONS</p> <p>Logic level versions are designed to interface directly with low power drivers such as microcontrollers.</p>			

Maximun Ratings and Electrical Characteristics at 25°C

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
$I_{T(RMS)}$	RMS On-state Current (full sine wave)	All Conduction Angle, $T_c = 95\text{ }^\circ\text{C}$	1	A
I_{TSM}	Non-repetitive On-State Current	Full Cycle, 60 Hz ($t = 16.7\text{ ms}$)	8.5	A
I_{TSM}	Non-repetitive On-State Current	Full Cycle, 50 Hz ($t = 20\text{ ms}$)	8	A
I^2t	Fusing Current	$t_p = 10\text{ ms}$, Half Cycle	0.32	A^2s
I_{GM}	Peak Gate Current	20 μs max. $T_j = 125\text{ }^\circ\text{C}$	1	A
$P_{G(AV)}$	Average Gate Power Dissipation	$T_j = 125\text{ }^\circ\text{C}$	0.1	W
di/dt	Critical rate of rise of on-state current	$I_G = 2x I_{GT}$, $t_r \leq 100\text{ ns}$ $f = 120\text{ Hz}$, $T_j = 125\text{ }^\circ\text{C}$	20	$A/\mu\text{s}$
T_j	Operating Temperature		(-40 +125)	$^\circ\text{C}$
T_{stg}	Storage Temperature		(-40 +150)	$^\circ\text{C}$
T_{sld}	Soldering Temperature	10s max	260	$^\circ\text{C}$

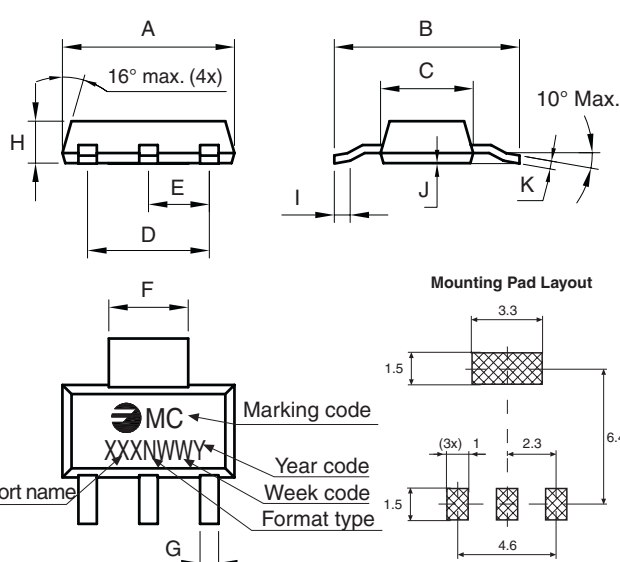
SYMBOL	PARAMETER	VOLTAGE			Unit
		D	M	N	
V_{DRM}/V_{RRM}	Repetitive Peak Off State Voltage	400	600	800	V

LOGIC LEVEL TRIAC

Ordering information

PREFERRED P/N	PACKAGE CODE	DELIVERY MODE	BASE QUANTITY	UNIT WEIGHT (g)
FT0103DN 00RS	RS	REEL	1,000	0.116
FT0103DN 00RB	RB	REEL	2,500	0.116

Package Outline Dimensions: (mm) (SOT-223)



The technical drawing shows the SOT-223 package with dimensions A through K. Dimensions A, B, C, D, E, F, G, H, I, J, and K are defined in millimeters. The package has a maximum lead angle of 16° (4x) and a maximum lead angle of 10°.

Mounting Pad Layout

The mounting pad layout shows three pads with dimensions: 3.3 mm width, 1.5 mm height, and 4.6 mm spacing between pads. The total width of the pads is 6.4 mm.

Marking code layout

The marking code layout shows the following information: MC (Marking code), XXXN (Year code), WWY (Week code), and Format type. The test sort name is also indicated.

REF.	DIMENSIONS		
	Milimeters		
	Min.	Nominal	Max.
A	6.30	6.50	6.70
B	6.70	7.00	7.30
C	3.30	3.50	3.70
D	-	4.60	-
E	-	2.30	-
F	2.95	3.00	3.15
G	0.65	0.70	0.85
H	1.50	1.60	1.70
I	0.50	0.60	0.70
J	-	0.02	0.05
K	0.25	0.30	0.35

LOGIC LEVEL TRIAC

Ratings and Characteristics (Ta 25 °C unless otherwise noted)

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle)

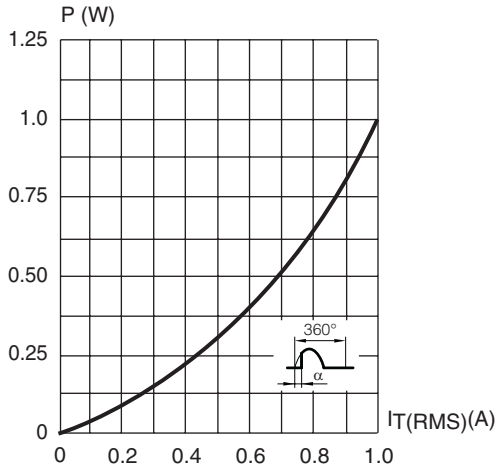


Fig. 2: RMS on-state current versus case temperature (full cycle).

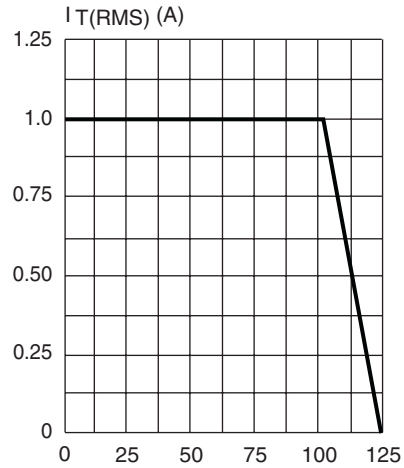


Fig. 3: Relative variation of thermal impedance versus pulse duration.

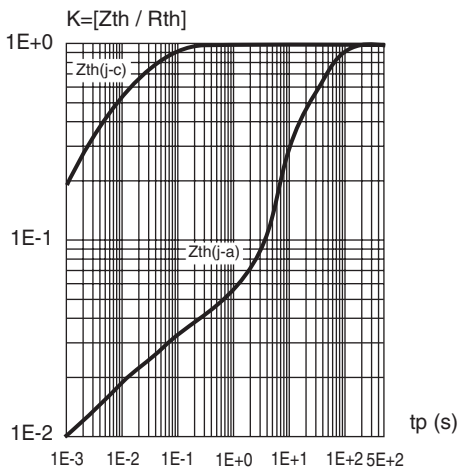


Fig. 4: On-state characteristics (maximum values)

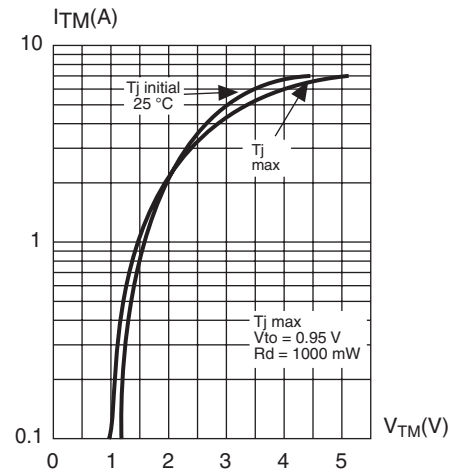


Fig. 5: Surge peak on-state current versus number of cycles

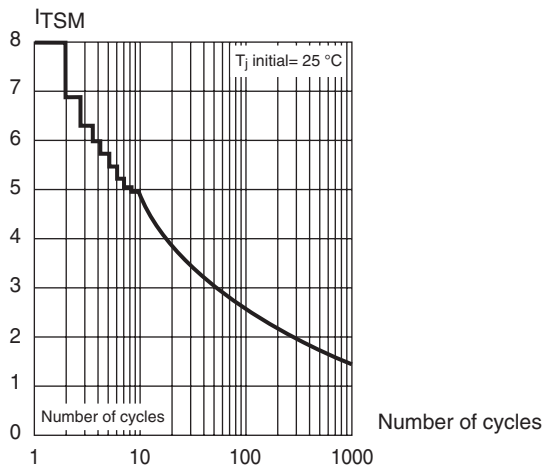
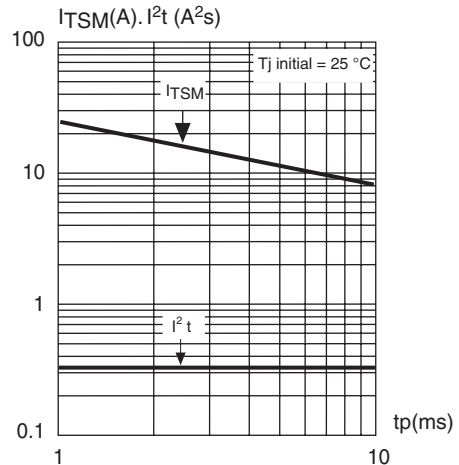


Fig. 6: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp < 10ms, and corresponding value of I²t.



LOGIC LEVEL TRIAC

Ratings and Characteristics (Ta 25 °C unless otherwise noted)

Fig. 7: Relative variation of gate trigger current, holding current and latching versus junction temperature (typical values)

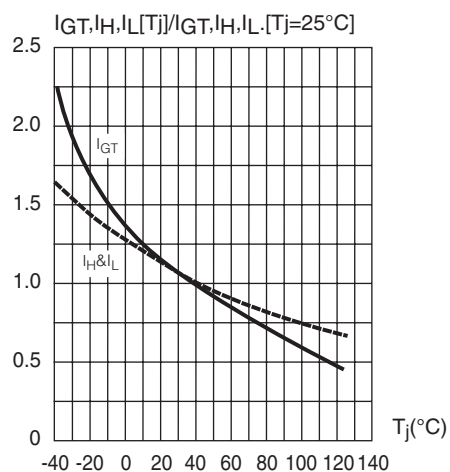


Fig. 8: Relative variation of critical rate of decrease of main current versus junction temperature

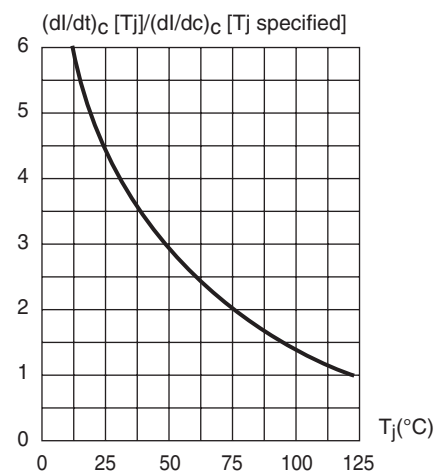
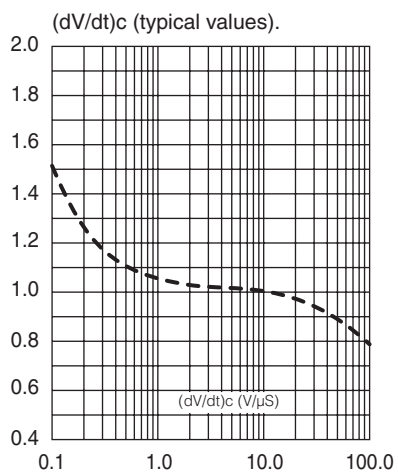


Fig. 9: Relative variation of critical rate of decrease of main current versus



LOGIC LEVEL TRIAC

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