40V, 300mA, Low-I_Q, Adjustable Output Linear Regulator

Features

- Input Voltage Range: 3.5V to 40V
- Quiescent Current: 13μA
- Stable with Low-value Output Ceramic Capacitor (≥ 1μF)
- Rated Output Current: 300mA
- Fixed Output: 3.3V and 5V
- Adjustable Output: 1.25V to 15V
- Output ±2% Accuracy Over Temperature
- Specified Current Limit
- Power Good
- Programmable Power Good Delay
- Thermal Shutdown and Fold-back Short-Circuit Protection
- -40°C to +150°C Specified Junction Temperature Range
- Available in ESOP-8L Package
- Available in AEC-Q100 Grade 1

Applications

- Automotive head unit
- Body Control Module
- Automotive Headlight
- Portable/Battery-Powered Equipment
- DC/AC Inverter and Motor Control

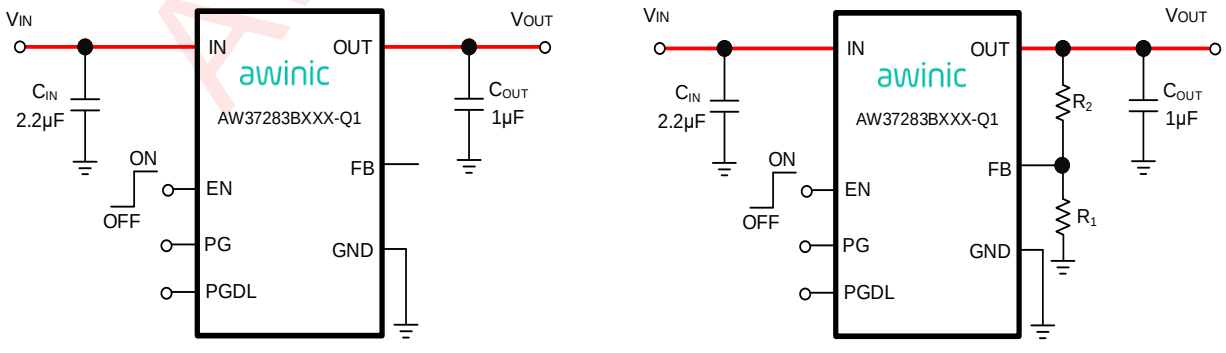
General Description

The AW37283BXXX-Q1 is a low-power linear regulator that supplies power to systems with high-voltage batteries. It includes a wide 3.5V to 40V input range, low-dropout voltage and low-quiescent supply current. The low-quiescent current and low-dropout voltage allow operations at extremely low-power levels. Therefore, the AW37283BXXX-Q1 is ideal for low-power microcontrollers and battery-powered equipment.

The AW37283BXXX-Q1 provides a wide variety of fixed output-voltage options (if requested): 3.3V, 5.0V, Also it provides the output-adjustable option (from 1.25V to 15V).

The regulator output current is limited internally, and the device is protected against short-circuit, over-load, and over-temperature conditions. The AW37283BXXX-Q1 includes thermal shutdown (TSD), current-limiting fault protection, and is available in ESOP-8L package.

Typical Application Circuit



Output Fixed Version　　Output Adjustable Version

Figure 1 Typical Application Circuit

Pin Configuration And Top Mark

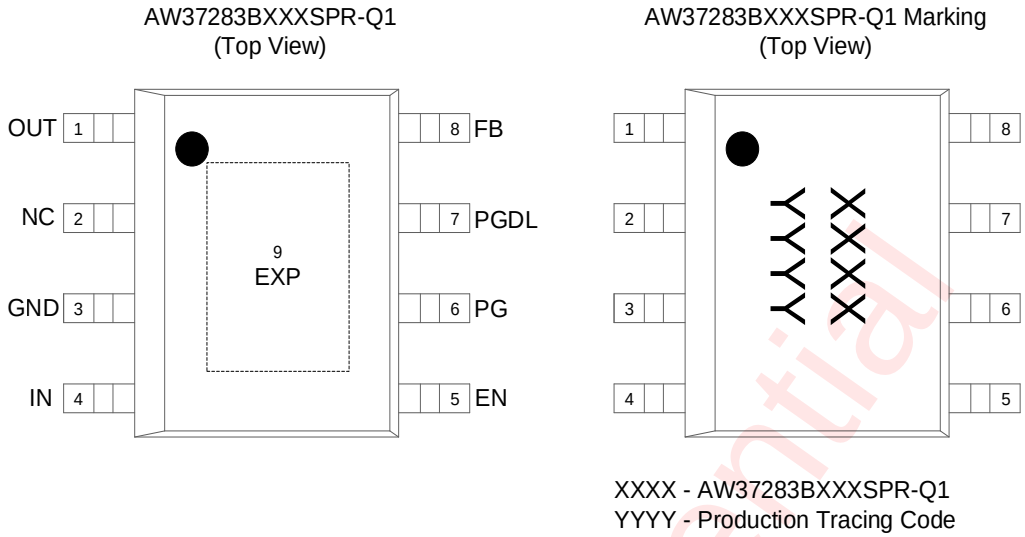
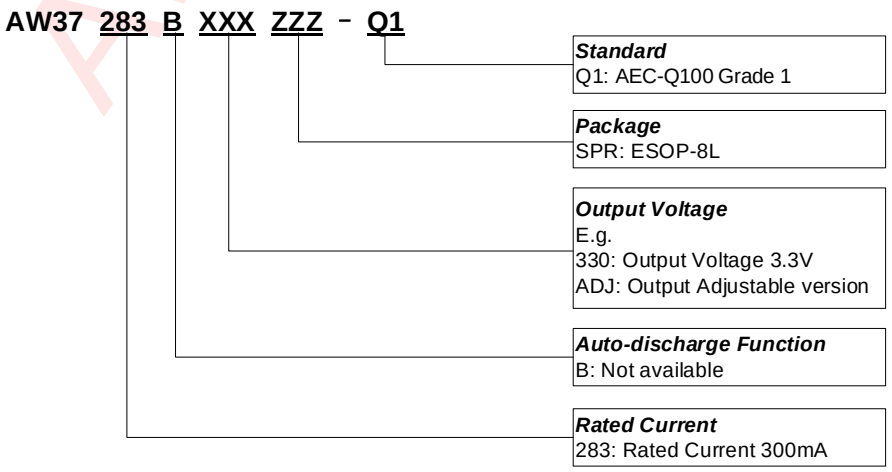


Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	OUT	Regulated output voltage pin. Put a 1 μF or more ceramic capacitor at the output pin.
2	NC	Not connect.
3	GND	Ground.
4	IN	Input supply pin. Put a 2.2 μF or more bypass capacitor at the power supply.
5	EN	Regulator On/Off Control Input. Logic low shuts down the IC, logic high starts up the IC. Connect EN to IN for automatic start-up.
6	PG	Power Good. If not used, pin can be left floating.
7	PGDL	Programmable Power Good Delay Time. If not used, pin can be left floating.
8	FB	Feedback Input for Output Adjustable Version. FB is regulated to 1.25 V nominally. This terminal is used to set the output voltage.
9	EXP	Exposed pad should be tied to ground plane for better power dissipation.

Name Rule



Functional Block Diagram

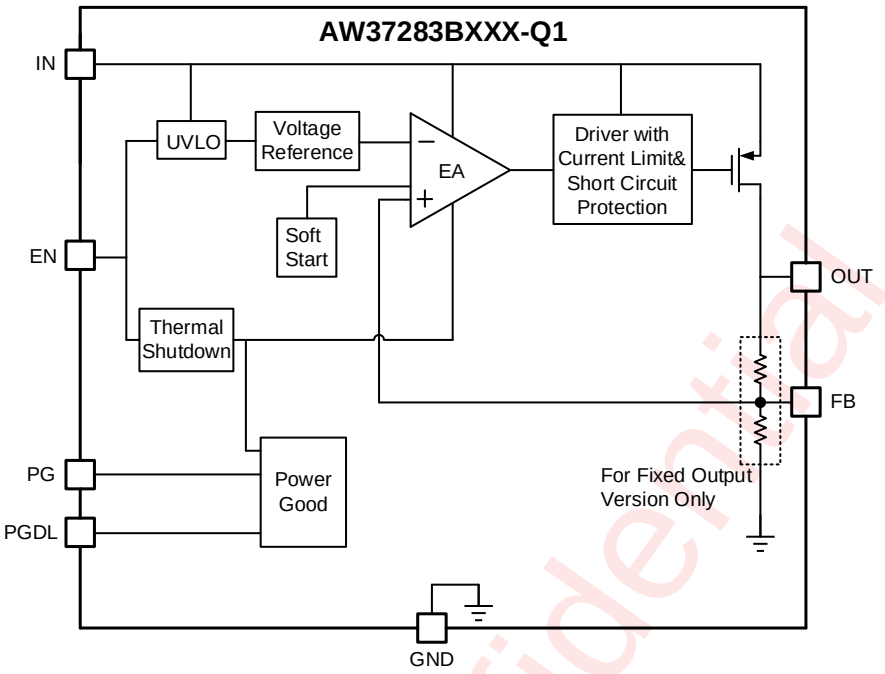


Figure 3 Functional Block Diagram

Typical Application Circuit

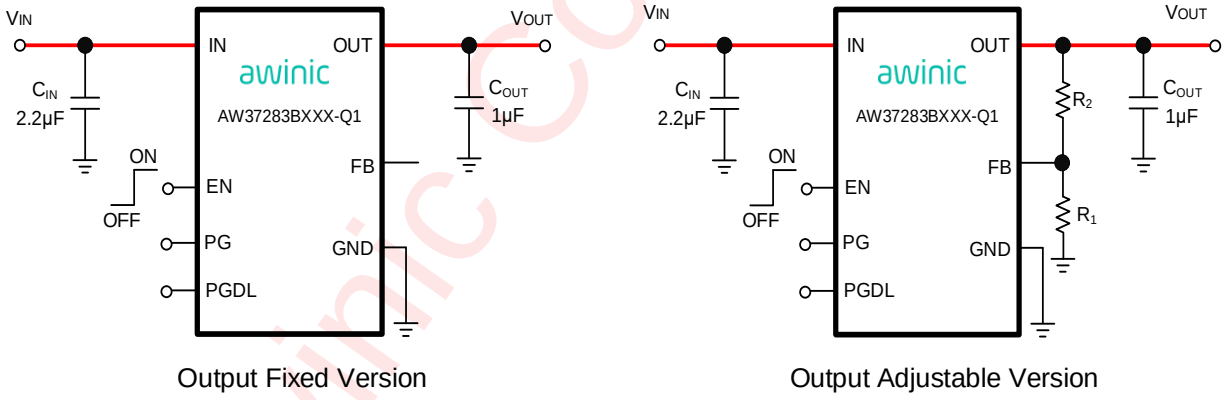


Figure 4 Typical Application Circuit

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW37283B330SPR-Q1	-40°C～125°C	ESOP-8L	DYVT	MSL3	RoHS+HF	2500 units/ Tape and Reel
AW37283B500SPR-Q1	-40°C～125°C	ESOP-8L	4DDR	MSL3	RoHS+HF	2500 units/ Tape and Reel
AW37283BADJSPR-Q1	-40°C～125°C	ESOP-8L	RKH6	MSL3	RoHS+HF	2500 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
IN，EN		-0.3V to + 42V
OUT(Fixed version)		-0.3V to + 6.5V
OUT(Adjustable version)		-0.3V to + 17V
PG		-0.3V to + 15V
PGDL，FB		-0.3V to + 6.5V
Junction-to-ambient thermal resistance θ_{JA}(NOTE 2)		40.38°C /W
Maximum operating junction temperature T_{JMAX}		150°C
Operating free-air temperature range T_A		-40°C to 125°C
Storage temperature T_{STG}		-65°C ~ 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD		
HBM (Human Body Model) (NOTE 3)		±2kV
CDM(Charged Device Model) (NOTE 4)	Corner pins	±750V
	Other pins	±500V

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Thermal resistance from junction to ambient is highly dependent on PCB layout.

NOTE3: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: AEC-Q100-002-RevE.

NOTE4: All pins. Test Condition: AEC-Q100-011-RevD.

Electrical Characteristics

V_{IN} = V_{EN} = 13.5V, T_A = -40°C to + 125°C, T_A ≤ T_J ≤ +150°C, unless otherwise noted. Typical values are at T_A=+25°C.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range		3.5		40	V
V_{OUT}	Output Voltage Range		1.25		15	V
V_{IN_UVLOH}	UVLO Trip Level_H	V_{IN} rising		3	3.3	V
V_{IN_UVLOL}	UVLO Trip Level_L	V_{IN} falling	2.5	2.8		V
I_Q	Quiescent Current	I_{OUT}=0mA		13	25	μA
I_{SD}	Shutdown Current	V_{EN}≤0V			1.5	μA
I_{CL}	Output Current Limit		300			mA
I_{SC}	Short Current Limit			150		mA
V_{FB}	FB Voltage		1.225	1.25	1.275	V
V_{OUT_ACC}	Output Voltage Accuracy		-2		2	%
$V_{dropout}$	Dropout Voltage(1)	I_{OUT}=300mA, $V_{OUT(SET)}$=3.3V		275		mV
		I_{OUT}=300mA, $V_{OUT(SET)}$=5V		260		mV
I_{FB}	FB Input Current	V_{FB}=1.3V			50	nA
$LINE_{Reg}$	Line Regulation	V_{IN} =3.5V to 40V, I_{OUT}=5mA, $V_{OUT(SET)}$=V_{FB}		1	10	mV
		V_{IN} =3.8V to 40V, I_{OUT}=5mA, $V_{OUT(SET)}$=3.3V		1	10	mV
		V_{IN} =5.5V to 40V, I_{OUT}=5mA, $V_{OUT(SET)}$=5V		1	10	mV
$LOAD_{Reg}$	Load Regulation	I_{OUT}=5mA to 300mA, T_A=25°C		1	15	mV
PSRR	Power Supply Ripple Rejection	I_{OUT}=10mA, C_{OUT}=1uF, f=100Hz		65		dB
		I_{OUT}=10mA, C_{OUT}=1uF, f=1kHz		55		dB
		I_{OUT}=10mA, C_{OUT}=1uF, f=10kHz		56		dB
V_{ENH}	EN Input Voltage “H”		1.2			V
V_{ENL}	EN Input Voltage “L”				0.4	V
I_{EN}	EN pulldown Current	V_{EN}=0V or 15V		0.18	0.3	μA
PCT_{PGH}	PG Rising Threshold		88%	92%	96%	V_{FB}
PCT_{HYS_PG}	PG Rising Threshold Hysteresis			5%		V_{FB}

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{OL_PG}	PG Low Voltage	Sink 1mA Current		0.1	0.4	V
I_{LEAK_PG}	PG Leakage Current	V_{PG}=5V			1	μA
I_{CHARGE_PGDL}	PGDL Charging Current	V_{PGDL}=1V	7	10	13	μA
V_{H_PGDL}	PGDL Rising Threshold		1.4	1.7	2	V
V_{L_PGDL}	PGDL Falling Threshold		0.2	0.4	0.7	V
T_{DLY_PG}	PG Delay Time	C_{PGDL}=47nF	5	10	15	ms
T_{REAC_PG}	PG Reaction Time	C_{PGDL}=47nF		5		μs
T_{SDH}	Thermal Shutdown Threshold	Temperature Rising	150	165		°C
T_{SDL}	Thermal Shutdown Reset Threshold	Temperature Falling		135		°C

(1) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 98% of its nominal value.

Typical Characteristics

V_{IN} = V_{EN} = 13.5V, T_A = -40°C to +125°C, $T_A \le T_J \le$ +150°C, unless otherwise noted. Typical values are at T_A=+25°C.

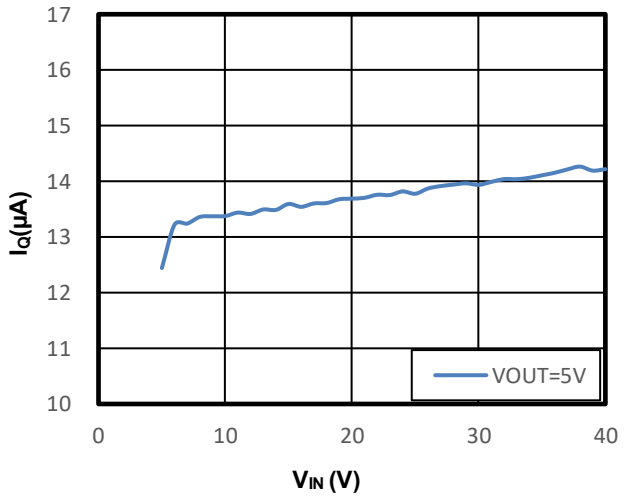


Figure 5 Quiescent Current vs. V_{IN}, No load

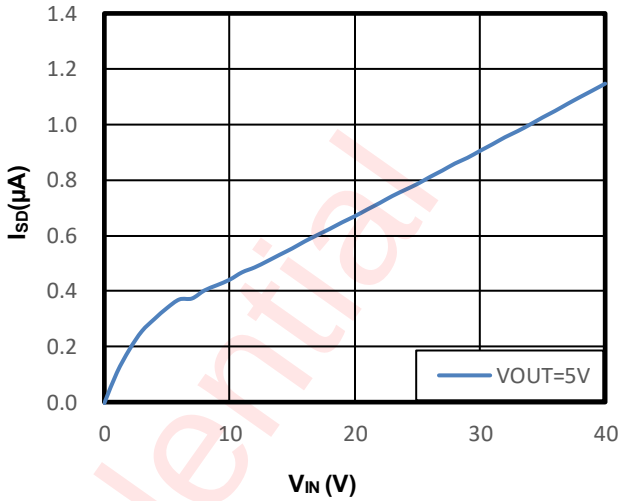


Figure 6 IN Shutdown Current vs. V_{IN}

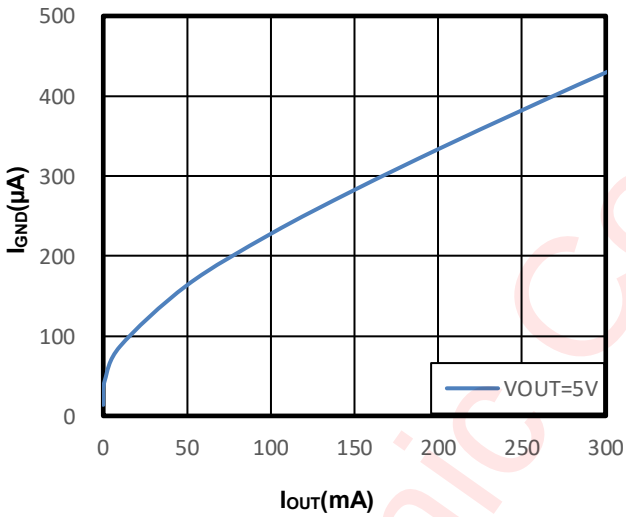


Figure 7 GND Current vs. I_{OUT}

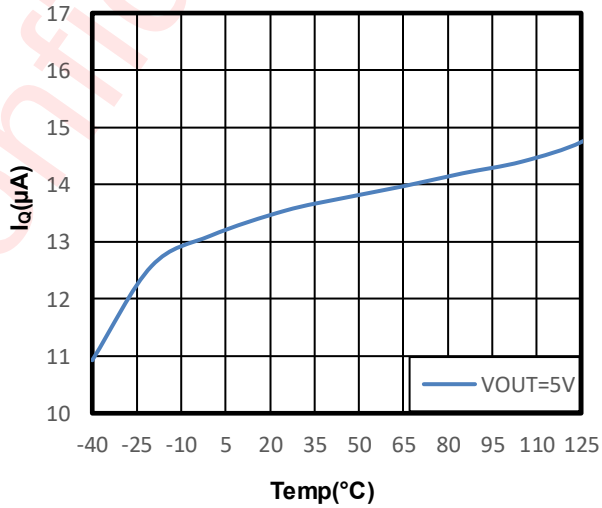


Figure 8 Quiescent Current vs. Temp

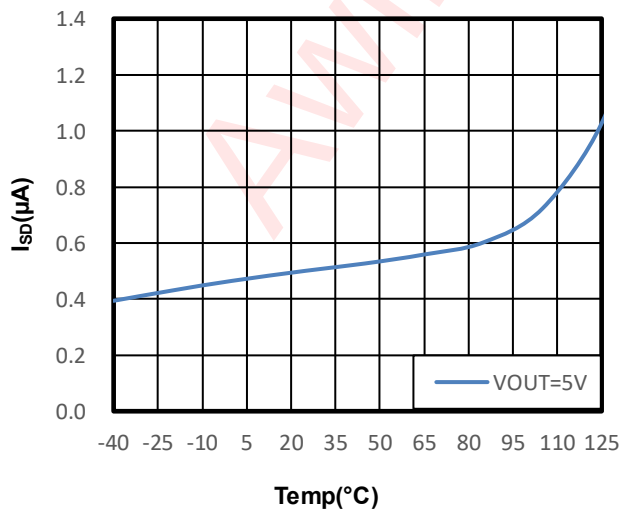


Figure 9 IN Shutdown Current vs. Temp

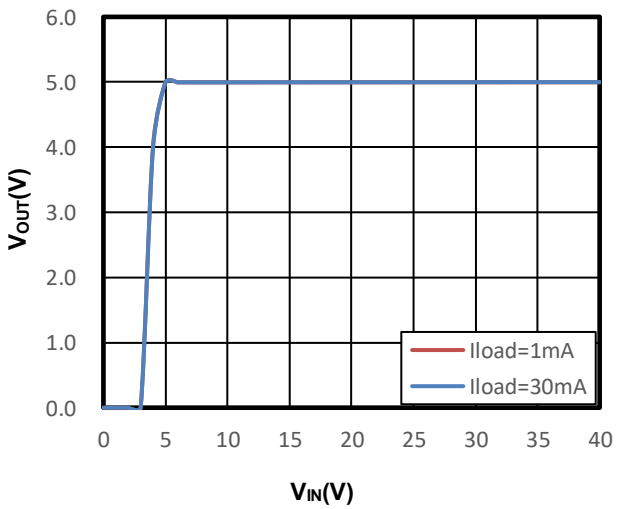


Figure 10 V_{OUT} vs. V_{IN}

Typical Characteristics (continued)

V_{IN} = V_{EN} = 13.5V, T_A = -40°C to + 125°C, T_A ≤ T_J ≤ +150°C, unless otherwise noted. Typical values are at T_A=+25°C.

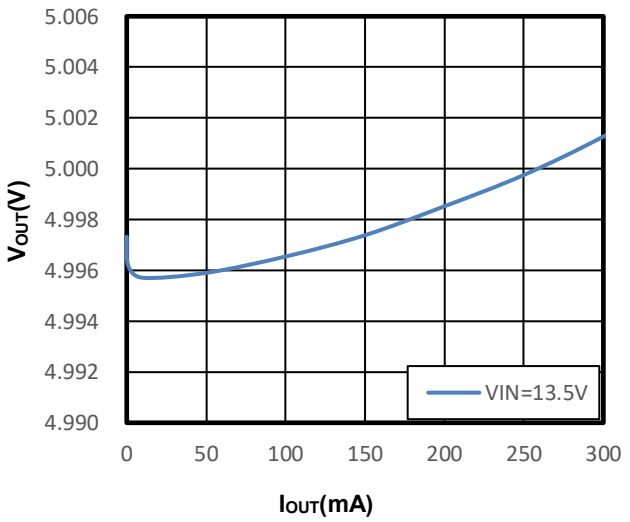


Figure 11 V_{OUT} vs. I_{OUT}

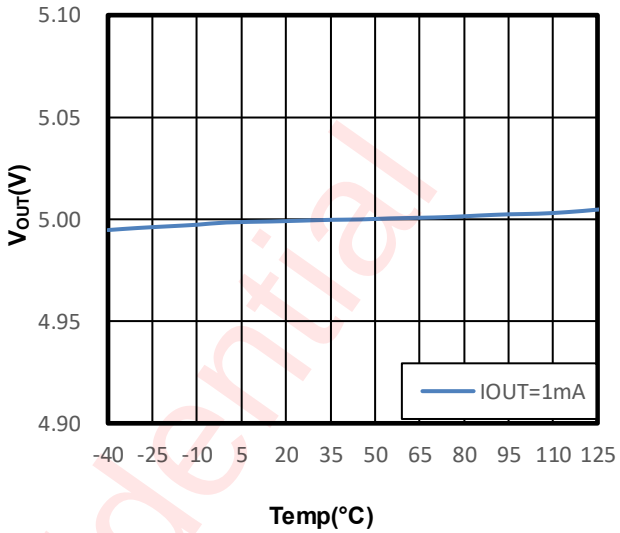


Figure 12 V_{OUT} vs. Temp

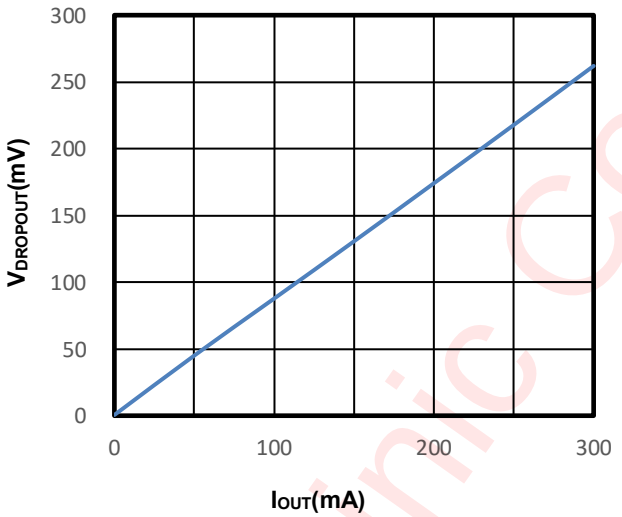


Figure 13 $V_{DROPOUT}$ vs. I_{OUT}

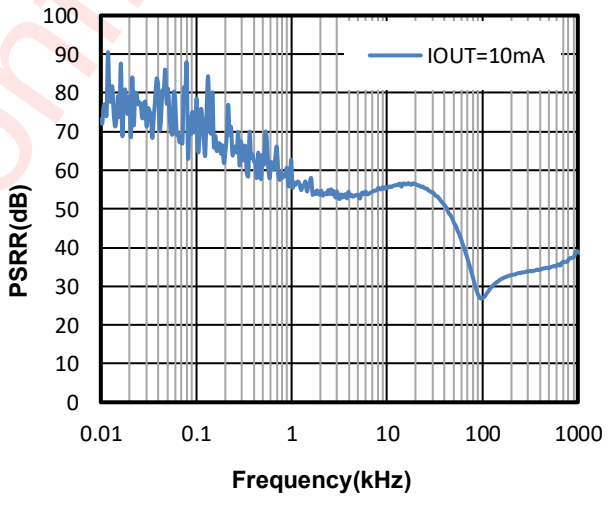
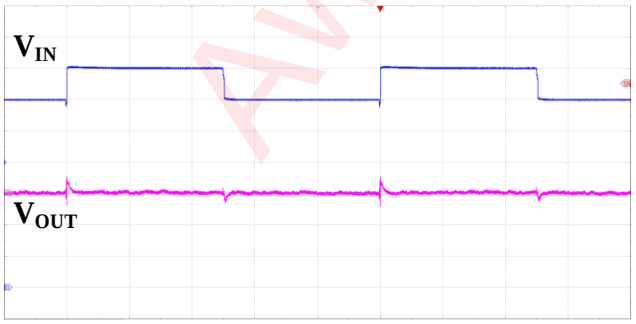


Figure 14 PSRR vs. Frequency

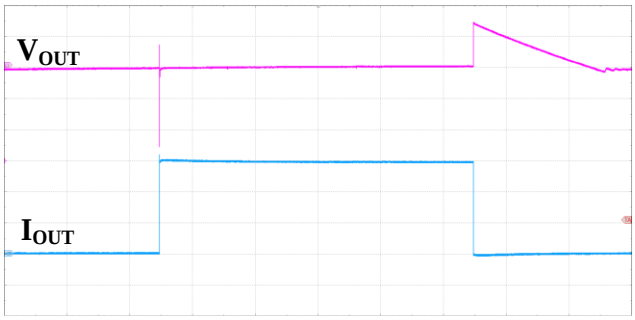


C1: 1.00V/div C2: 20mV/div t=2ms/div

V_{IN}=6V to 7V，C_{OUT}=1μF，I_{OUT}=300mA，tr=tf=10μs

V_{OUT}=5V

Figure 15 Line Transient



C2: 400mV/div C3: 100mA/div t=2ms/div

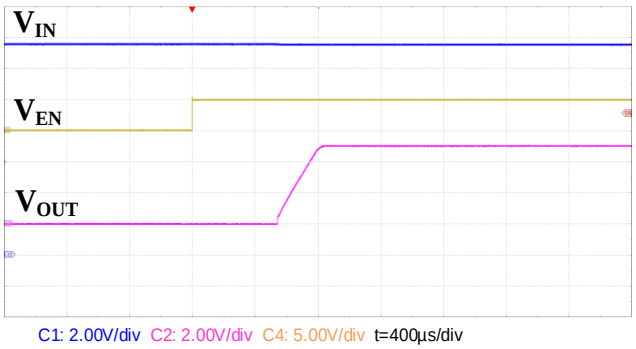
V_{IN}=13.5V，C_{OUT}=1μF，I_{OUT}=1mA to 300mA，tr=tf=1μs

V_{OUT}=5V

Figure 16 Load Transient

Typical Characteristics (continued)

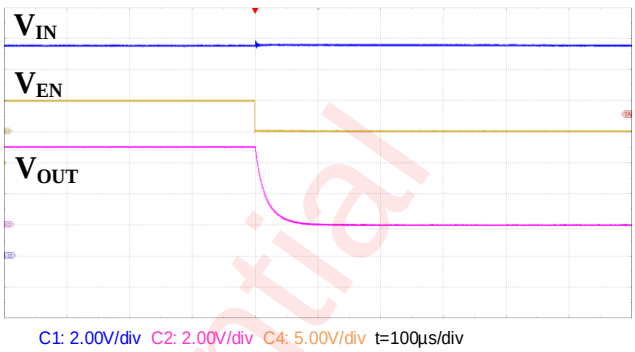
V_{IN} = V_{EN} = 13.5V, T_A = -40°C to + 125°C, T_A ≤ T_J ≤ +150°C, unless otherwise noted. Typical values are at T_A=+25°C.



V_{IN}=13.5V，C_{OUT}=1μF，I_{OUT}=300mA

V_{OUT}=5V

Figure 17 Turn on with EN



V_{IN}=13.5V，C_{OUT}=1μF，I_{OUT}=300mA

V_{OUT}=5V

Figure 18 Turn off with EN

Detailed Functional Description

The AW37283BXXX-Q1 is a linear regulator . After powered on, with EN pin assertion, feedback voltage signal from the integrated resistor network and a voltage related to the voltage reference are transmit to positive input terminal and negative input terminal of an error amplifier (EA) respectively. The output signal of EA is used to control the open-state of power MOSFET. After soft-start, feedback voltage signal compares with the established reference voltage, making output voltage stable and accurate. AW37283BXXX-Q1 integrates function of Power Good.

Enable Operation

AW37283BXXX-Q1 uses EN pin to realize enable operation. Applying proper value of voltage to EN pin can make IC enable/disable.

If the voltage of EN pin is less than 0.4V, AW37283BXXX-Q1 is guaranteed to be disabled. In this state, function modules of IC and power MOSFET are turned off. In disable state, AW37283BXXX-Q1 only consumes a typical 100nA current.

If the voltage of EN pin is more than 1.2V, AW37283BXXX-Q1 is guaranteed to be enabled. In this state, AW37283BXXX-Q1 regulates output voltage to the designed value of voltage.

A 180nA pull down current to Ground is built-in at EN pin, making sure that the IC is disabled when EN pin floats. If Enable function is not required, EN pin should be connected directly to IN pin.

Setting V_{OUT} of Adjustable Version

Set the output voltage of the AW37283BXXX-Q1 by using a resistor divider(See Typical Application Circuit).

Choose R_1=1MΩ to maintain a 1.25μA minimum load. Calculate the value for R_2 using the following equation:

$$R_2 = R_1 \times \left(\frac{V_{OUT}}{1.25V} - 1\right)$$

Undervoltage Shutdown

AW37283BXXX-Q1 has an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage (V_{IN}) falls below an internal UVLO threshold (V_{IN_UVLOL}). This threshold limit ensures that the regulator does not latch into an unknown state during low-input-voltage conditions. If the input voltage has a negative transient that drops below V_{IN_UVLOL} and recovers, the regulator shuts down and powers up with a normal power-up sequence when the input voltage is above V_{IN_UVLOH}.

Power Good Function

The AW37283BXXX-Q1 has one power good (PG) pin. The PG pin is the open drain of an internal MOSFET. It should be connected to V_{OUT} or external voltage source(<15V) through a resistor. After the V_{FB} reaches 92% of nominal value, the MOSFET turns off and PG pin is pulled to high by V_{OUT} or external voltage source. When the V_{FB} drops to 88% of nominal value, the PG voltage is pulled to GND.

There is a delay time when PG asserts high. The delay time can be programmed by adding a capacitor on PGDL. To select a capacitor for PGDL, use below equation:

$$C_{PGDL} = \frac{T_{DLY\_PG} \times I_{CHARGE\_PGDL}}{V_{H\_PGDL}}$$

Where T_{DLY_PG} is the desired delay time for PG asserts high, I_{CHARGE_PGDL} is the PGDL charging current and V_{H_PGDL} is 1.7V.

Figure 18 shows the power good timing.

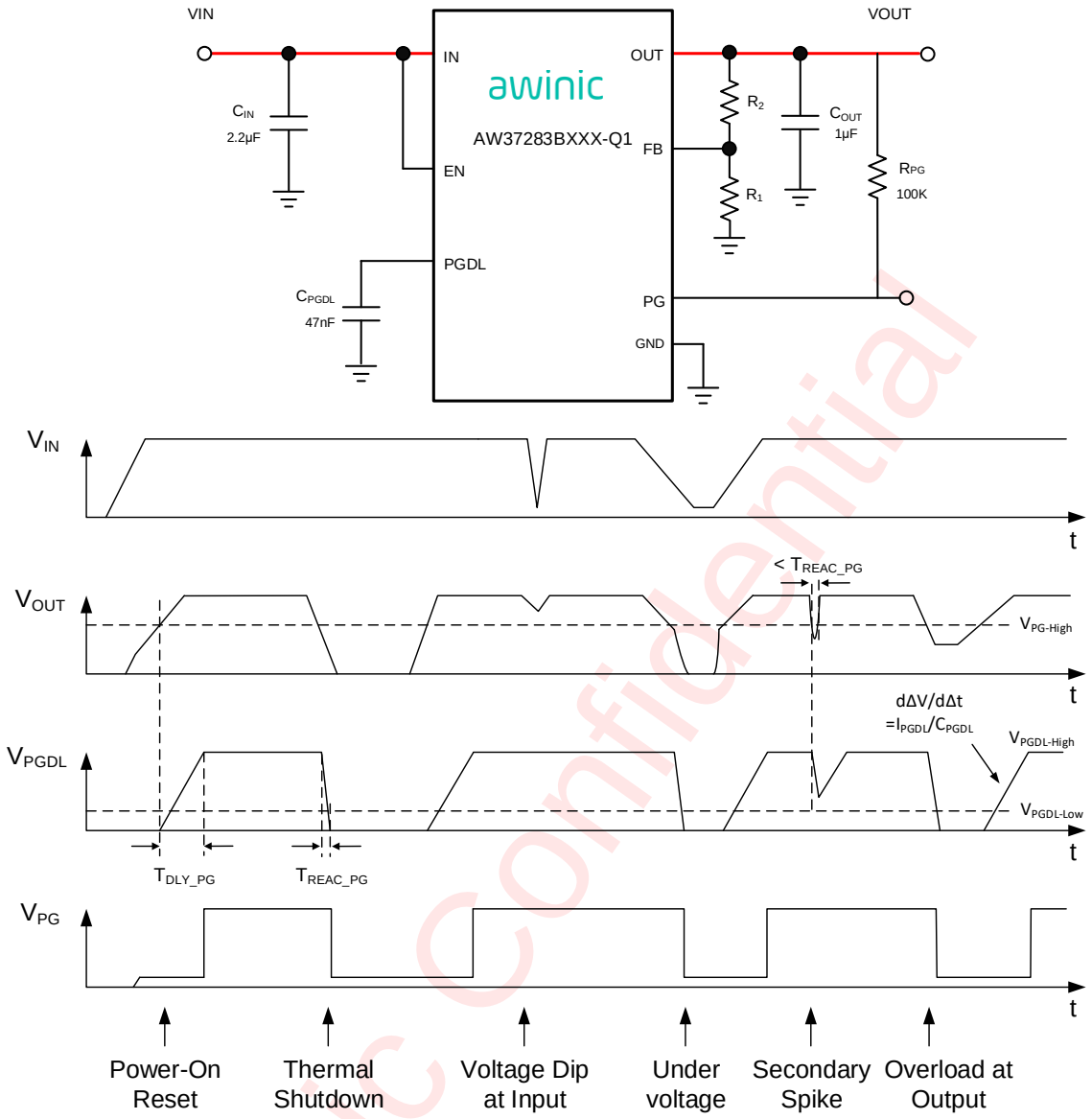


Figure 19 Power Good Timing

Output Current Limit

AW37283BXXX-Q1 integrates output current limit function, protecting IC from excessive current.

When the load is excessively heavy, AW37283BXXX-Q1 limits the current flowing through the IC to a typical 600Ma current. This value is specially designed, so that IC is protected properly and the output capability of 300Ma is not influenced either.

Meanwhile, AW37283BXXX-Q1 integrates a 130Ma fold-back current limit function, lowering the system dissipation when output overload or short to Ground.

Thermal Shutdown

AW37283BXXX-Q1 integrates thermal shutdown function, protect IC from excessively high temperature.

When the chip temperature exceeds 165°C, AW37283BXXX-Q1 detects it as an over-temperature event, triggering thermal shutdown, which will turn off the main function module, including power MOSFET. This inhibits increase of chip's temperature. IC would keep the protection-state on until the chip's temperature falls below to 135°C. At this moment, the over-temperature protection-state is released, IC resumes to work again.The hysteresis avoids IC's turning off and on frequently around the the Thermal Shutdown threshold.

Application Information

Power Dissipation and Device Operation

The permissible power dissipation is dependent on the ambient temperature T_A and the junction-to-ambient thermal resistance θ_{JA}.

The absolute maximum allowable power dissipation for the device in a given package can be calculated using Equation below, where T_{J_MAX} = 150°C :

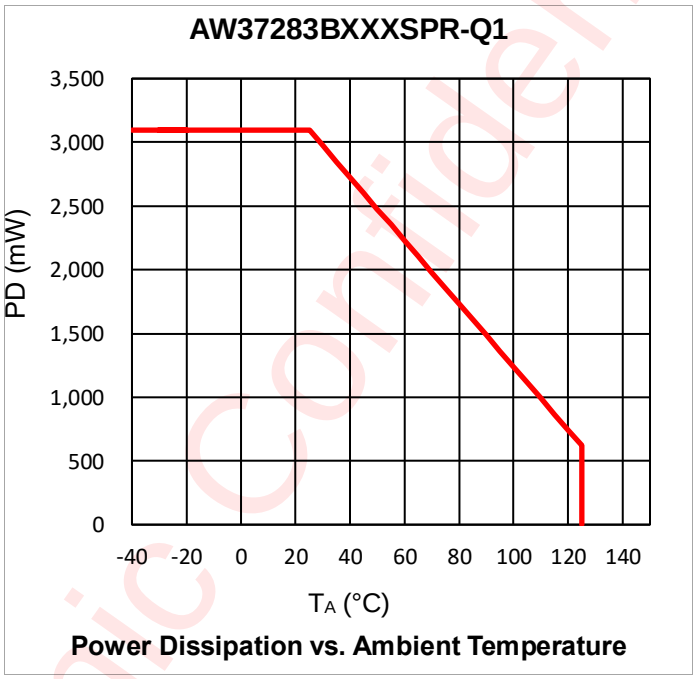
$$PD_{MAX} = (T_{J\_MAX} - T_A) / \theta_{JA}$$

The actual power being dissipated in the device can be represented by Equation below:

$$PD_{ACT} = (V_{IN} - V_{OUT}) \times I_{OUT}$$

These equations above establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device.

The graphs of Power Dissipation vs. Ambient Temperature are showed below :



Power Dissipation vs. Ambient Temperature

The above graph shows the maximum power dissipation for this package at T_{J_MAX} = 150°C. Operating the device above the region PD_{MAX} might have a negative influence on its lifetime.

Capacitors Selection

IN pin: Input Capacitor C_{IN}

AW37283BXXX-Q1 advises to use a 2.2μF or more X5R or X7R ceramic capacitor at IN pin as shown in Typical Application Circuit. Larger values can improve line transient response. The rated voltage of C_{IN} should be higher than V_{IN} voltage.

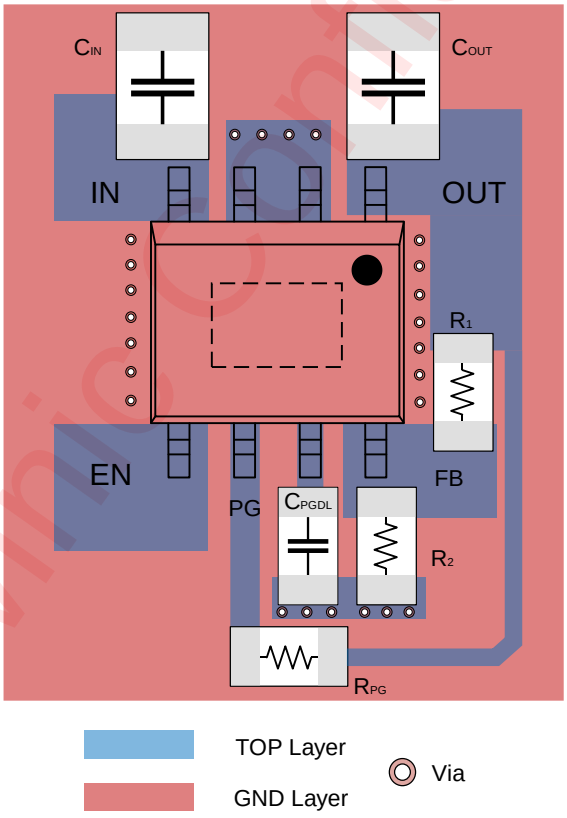
OUT pin: Output Capacitor C_{OUT}

AW37283BXXX-Q1 advises to use a 1μF or more X5R or X7R ceramic capacitor at OUT pin as shown in Typical Application Circuit. Larger values can improve load transient response and reduce noise. The rated voltage of C_{OUT} should be higher than V_{OUT} voltage.

PCB Layout Consideration

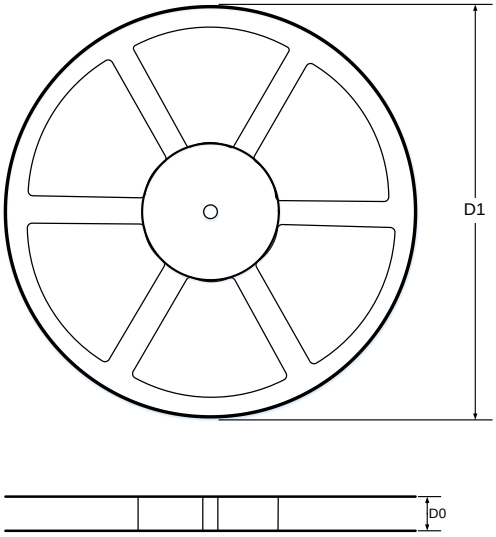
The performance of a power source circuit using this device is highly dependent on a peripheral circuit. To obtain the optimal performance, a peripheral component or the device mounted on PCB should not exceed its rated voltage, rated current or rated power. When designing a peripheral circuit, guidelines below for PCB layout of AW37283BXXX-Q1 should be obeyed:

1. All peripheral components should be placed as close to the chip as possible. C_{IN} and C_{OUT} should be close to IN and OUT pins respectively. Avoid connecting device and chip pins with two different layers of copper, use the same layer of copper instead.
2. IN and OUT pin are the large current input and output of the chip, make IN, OUT, and meanwhile GND lines sufficient.
3. Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4. The connection lines between the planes of C_{IN} or C_{OUT} and respective chip pin should be as short and wide as possible, to reduce noise and EMI interference, or it may cause noise pickup or unstable operation.
5. The exposed plane of chip and GND pins must be connected to the large-area ground layer of PCB directly, meanwhile place sufficient vias below the exposed plane. Thus we can decrease the thermal resistor on the board to optimize heat-diffusion performance.

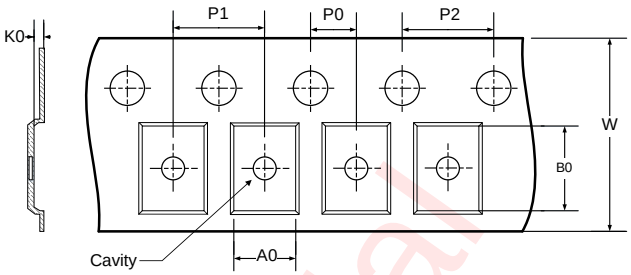


Tape And Reel Information

REEL DIMENSIONS

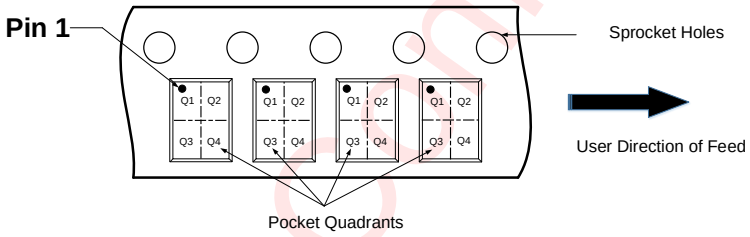


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



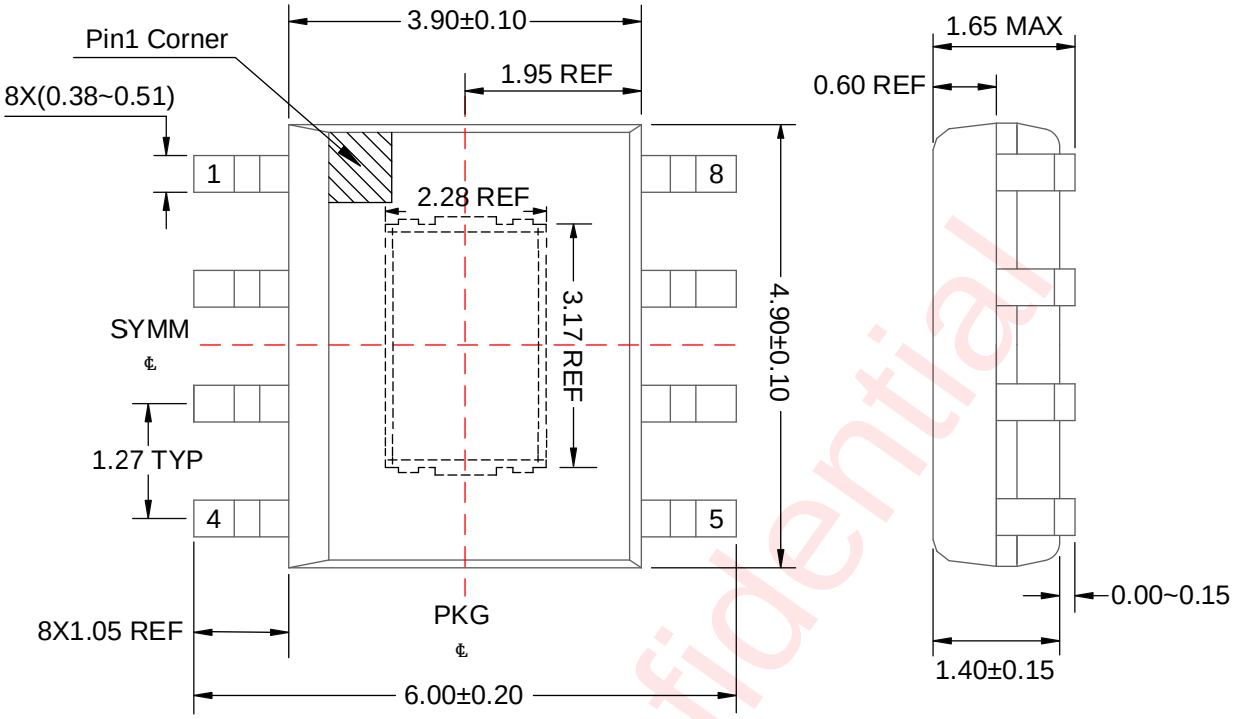
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

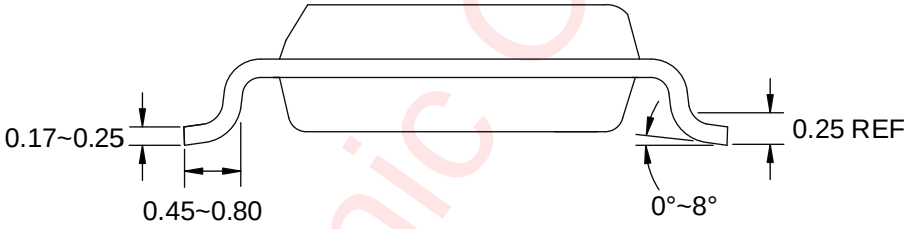
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	6.5	5.3	2.2	2	8	4	12	Q1

All dimensions are nominal

Package Description



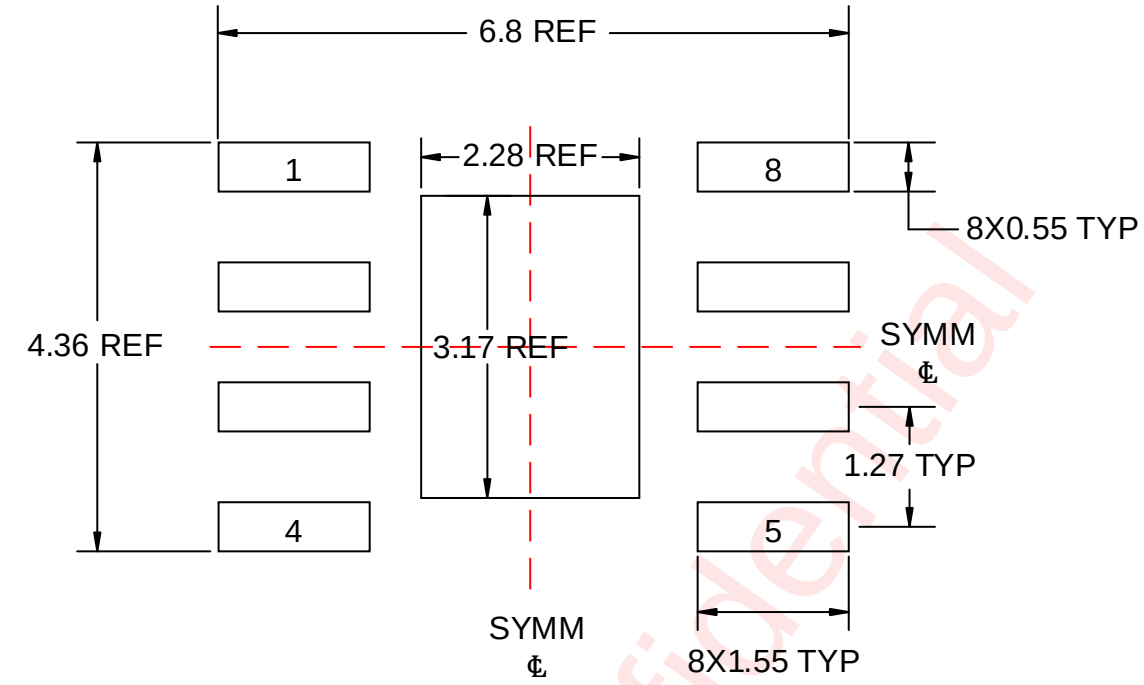
Top View **Side View**



Side View

Unit: mm

Land Pattern Data



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit：mm

Revision History

Version	Date	Change Record
V1.0	Oct. 2024	Officially released
V1.1	Nov. 2024	Update “V” to “mA” in Figure 11,13(P8)
V1.2	Feb. 2025	Update Absolute Maximum Ratings(P4)
V1.3	Sep. 2025	Update Electrical Characteristics(P5)

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