钍地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65LBC182/SN75LBC182

Differential bus transceiver

网址 www.sztdbdt.com

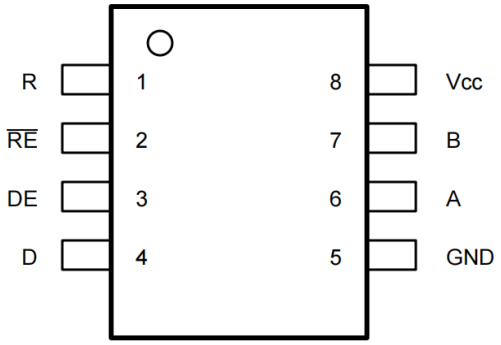
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

●Quarter-unit load allows up to 128 devices on a single bus
●Meets or exceeds the requirements of ANSI standards T/EIA-485-A and ISO 8482: 1987(E)
● Controlled driver output voltage slew rate allows longer cable lengths
● Specifically designed for signal transmission rates.
– The signal transmission rate of the line is the number of voltage transitions per second, expressed in bps (bits per second), up 250kbps
● Low disabled supply current: 250μA (maximum)
● Thermal shutdown protection
●Open-circuit fail-safe receiver
● Receiver input hysteresis: 70mV (typical)
●Interference-free power-up and power-down protection



PDIP or SOIC Package
(Top View)

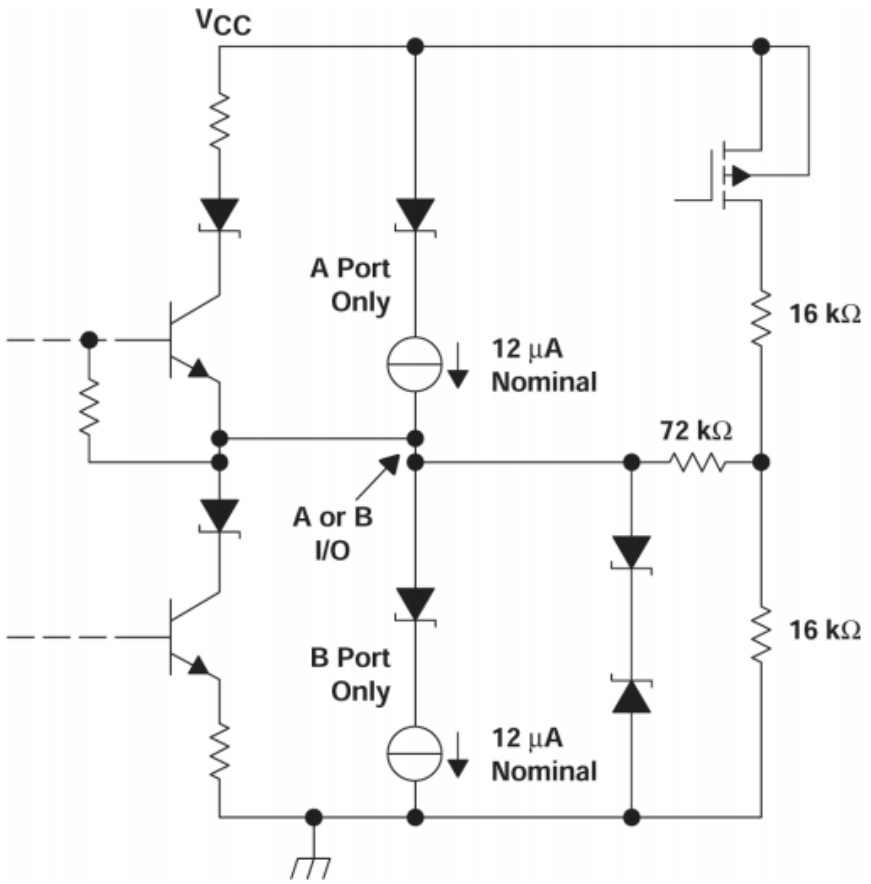
Applications

● Utility metering
● Industrial process control
● Building automation

Description

SN65LBC182 and SN75LBC182 are differential data line transceivers that provide high- ESD protection and use the industry-standard SN75176 package. These devices are designed for balanced transmission lines and comply with ANSI standards TIA/EIA-48-A and ISO 8482. SN65LBC182 and SN75LBC182 integrate a three-state differential line driver and a input line receiver, both of which are powered by a single 5V supply. The driver and receiver have active-high and active-low enable pins, respectively, which can externally connected to function as direction control.

The driver outputs and receiver inputs are internally connected to form a differential input/ output (I/O) bus port, which provides a minimum for the bus and can operate over a wide common-mode voltage range, making the device ideal for use in combined-line applications. The device also includes additional functionality for the combinedline data bus, suitable for applications in electrically noisy environments, such as industrial process control or power inverters.The SN75LBC182 and SN65LBC18 bus pins also feature a high input resistance equivalent to a quarter-unit load, allowing up to 128 similar devices to be connected to the bus. High ESD tolerance protects the devices cable connections. (For higher levels of protection, refer to SN65/75LBC184, document number SLLS236.)
The differential design includes slew-rate-controlled outputs, sufficient to transmit data at rates up to 250 kbps. Compared to uncontrolled voltage transitions, slew-rate control allows for unterminated cables and longer stubs to be deployed from the trunk. The receiver design provides a high-level fail-safe output when the input is left floating (open circuit).-low device standby current can be achieved by disabling the driver and receiver.
The rated operating temperature range for the SN65LBC182 is -40 ° C to85 ° C, and the rated operating temperature range for the SN75LBC182 is 0 ° C to 70 ° C



输入和输出原理图

表 **4-1. Pin Functions**

PIN		TYPE	DESCRIPTION
NAME	NO.		
R	1	O	Receiver Output
$\overline{RE}$	2	I	Active Low Receiver Enable Input
DE	3	I	Active High Driver Enable Input
D	4	I	Driver Input
GND	5	GND	Device GND
A	6	I/O	Non-Inverting Differential Bus I/O
B	7	I/O	Inverting Differential Bus I/O
V_{CC}	8	PWR	Device VCC (4.75V to 5.25V)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free−air temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range, (see (2))	−0.5	7	V
(A or B)	Voltage range at any bus terminal	−15	15	V
V_I (D, DE, R or $\overline{RE}$)	Input voltage	−0.3	7	V
I_O	Receiver output current		±20	mA
	Continuous total power dissipation		See *Dissipation Rating* table	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	A, B, GND	±15	kV
		All pins	±3	
	IEC 61000-4-2 contact discharge	A, B, GND	±8	kV
	IEC 61000-4-2 Air-gap discharge	A, B, GND	±15	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Dissipation Rating

PACKAGE(2)	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1150 mW	9.2 mW/°C	736 mW	598 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature

5.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus I/O terminal (separately or common mode) V_I or V_{IC}		−7		12	V
High-level input voltage, V_{IH}	D, DE, $\overline{RE}$	2			V
Low-level input voltage, V_{IL}				0.8	
Differential input voltage, V_{ID} (see (1))		−12		12	V
Output current, I_O	Driver	−60		60	mA
	Receiver	−8		4	
Operating free-air temperature, T_A	SN65LBC182	−40		85	°C
	SN75LBC182	0		70	

(1) Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

5.5 Thermal Information

THERMAL METRIC(1)		D (SOIC)	P (PDIP)	UNIT
		8-PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	84.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	65.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	62.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	31.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	60.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.6 Driver Electrical Characteristics

over recommended operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA		−1.5			V
V_O	Output voltage		I_O = 0		0		V_{CC}	V
$\|V_{OD}\|$	Differential output voltage		R_L = 54 Ω,	See 图 6-1	1.5	2.2	V_{CC}	V
			V_{test} = −7 V to 12 V,	See 图 6-2	1.5	2.2	V_{CC}	V
ΔV_{OD}	Change in magnitude of differential output voltage		See 图 6-1		−0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage				1		3	
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		See 图 6-1 and 图 6-4		−0.2		0.2	
$V_{OC(PP)}$	Peak-to-peak change in common-mode output voltage during state transitions					0.8		V
I_{OZ}	High-impedance output current		See receiver input currents					
I_{IH}	High-level input current (D, DE)		V_I = 2.4 V				50	μA
I_{IL}	Low-level input current (D, DE)		V_I = 0.4 V		−50			μA
I_{OS}	Short-circuit output current		V_O = −7 V to 12 V		−250		250	mA
I_{CC}	Supply current	SN75LBC182	No load, DE at V_{CC},	$\overline{RE}$ at V CC		12	25	mA
		SN65LBC182				12	30	

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.

5.7 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage					0.2	V
V_{IT-}	Negative-going input threshold voltage			−0.2			
V_{hys}	Hysteresis voltage (V_{IT+} − V_{IT-})				70		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA		−1.5			V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_O = −8 mA,	See 图 6-7	2.8			V

5.7 Receiver Electrical Characteristics（续）

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{OL}	Low-level output voltage	V_{ID} = 200 mV, I_O = 4 mA,	See 图 6-7			0.4	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 to 2.4 V				±1	μA
I_I	Bus input current	V_{IH} = 12 V, V_{CC} = 5 V	Other input at 0 V			250	μA
		V_{IH} = 12 V, V_{CC} = 0 V				250	
		V_{IH} = −7 V, V_{CC} = 5 V		−200			
		V_{IH} = −7 V, V_{CC} = 0 V		−200			
I_{IH}	High-level input current ($\overline{RE}$)	V_{IH} = 2 V				50	μA
I_{IL}	Low-level input current ($\overline{RE}$)	V_{IL} = 0.8 V		−50			μA
I_{CC}	Supply current	No load	DE at 0 V, $\overline{RE}$ at 0 V			3.5	mA
			DE at 0 V, $\overline{RE}$ at V_{CC}		175	250	μA

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.

5.8 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

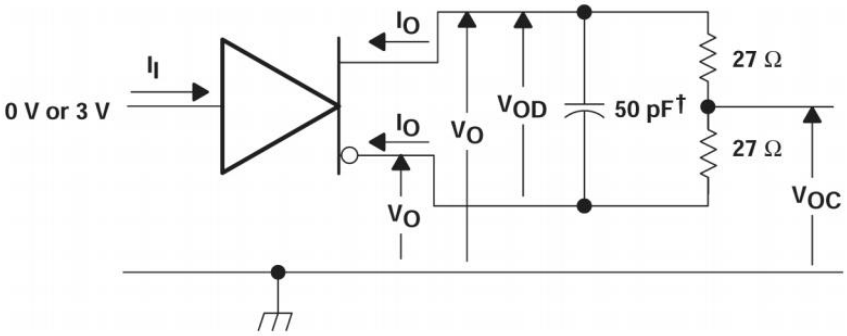
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r	Differential output signal rise time	R_L = 54 Ω, See 图 6-3	C_L = 50 pF,	0.25	0.72	1.2	μs
t_f	Differential output signal fall time			0.25	0.73	1.2	
t_{PLH}	Propagation delay time, low-to-high-level output					1.3	
t_{PHL}	Propagation delay time, high-to-low-level output					1.3	
$t_{sk(p)}$	Pulse skew (t_{PHL} − t_{PLH})				0.075	0.15	
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See 图 6-5			3.5	μs
t_{PHZ}	Output disable time from high level					3.5	
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See 图 6-6			3.5	μs
t_{PLZ}	Output disable time from low level					3.5	

5.9 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r	Differential output signal rise time	C_L = 50 pF,	See 图 6-7		20		ns
t_f	Differential output signal fall time				20		
t_{PLH}	Propagation delay time, low-to-high-level output					150	
t_{PHL}	Propagation delay time, high-to-low-level output					150	
t_{PZH}	Output enable time to high level	See 图 6-8				100	ns
t_{PZL}	Output enable time to low level					100	
t_{PHZ}	Output disable time from high level					100	ns
t_{PLZ}	Output disable time from low level					100	
$t_{sk(p)}$	Pulse skew |t_{PHL} − t_{PLH}|					50	ns

6 Parameter Measurement Information



A. Includes probe and jig capacitance

图 6-1. Driver Test Circuit, v_{OD} And v_{OC} Without Common-Mode Loading

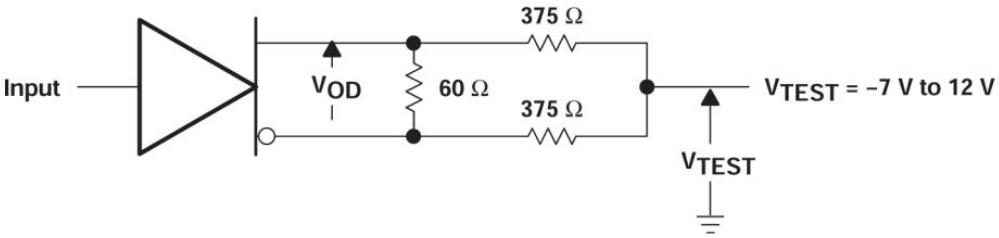
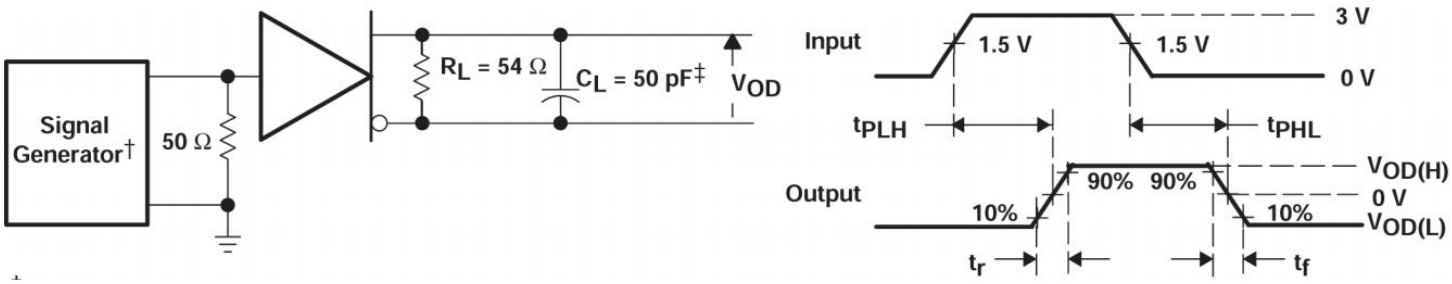


图 6-2. Driver Test Circuit, v_{OD} With Common-Mode Loading



A. PRR = 1 MHz, 50% duty cycle, t_r < 6 ns, t_f < 6 ns, Z_o = 50 Ω
B. Includes probe and jig capacitance

图 6-3. Driver Switching Test Circuit and Waveforms

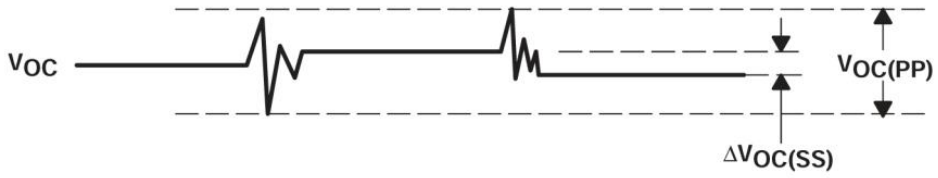
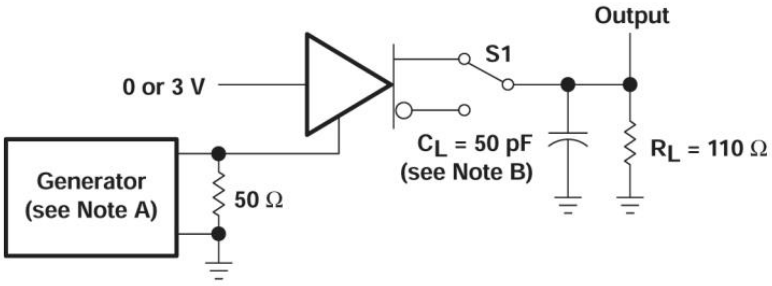
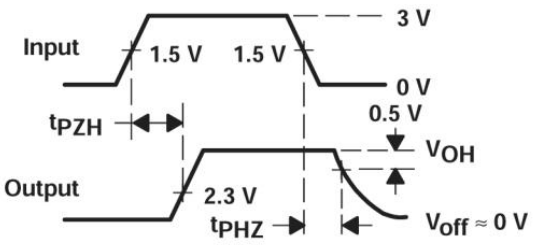


图 6-4. V_{OC} Definitions



TEST CIRCUIT

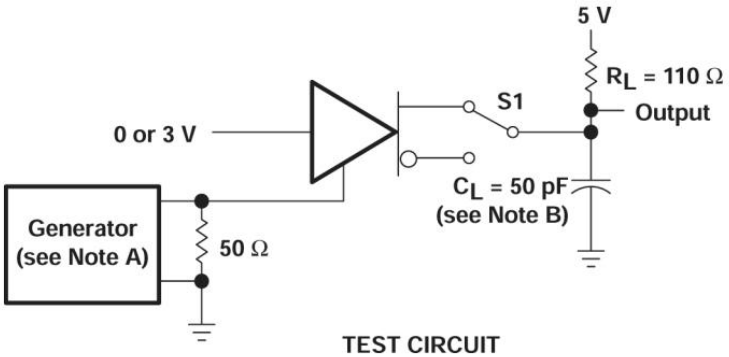


VOLTAGE WAVEFORMS

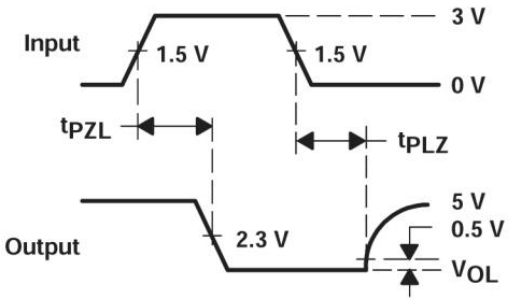
A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, $t_r \leqslant 10$ ns, $t_f \leqslant 10$ ns, $Z_O = 50\ \Omega$.

B. C_L includes probe and jig capacitance.

图 6-5. Driver T_{PZH} And T_{PHZ} Test Circuit and Voltage Waveforms



TEST CIRCUIT

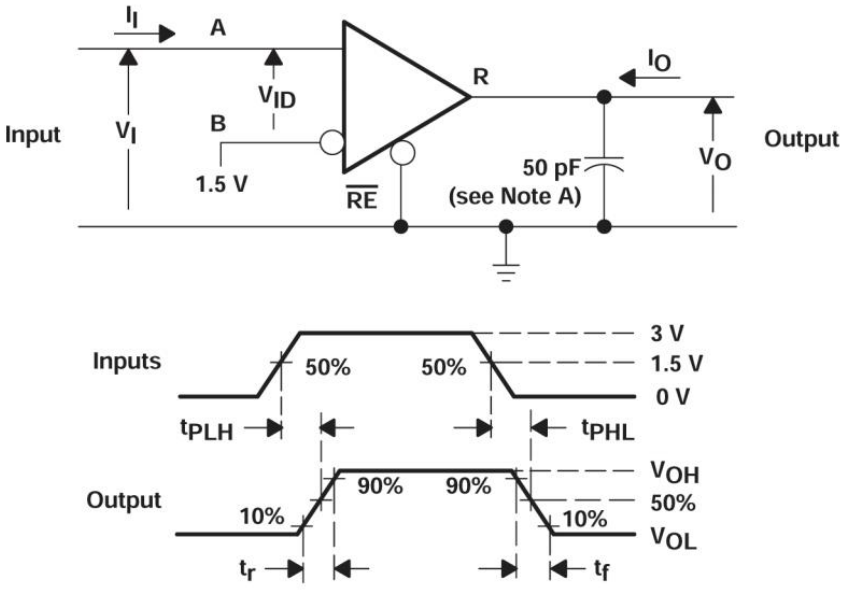


VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, $t_r \leqslant 10$ ns, $t_f \leqslant 10$ ns, $Z_O = 50\ \Omega$.

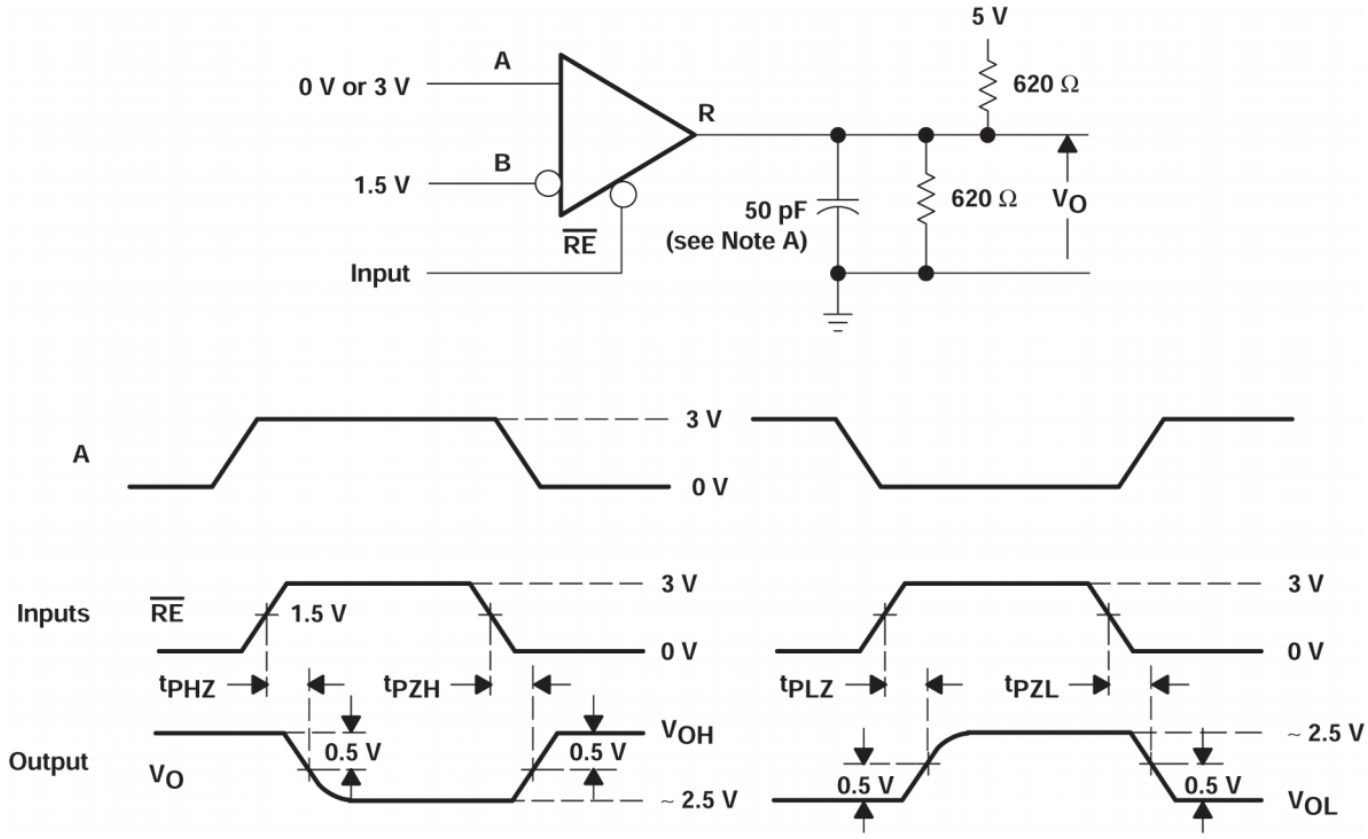
B. C_L includes probe and jig capacitance.

图 6-6. Driver T_{PZL} And T_{PLZ} Test Circuit and Voltage Waveforms



A. This value includes probe and jig capacitance (± 10%).

图 6-7. Receiver T_{PLH} And T_{PHL} Test Circuit and Voltage Waveforms

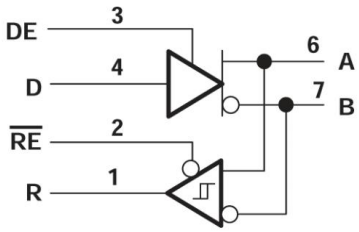


A. This value includes probe and jig capacitance (± 10%).

图 6-8. Receiver T_{PZL}, T_{PLZ}, T_{PZH}, And T_{PHZ} Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram



7.2 Device Functional Modes

表 7-1. Function Tables Driver

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

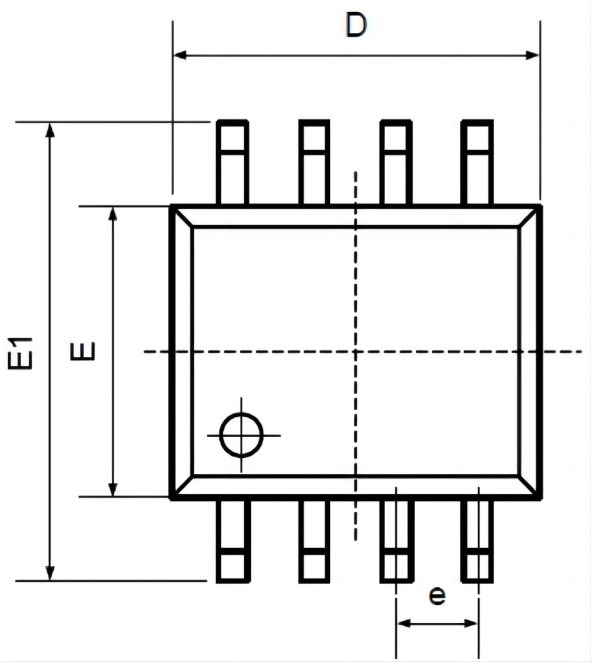
表 7-2. Function Tables Receiver

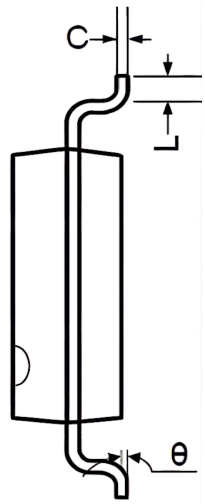
DIFFERENTIAL INPUTS	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geqslant 0.2$ V	L	H
-0.2V < V_{ID} < 0.2 V	L	?
$V_{ID} \leqslant -0.2$ V	L	L
X	H	Z
Open	L	H

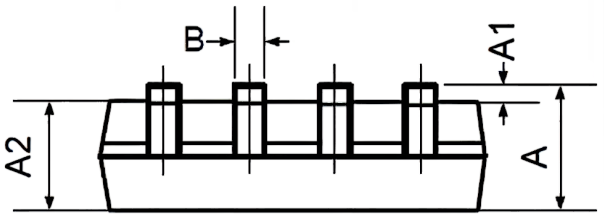
Order information

Order Number	Package	Package Quantity	Marking On The park
SN65LBC182DR-TUDI	SOP8	Tape,Reel,2500	SN65LBC182DR
SN65LBC182P-TUDI	DIP8	Tube,50,A box of 2000	SN65LBC182P
SN75LBC182DR-TUDI	SOP8	Tape,Reel,2500	SN75LBC182DR
SN75LBC182P-TUDI	DIP8	Tube,50,A box of 2000	SN75LBC182P

Package SOP8

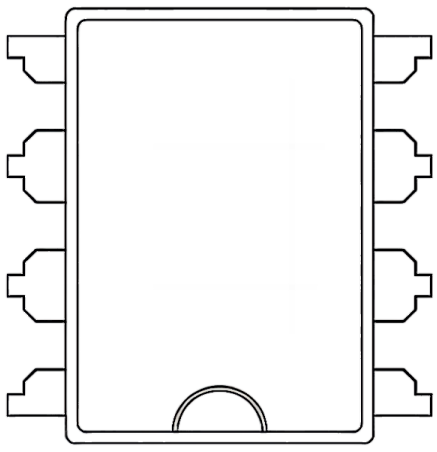


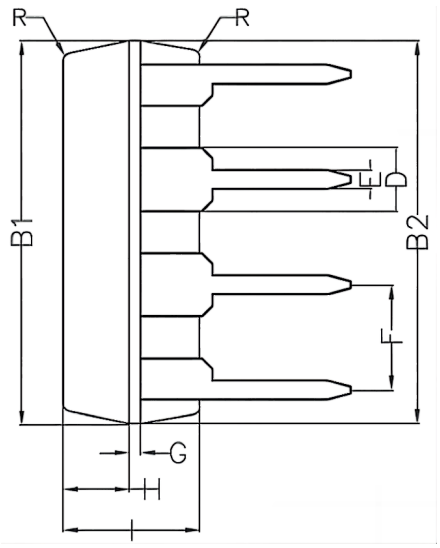


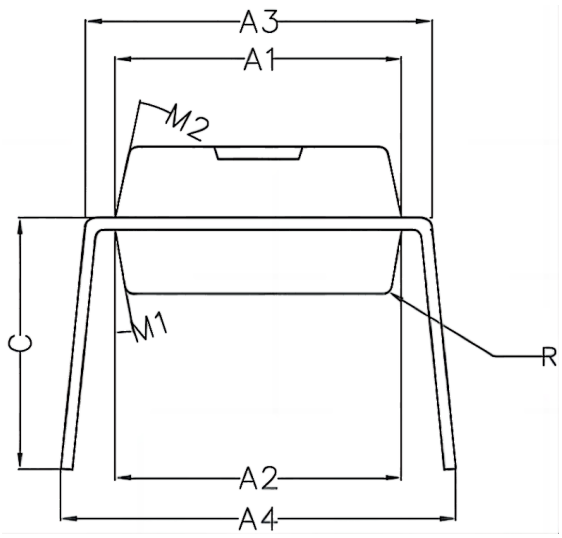


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package DIP8







Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

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