钍地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65HVD05/65HVD06/65HVD07 /SN75HVD05/75HVD06/75HVD07

高输出 RS-485 收发器

网址 www.sztdbdt.com

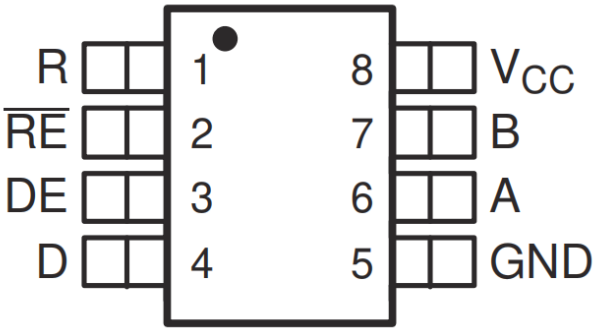
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

● Minimum differential output voltage into a 54 Ω load is 2.5V
● Fail-safe receiver for open, short and bus idle conditions
●1/8 unit load option available (up to 256 nodes on the bus)
●Bus pin ESD protection exceeds 16 kVBM
●Driver output slew rate control options
● Electrical characteristics comply with ANSI TIA/EIA-485-A standard
● Low current standby mode: 1μ (typical)
● Glitch-free power-up and power-down protection for hot-swap applications ? Pin compatible with industry-standard SN7517



D OR P PACKAGE
(TOP VIEW)

Applications

● Data transmission in long-distance, lossy lines or environments with electrical noise
●Profibus line interface
● Industrial process control networks
Point of Sale (POS) networks
●Power metering
● Building automation
● Digital motor control

Description

SN65HVD05, SN75HVD05, SN65HVD06, SN75VD06, SN65HVD07 and SN75HVD07 combine a three-state differential line driver and a differential line receiver. They are designed balanced data transmission and are interoperable with devices compliant with ANSI TIA/EIA-485-A and ISO 8482E standards. The driver provides differential output voltage greater than required by these standards, thereby improving noise immunity. The driver and receiver have high-level active and low-level active enable pins, respectively, which can externally connected together to serve as direction control.
The driver's differential output and the receiver's differential input are internally connected to form a differential input/output (I/O bus port, which provides a minimum load to the bus when the driver is disabled or unpowered. These devices have a wide positive and negative common-mode voltage range, making them for combined-line applications.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1) (2)

			SN65HVD05, SN65HVD06, SN65HVD07 SN75HVD05, SN75HVD06, SN75HVD07
Supply voltage range, V_{CC}			- 0.3 V to 6 V
Voltage range at A or B			- 9 V to 14 V
Input voltage range at D, DE, R or $\overline{RE}$			- 0.5 V to V_{CC} + 0.5 V
Voltage input range, transient pulse, A and B, through 100 Ω (see 图 6-11)			- 50 V to 50 V
Receiver output current, I_O			- 11 mA to 11mA
Electrostatic discharge	Human body model(3)	A, B, and GND	16 kV
		All pins	4 kV
	Charged-device model(4)	All pins	1 kV
Continuous total power dissipation			See Dissipation Rating Table

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under" recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

5.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5		5.5	V
Voltage at any bus terminal (separately or common mode) V_I or V_{IC}		- 7(1)		12	V
High-level input voltage, V_{IH}	D, DE, $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see 图 6-7)		- 12		12	V
High-level output current, I_{OH}	Driver	- 100			mA
	Receiver	- 8			
Low-level output current, I_{OL}	Driver			100	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65HVD05	- 40		85	°C
	SN65HVD06				
	SN65HVD07				
	SN75HVD05	0		70	°C
	SN75HVD06				
	SN75HVD07				

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

5.3 Thermal Information

THERMAL METRIC(1)		D (SOIC) SN65 Variation	D (SOIC) SN75 Variation	P (PDIP)	UNIT
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	175.4	125	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	53.6	34.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	45.1	23.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	10.1	12.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	44.4	23.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

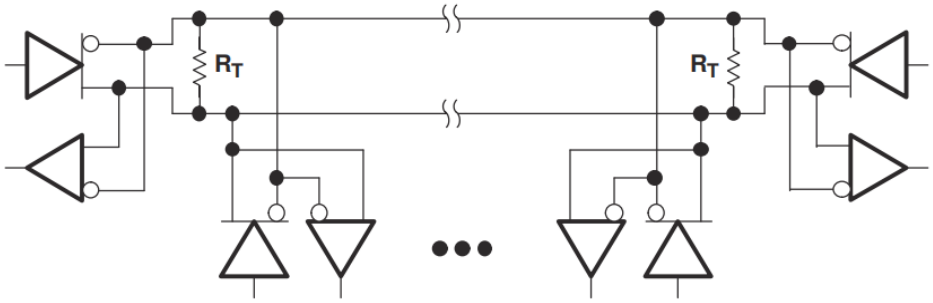
5.4 Package Dissipation Ratings

(See 图 5-1 and 图 5-2)

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D(2)	710 mW	5.7 mW/°C	455 mW	369 mW
D(3)	1282 mW	10.3 mW/°C	821 mW	667 mW
P	1000 mW	8.0 m W/°C	640 mW	520 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) Tested in accordance with the Low-K thermal metric definitions of EIA/JESD51-3
(3) Tested in accordance with the High-K thermal metric definitions of EIA/JESD51-7

Typical Application



Device	Number of Devices on Bus
HVD05	64
HVD06	256
HVD07	256

NOTE: The line should be terminated at both ends with its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

图 8-1. Typical Application Circuit

5.5 Driver Electrical Characteristics

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = – 18 mA		– 1.5			V
$\|V_{OD}\|$	Differential output voltage		No Load				V_{CC}	V
			R_L = 54 Ω, See 图 6-4		2.5			
			V_{test} = – 7 V to 12 V, See 图 6-2		2.2			
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage		See 图 6-4 and 图 6-2		– 0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage		See 图 6-3		2.2		3.3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage				– 0.1		0.1	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	HVD05	See 图 6-3			600		mV
		HVD06				500		
		HVD07				900		
I_{OZ}	High-impedance output current		See receiver input currents					
I_I	Input current	D			– 100		0	μA
		DE			0		100	
I_{OS}	Short-circuit output current		– 7 V ≤ V_O ≤ 12 V		– 250		250	mA
$C_{(diff)}$	Differential output capacitance		V_{ID} = 0.4 sin (4E6 π t) + 0.5 V, DE at 0 V			16		pF
I_{CC}	Supply current		$\overline{RE}$ at V_{CC}, D and DE at V_{CC}, No load	Receiver disabled and driver enabled		9	15	mA
			$\overline{RE}$ at V_{CC}, D at V_{CC} DE at 0 V, No load	Receiver disabled and driver disabled (standby)		1	5	μA
			$\overline{RE}$ at 0 V, D and DE at V_{CC}, No load	Receiver enabled and driver enabled		9	15	mA

(1) All typical values are at 25°C and with a 5-V supply.

5.6 Driver Switching Characteristics

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	HVD05	R_L = 54 Ω, C_L = 50 pF, See 图 6-4		6.5	11	ns
		HVD06			27	40	
		HVD07			250	400	
t_{PHL}	Propagation delay time, high-to-low-level output	HVD05			6.5	11	ns
		HVD06			27	40	
		HVD07			250	400	
t_r	Differential output signal rise time	HVD05		2.7	3.6	6	ns
		HVD06		18	28	55	
		HVD07		150	300	450	
t_f	Differential output signal fall time	HVD05		2.7	3.6	6	ns
		HVD06		18	28	55	
		HVD07		150	300	450	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	HVD05				2	ns
		HVD06				2.5	
		HVD07				10	
$t_{sk(pp)}$ (2)	Part-to-part skew	HVD05				3.5	ns
		HVD06				14	
		HVD07				100	
t_{PZH1}	Propagation delay time, high-impedance-to-high-level output	HVD05	$\overline{RE}$ at 0 V, R_L = 110 Ω, See 图 6-5			25	ns
		HVD06				45	
		HVD07				250	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	HVD05				25	ns
		HVD06				60	
		HVD07				250	
t_{PZL1}	Propagation delay time, high-impedance-to-low-level output	HVD05	$\overline{RE}$ at 0 V, R_L = 110 Ω, See 图 6-6			15	ns
		HVD06				45	
		HVD07				200	
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	HVD05				14	ns
		HVD06				90	
		HVD07				550	
t_{PZH2}	Propagation delay time, standby-to-high-level output		R_L = 110Ω , $\overline{RE}$ at 3 V, See 图 6-5			6	μs
t_{PZL2}	Propagation delay time, standby-to-low-level output		R_L = 110 Ω, $\overline{RE}$ at 3 V, See 图 6-6			6	μs

(1) All typical values are at 25°C and with a 5-V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

5.7 Receiver Electrical Characteristics

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		I_O = – 8 mA					– 0.01	V
V_{IT-}	Negative-going input threshold voltage		I_O = 8 mA			– 0.2			
V_{hys}	Hysteresis voltage (V_{IT+} - V_{IT-})						35		mV
V_{IK}	Enable-input clamp voltage		I_I = – 18 mA			– 1.5			V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = – 8 mA,	See 图 6-7	4			V
V_{OL}	Low-level output voltage		V_{ID} = -200 mV,	I_{OL} = 8 mA,	See 图 6-7			0.4	V
I_{OZ}	High-impedance-state output current		V_O = 0 or V_{CC}	$\overline{RE}$ at V_{CC}		– 1		1	μA
I_I	Bus input current	HVD05	Other inputat 0 V	V_A or V_B = 12 V			0.23	0.5	mA
				V_A or V_B = 12 V,	V_{CC} = 0 V		0.3	0.5	
				V_A or V_B = – 7 V		– 0.4	0.13		
				V_A or V_B = – 7 V,	V_{CC} = 0 V	– 0.4	0.15		
		HVD06 HVD07	Other inputat 0 V	V_A or V_B = 12 V			0.06	0.1	mA
				V_A or V_B = 12 V,	V_{CC} = 0 V		0.08	0.13	
				V_A or V_B = – 7 V		– 0.1	0.05		
				V_A or V_B = – 7 V,	V_{CC} = 0 V	– 0.05	0.03		
I_{IH}	High-level input current, $\overline{RE}$		V_{IH} = 2 V			– 60	26.4		μA
I_{IL}	Low-level input current, $\overline{RE}$		V_{IL} = 0.8 V			– 60	27.4		μA
$C_{(diff)}$	Differential input capacitance		V_I = 0.4 sin (4E6 π t) + 0.5 V, DE at 0 V				16		pF
I_{CC}	Supply current		$\overline{RE}$ at 0 V, D and DE at 0 V, No load	Receiver enabled and driver disabled			5	10	mA
			$\overline{RE}$ at V_{CC}, DE at 0 V, D at V_{CC}, No load	Receiver disabled and driver disabled (standby)			1	5	μA
			$\overline{RE}$ at 0 V, D and DE at V_{CC}, No load	Receiver enabled and driver enabled			9	15	mA

(1) All typical values are at 25°C and with a 5-V supply.

5.8 Receiver Switching Characteristics

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output 1/2 UL	HVD05	V_{ID} = – 1.5 V to 1.5 V, C_L = 15 pF, See 图 6-8		14.6	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output 1/2 UL	HVD05			14.6	25	ns
t_{PLH}	Propagation delay time, low-to-high-level output 1/8 UL	HVD06			55	70	ns
		HVD07			55	70	
t_{PHL}	Propagation delay time, high-to-low-level output 1/8 UL	HVD06			55	70	ns
		HVD07			55	70	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	HVD05				2	ns
		HVD06				4.5	
		HVD07				4.5	
$t_{sk(pp)}$ (2)	Part-to-part skew	HVD05				6.5	ns
		HVD06				14	
		HVD07				14	
t_r	Output signal rise time		C_L = 15 pF, See 图 6-8		2	3	ns
t_f	Output signal fall time				2	3	
t_{PZH1}	Output enable time to high level		C_L = 15 pF, DE at 3 V, See 图 6-9			10	ns
t_{PZL1}	Output enable time to low level					10	
t_{PHZ}	Output disable time from high level					15	
t_{PLZ}	Output disable time from low level					15	
t_{PZH2}	Propagation delay time, standby-to-high-level output		C_L = 15 pF, DE at 0, See 图 6-10			6	μs
t_{PZL2}	Propagation delay time, standby-to-low-level output					6	

(1) All typical values are at 25°C and with a 5-V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

5.9 Typical Characteristics (continued)

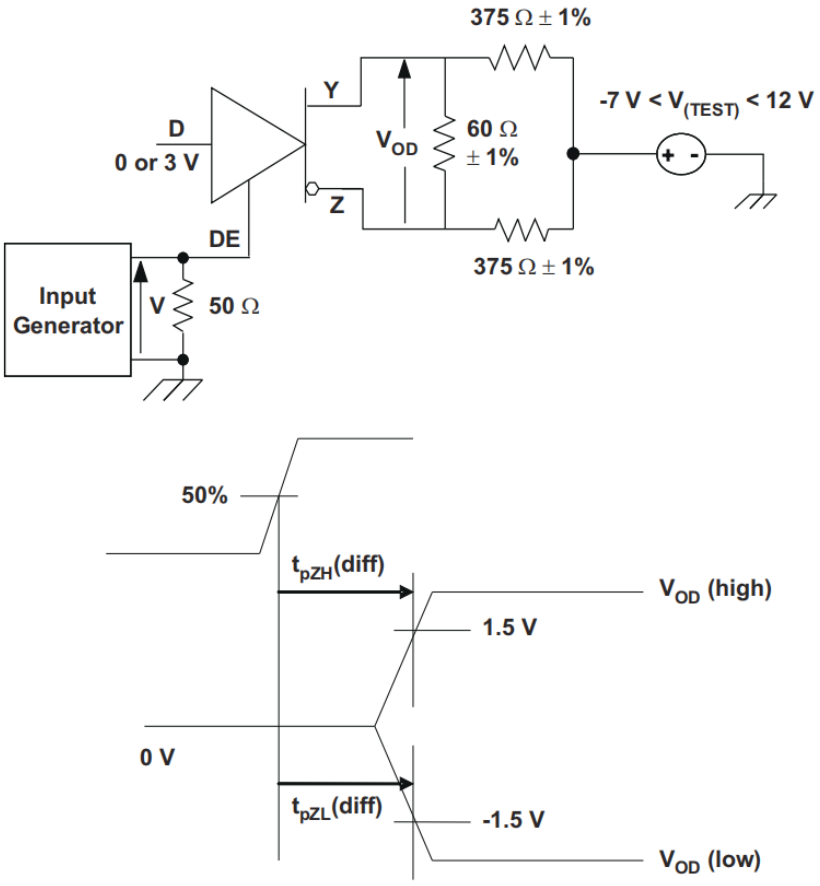


图 5-13. Driver Enable Time From DE to V_{OD}

Parameter Measurement Information

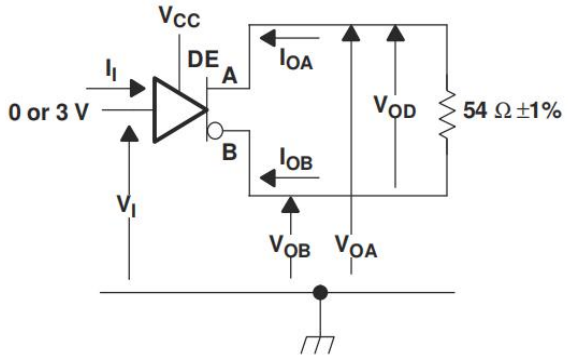


图 6-1. Driver V_{OD} Test Circuit and Voltage and Current Definitions

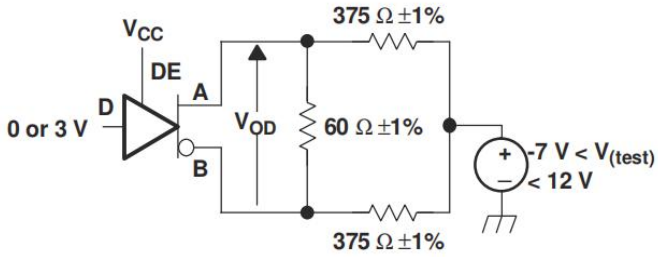
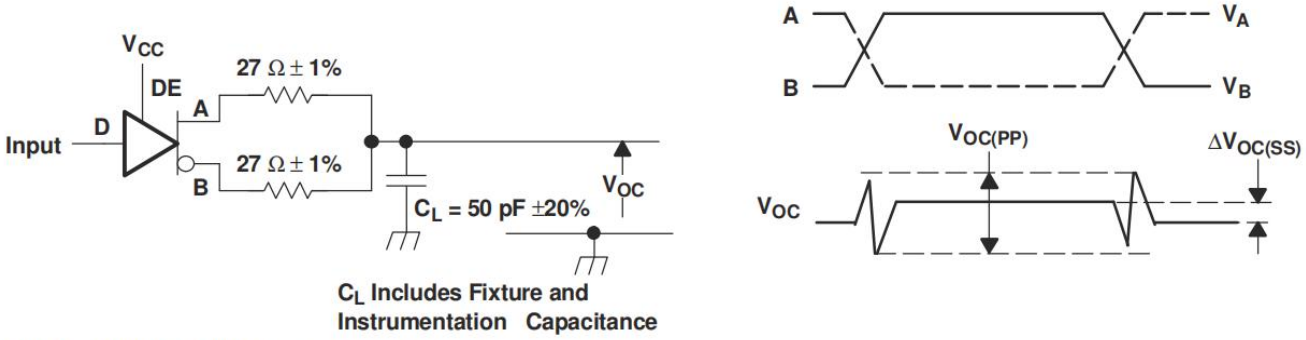
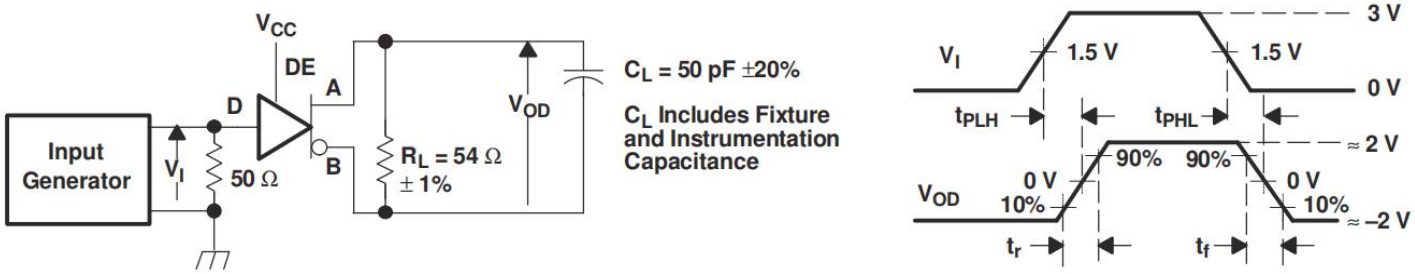


图 6-2. Driver V_{OD} With Common-Mode Loading Test Circuit



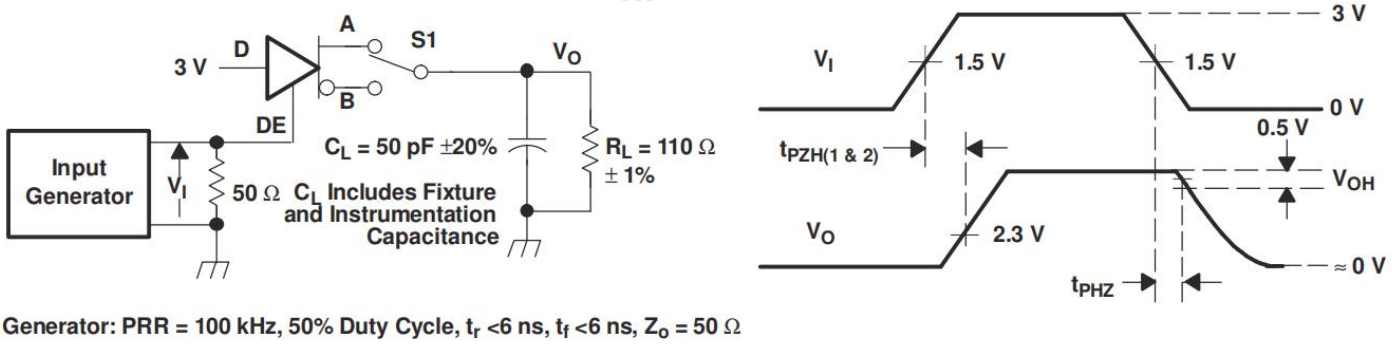
Input: PRR = 500 kHz, 50% Duty Cycle,t_r<6ns, t_f<6ns, Z_O = 50 Ω

图 6-3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



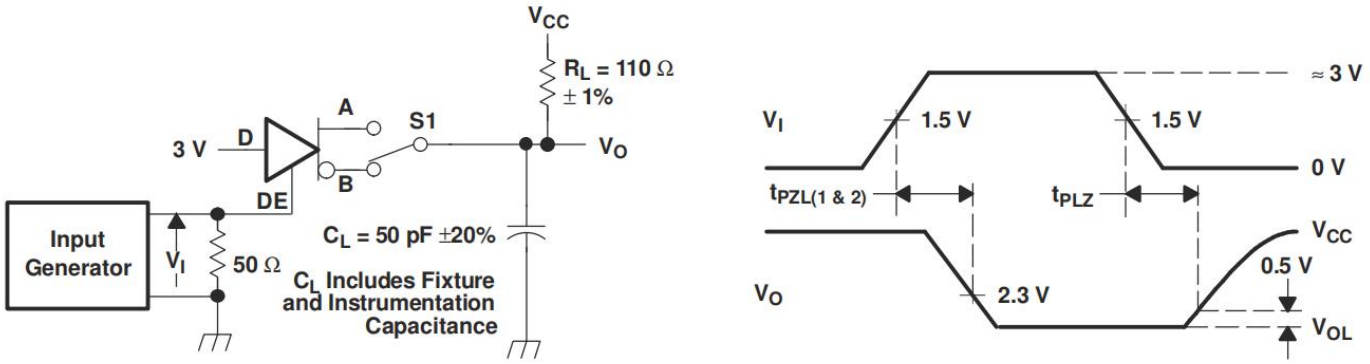
Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

图 6-4. Driver Switching Test Circuit and Voltage Waveforms



Generator: PRR = 100 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

图 6-5. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 100 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

图 6-6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

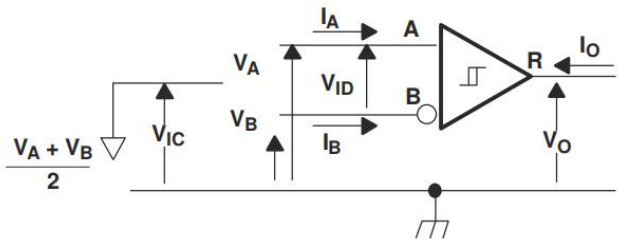
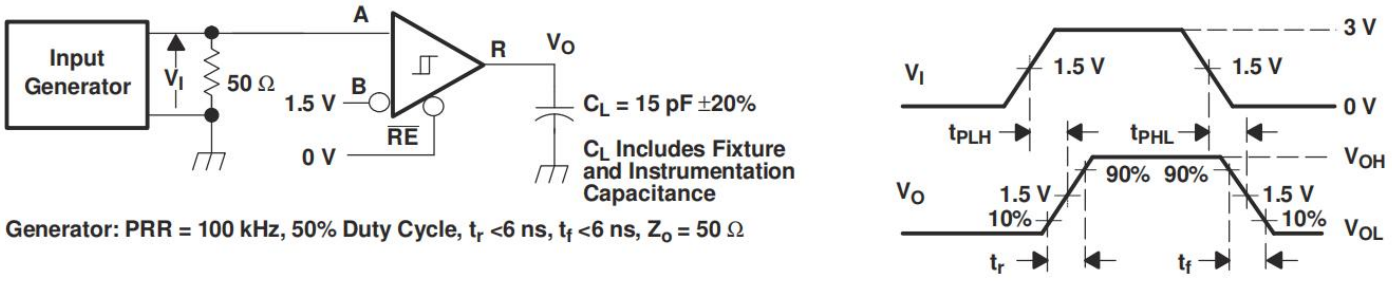


图 6-7. Receiver Voltage and Current Definitions



Generator: PRR = 100 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

图 6-8. Receiver Switching Test Circuit and Voltage Waveforms

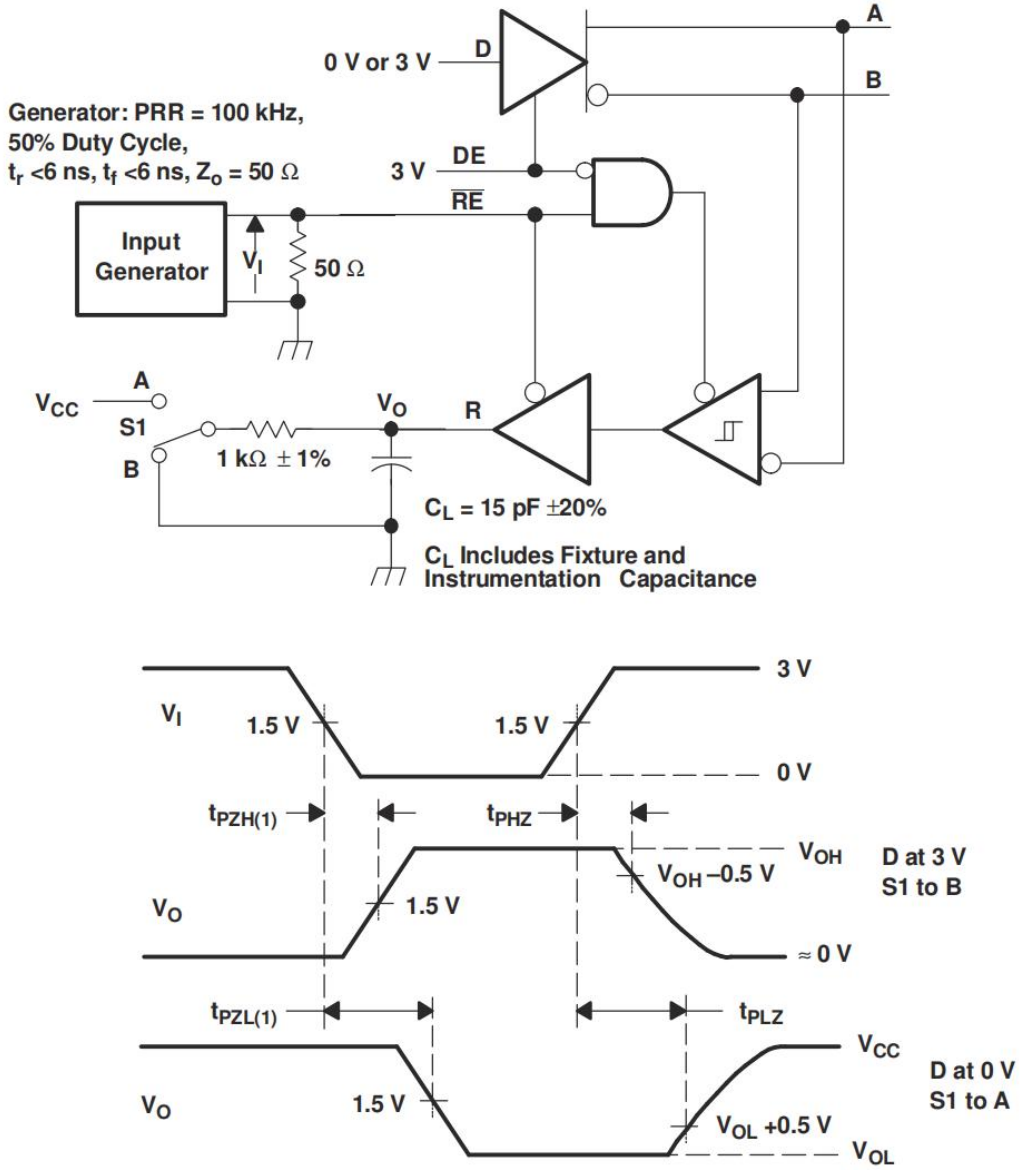


图 **6-9. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled**

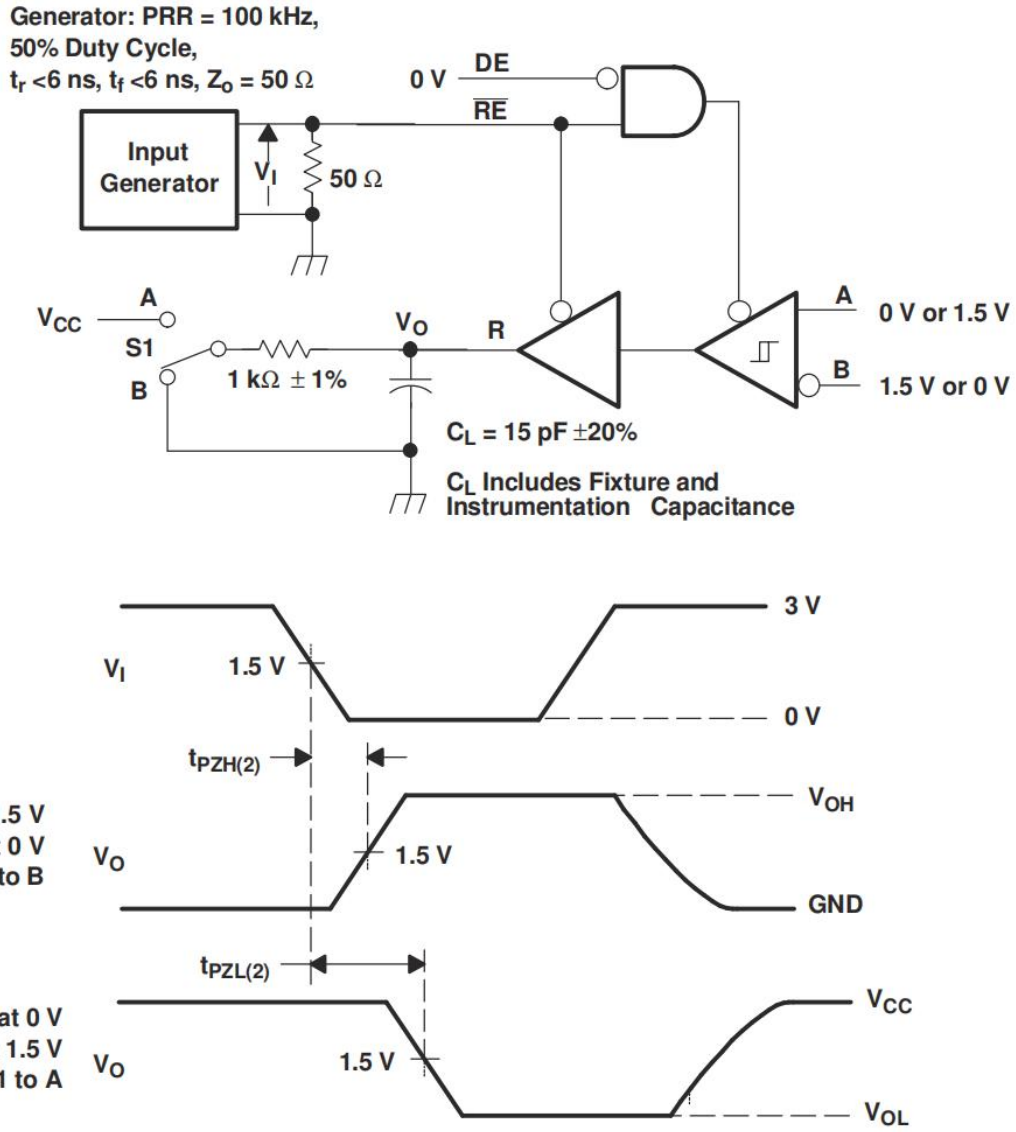
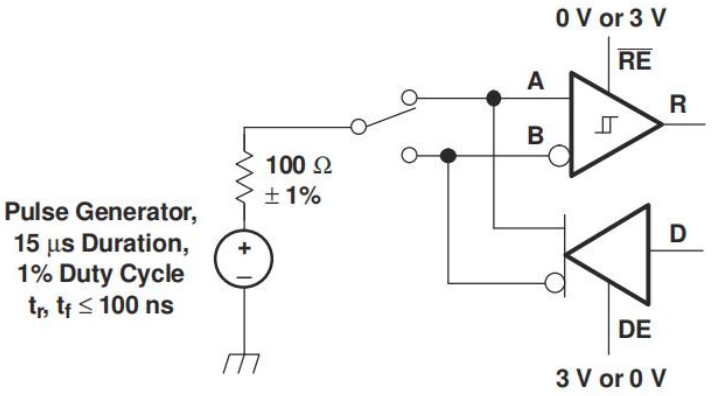


图 6-10. Receiver Enable Time From Standby (Driver Disabled)



NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

图 6-11. Test Circuit, Transient Over Voltage Test

6 Function Tables

表 6-1. DRIVER

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L
X	Open	Z	Z

表 6-2. RECEIVER

DIFFERENTIAL INPUTS(1)	ENABLE	OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \leqslant -0.2$ V	L	L
-0.2 V < V_{ID} < -0.01 V	L	?
-0.01 V $\leqslant V_{ID}$	L	H
X	H	Z
Open Circuit	L	H
Short Circuit	L	H
IDLE Bus	L	H
X	Open	Z

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

6.1 Receiver Failsafe

The differential receiver is “failsafe” to invalid bus states caused by:

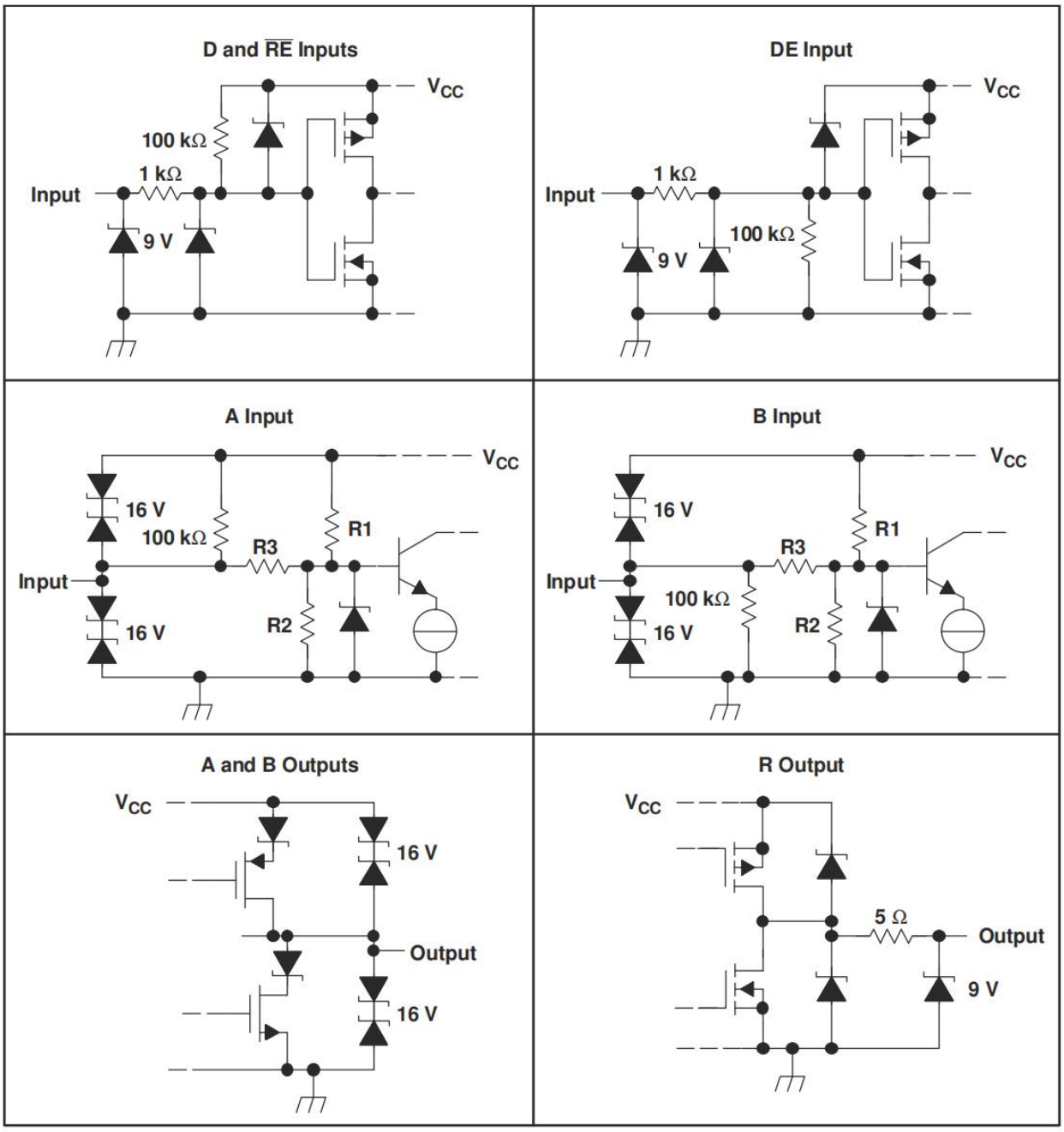
- open bus conditions such as a disconnected connector,
- shorted bus conditions such as cable damage shorting the twisted-pair together, or
- idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic High state, so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds so that the “input indeterminate” range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output *must* output a High when the differential input V_{ID} is more positive than +200 mV, and *must* output a Low when the V_{ID} is more negative than -200 mV. The receiver parameters which determine the failsafe performance are V_{IT+} and V_{IT-} and V_{HYS}. As seen in the Receiver Electrical Characteristics table, differential signals more negative than -200 mV will always cause a Low receiver output. Similarly, differential signals more positive than +200 mV will *always* cause a High receiver output.

When the differential input signal is close to zero, it will still be above the V_{IT+} threshold, and the receiver output is High. Only when the differential input is more negative than V_{IT-} will the receiver output transition to a Low state. So, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value V_{HYS} (the separation between V_{IT+} and V_{IT-}) as well as the value of V_{IT+}.

7 Equivalent Input and Output Schematic Diagrams

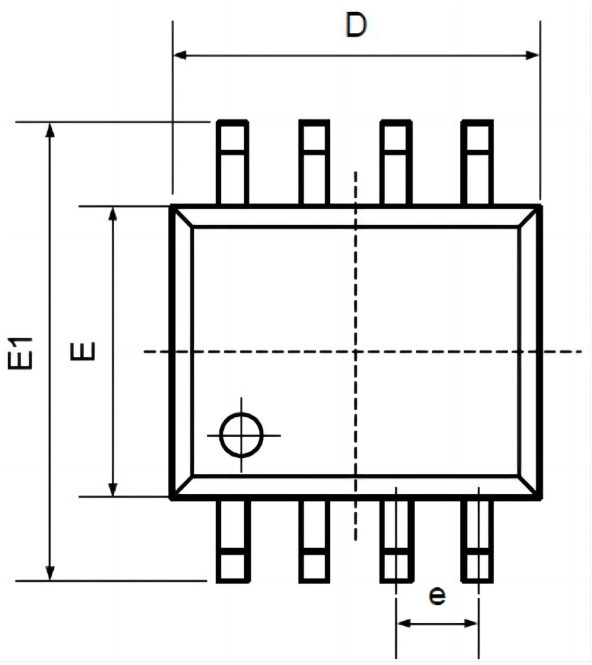


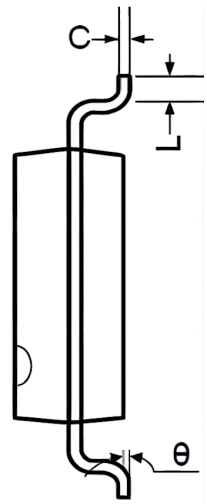
	R1/R2	R3
SN65HVD05	9 kΩ	45 kΩ
SN65HVD06	36 kΩ	180 kΩ
SN65HVD07	36 kΩ	180 kΩ

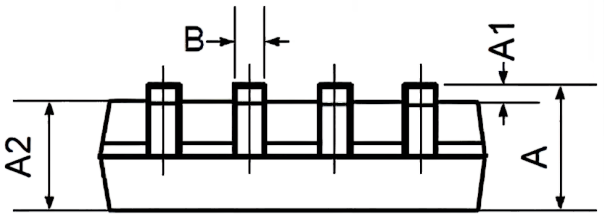
Order information

Order Number	Package	Package Quantity	Marking On The park
SN65HVD05DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD05DR
SN65HVD05P-TUDI	DIP8	Tube,50,A box of 2000	SN65HVD05P
SN65HVD06DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD06DR
SN65HVD06P-TUDI	DIP8	Tube,50,A box of 2000	SN65HVD06P
SN65HVD07DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD07DR
SN65HVD07P-TUDI	DIP8	Tube,50,A box of 2000	SN65HVD07P
SN75HVD05DR-TUDI	SOP8	Tape,Reel,2500	SN75HVD05DR
SN75HVD05P-TUDI	DIP8	Tube,50,A box of 2000	SN75HVD05P
SN75HVD06DR-TUDI	SOP8	Tape,Reel,2500	SN75HVD06DR
SN75HVD06P-TUDI	DIP8	Tube,50,A box of 2000	SN75HVD06P
SN75HVD07DR-TUDI	SOP8	Tape,Reel,2500	SN75HVD07DR
SN75HVD07P-TUDI	DIP8	Tube,50,A box of 2000	SN75HVD07P

Package SOP8

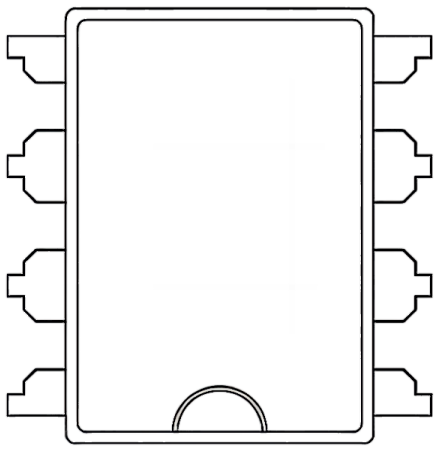


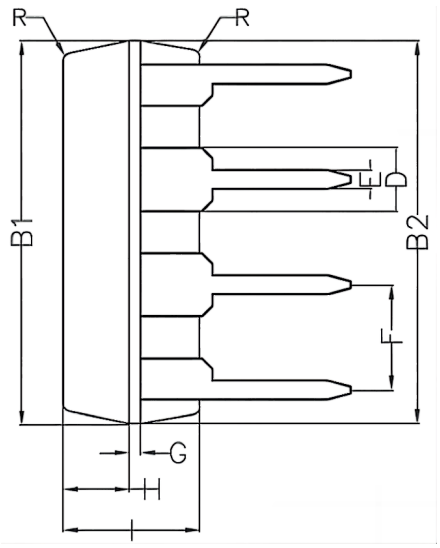


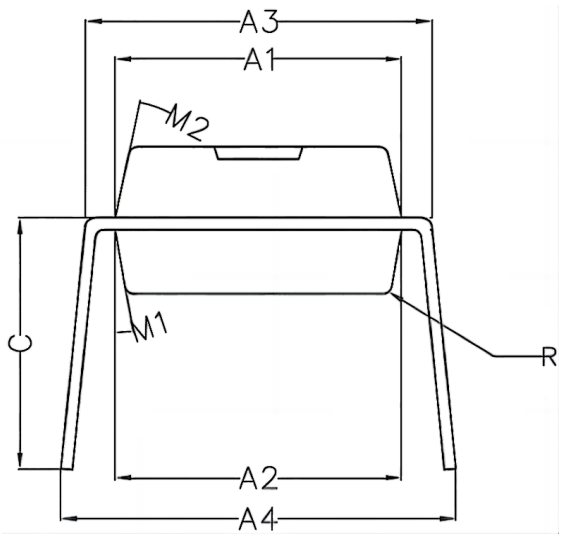


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package DIP8







Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

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